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4643 PRINTER

SERVICE MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

MANUAL PART NO. 070-3870-01
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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This service manual describes the Tektronix, Inc., 4643 Matrix Printer. This printer is manufactured for Tektronix, Inc., by Dataproducts Corporation, Woodland Hills, California. It is referred to in this manual as the "printer," or the Model M200.

The 4643 Printer produces paper copy of the alphanumeric output from devices such as the Tektronix 4050-Series.

WARRANTY SERVICE

If your 4643 Printer should require any service during the warranty period, call your nearest Tektronix Service Center. Only Tektronix service personnel will perform repair or maintenance work under terms of the Tektronix, Inc., warranty.

1.2 FEATURES

The 4643 Printer, Figure 1-1, is a general purpose, medium-speed, serial impact printer designed for use as an output device for information processing systems. It features a dual-column, 14-wire matrix print head that combines the speed of multiple-head printers with the flexibility of single-head printers. Driven by a motor, the print head moves horizontally and prints in both directions, further enhancing print speed. The print head has a life expectancy of more than 300 million characters, and is operator-replaceable.

Paper may be loaded from the front, bottom, or rear (optional). Horizontal and vertical alignment guides allow precise positioning of the paper forms. The ribbon is housed in an easy-to-load cassette, and may be changed quickly and cleanly by the operator. Other features include condensed print, paper-out switch, forms thickness control, status display, built-in self test, and automatic line feed.



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Figure 1-1. 4643 Printer

1.3 PRINTING PRINCIPLES (Figure 1-2)

The printer uses a 14-wire print head to produce dot pattern characters. The 14 print wires are arranged in two vertical columns of seven wires each. Printing is accomplished by selectively energizing 14 solenoids associated with the print wires. When a solenoid is energized, it strikes its associated print wire against the inked ribbon, paper, and platen, leaving a dot impression on the paper.

Characters are formed by combining a multiple of dots in a seven-vertical by seven-horizontal matrix; i. e., each character falls within an imaginary grid formed by the seven-wire height of the print wire columns and seven vertical dot columns. Three vertical dot columns are allotted for inter-character spacing. Figure 1-3 illustrates the dot configuration of the character "M" within the matrix.

The print head is mounted on a motor-driven shuttle mechanism, and moves at a fixed rate either from left to right or from right to left in parallel with the paper and platen. When moving from left to right, the right column of seven print wires reaches any given dot column before the left column. Similarly, when moving from right to left, the left column reaches any given dot column first, followed by the right column.

When a print wire is fired, it needs a finite amount of recovery time before it can be fired again. This recovery time, plus the wire firing time, is approximately equal to the amount of time it takes a wire column to move four dot columns. For example, a print wire fired in dot column 1 cannot be fired again until it reaches dot column 5. For this reason the print load is shared equally between both wire columns. Thus, a character may not be completely printed until the trailing wire column has reached the last printable dot column. In the example shown in figure 1-3, the right wire column fires wire 2 at dot column 2, wire 3 at dot column 3, wire 4 at dot column 4, and wires 1, 2, 3, 5, 6, and 7 at dot column 7. The left wire column fires all wires at dot column 1, wire 3 at dot column 5, wire 2 at dot column 6, and wire 4 at dot column 7. Other characters are printed in a similar manner. The wire firing assignments for each character are contained in a character generator ROM in the Processor Circuit Card Assembly.

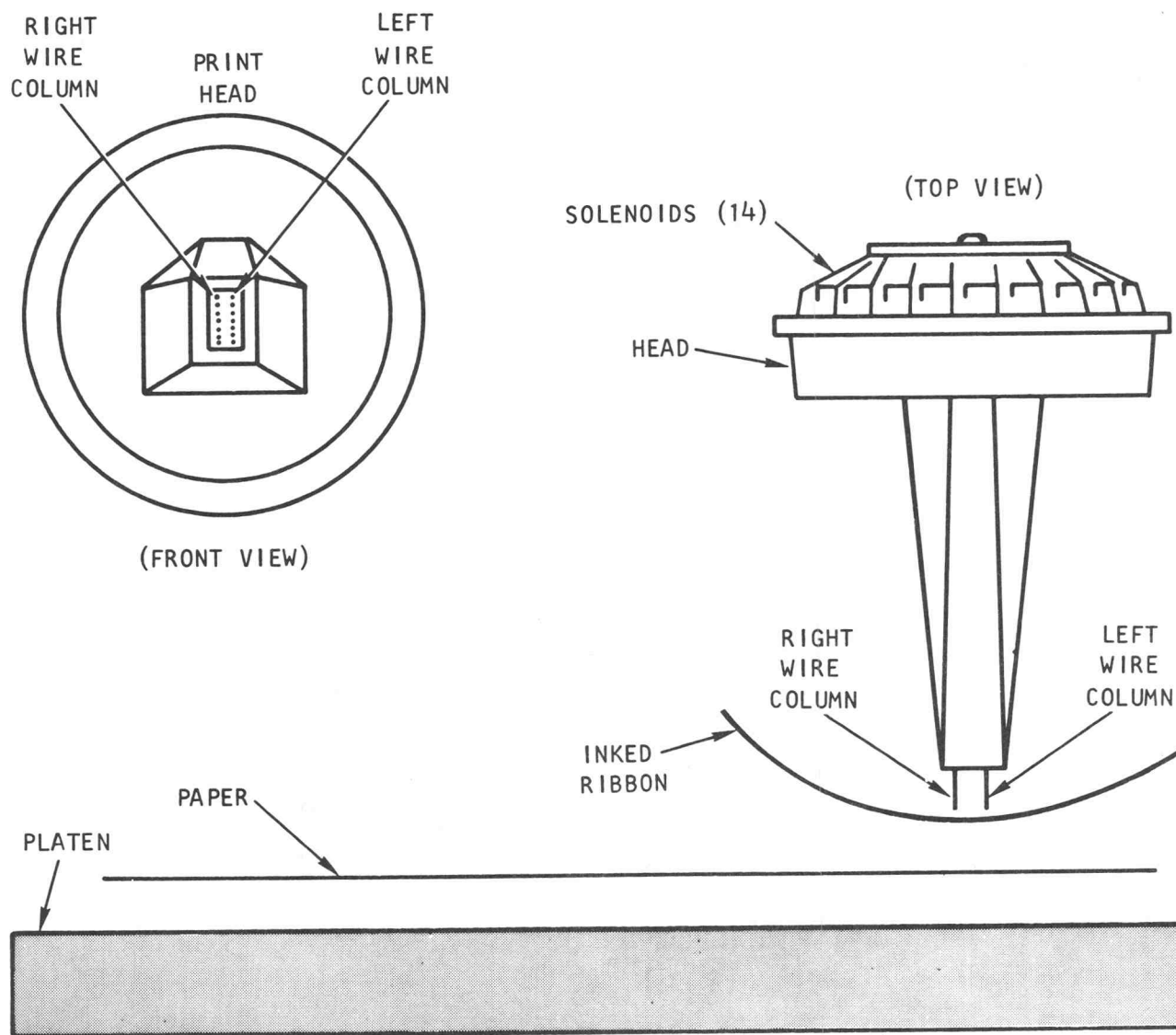
1.4 PHYSICAL DESCRIPTION (Figures 1-4 through 1-6)

The printer is made up of seven major physical components, as follows:

- a. Print Head
- b. Shuttle Components
- c. Ribbon Cassette and Drive Motor
- d. Paper Feed Components
- e. Power Supply
- f. Control Panel
- g. Circuit Card Assemblies

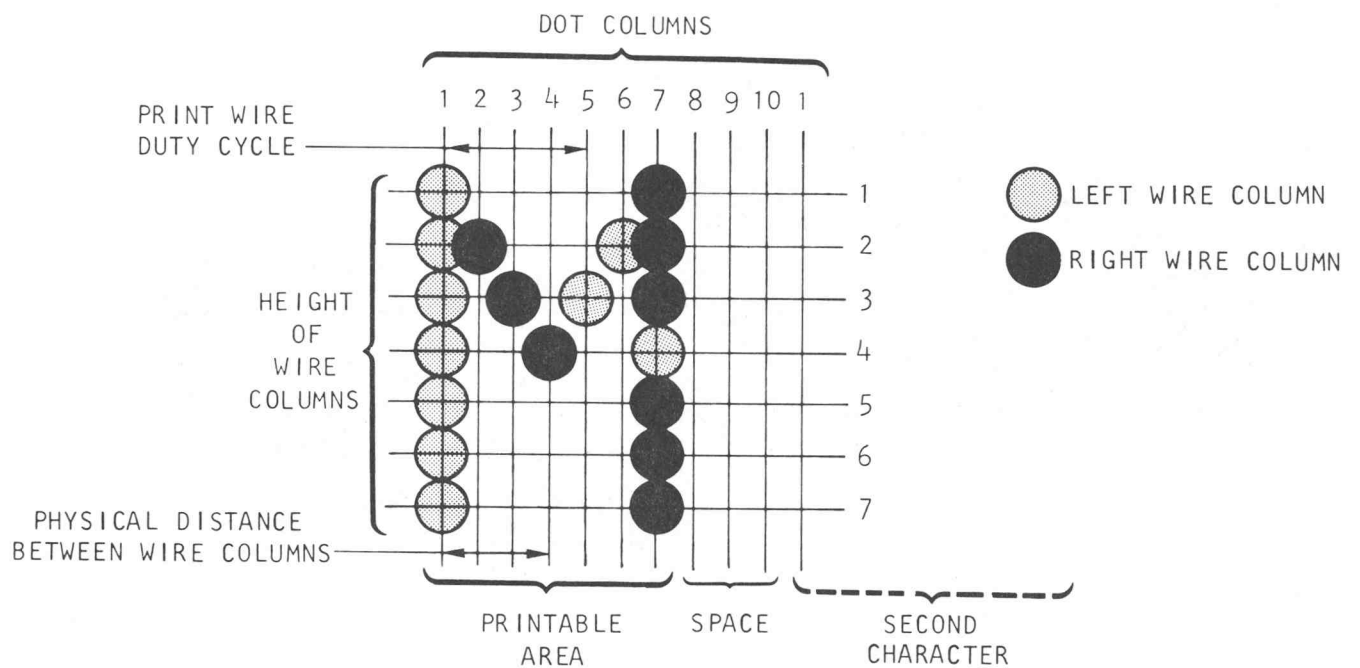
These components are enclosed in a clamshell plastic package, and mounted on the bottom half of the package. The two halves of the clamshell package are

GENERAL DESCRIPTION



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Figure 1-2. Printing Technique



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Figure 1-3. Character Matrix

GENERAL DESCRIPTION

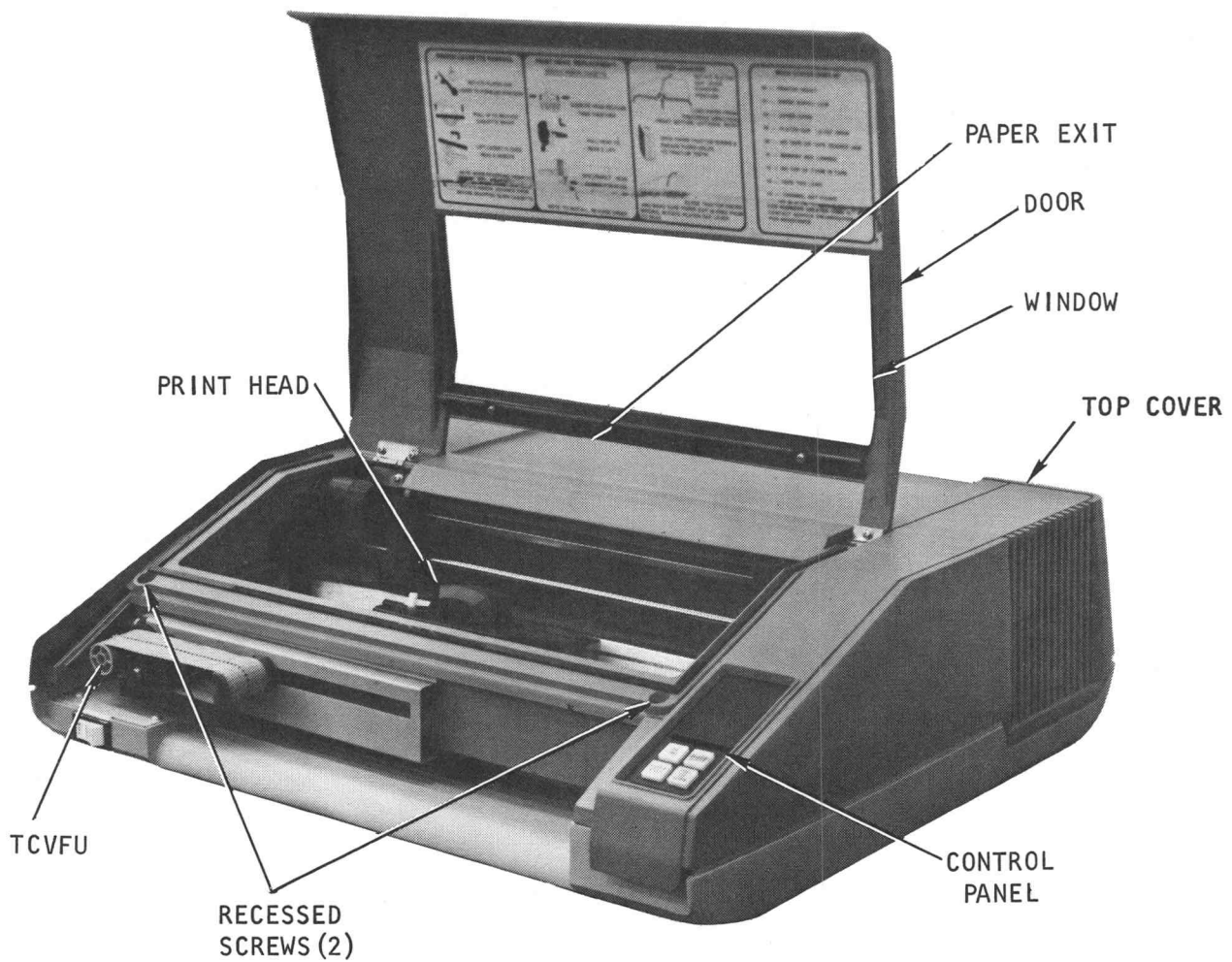


Figure 1-4. 4643 Printer, $\frac{3}{4}$ View, Window Raised

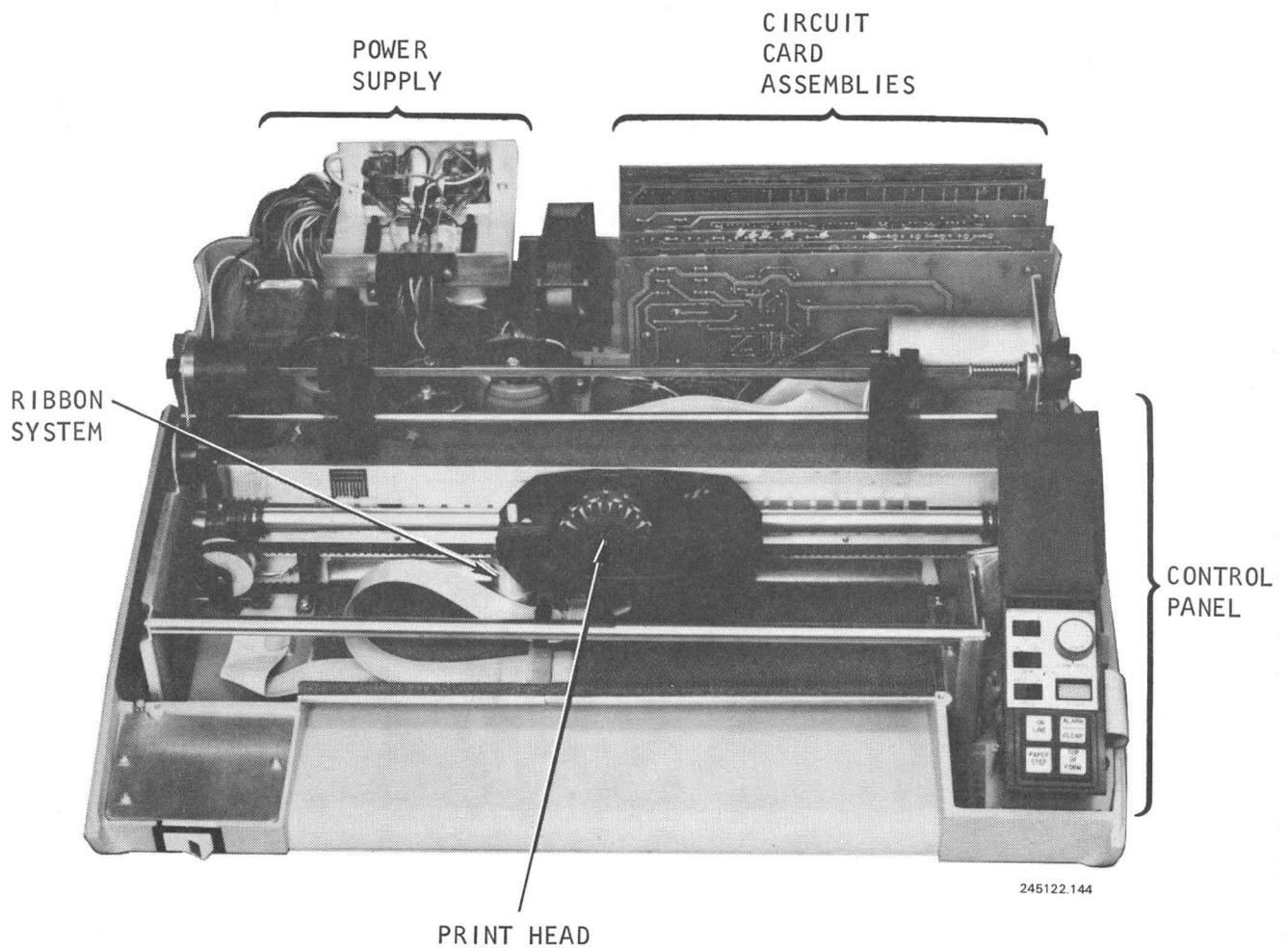


Figure 1-5. Printer Front View, Cover Removed

GENERAL DESCRIPTION

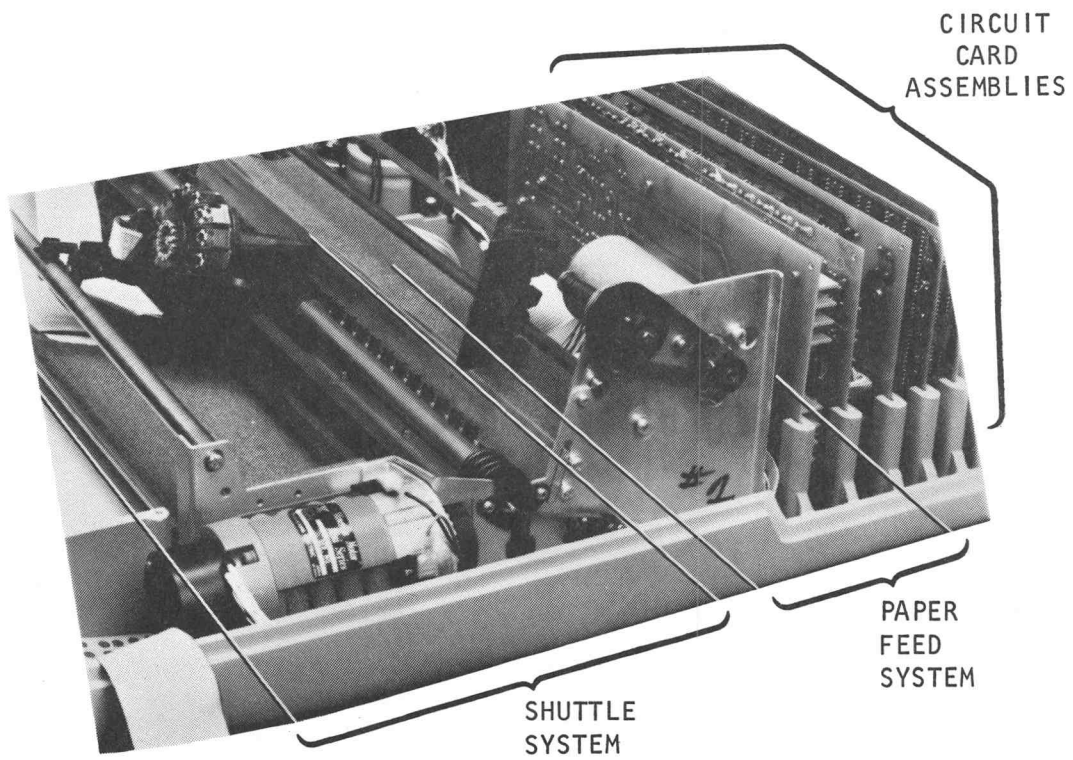


Figure 1-6. Printer Right Side View, Cover Removed

locked at the back by two quick-release latches, and secured at the front by two recessed screws. To gain access to all components of the printer, the top portion of the clamshell package, the top cover, is removed. The control panel is housed within the front right of the top cover, and fastened by a spring-loaded clip. When removing the top cover, the control panel is detached and placed in a recessed area within the printer chassis (see the top cover removal procedure in section V). A hinged portion of the top cover, the door, is raised as shown in figure 1-4 to gain access to the print head and ribbon cassette. A plastic window within the door allows for viewing the line currently being printed while the door is closed. Paper exits at the top through a slot within the top cover.

1.5 PRINTER ASSEMBLY ORGANIZATION AND DESCRIPTION

The printer assemblies and their interconnections are illustrated in figure 1-7. With the exception of the Tape Controlled Vertical Format Unit (TCVFU) option, all assemblies are interconnected either directly or by cable via the Mother Board Circuit Card Assembly (A7). The TCVFU interfaces with the printer via the Interface Circuit Card Assembly (A2).

Circuit card assemblies A2 through A6 are interconnected with the printer via P1 and P2 on the Mother Board Circuit Card Assembly (CCA). All other assemblies are connected with the Mother Board CCA by plug and jack, as shown in figure 1-7. The J14 (PA) and J15 (PB) shown in figure 1-7 are allocated for option plugs when the printer is configured with the options described in section VII.

The following assemblies are described in subsequent paragraphs:

- a. Power Supply Components and Regulator Circuit Card Assembly
- b. Interface Circuit Card Assembly
- c. Processor Circuit Card Assembly
- d. Motor Driver Circuit Card Assembly
- e. Wire Driver Circuit Card Assembly
- f. Printhead and Shuttle Mechanism
- g. Ribbon Control Components
- h. Paper Feed Components
- i. Control Panel

1.5.1 Power Supply Components and Regulator Circuit Card Assembly

a. Power Supply Components - The power supply is comprised of discrete components as illustrated in the block diagram shown in figure 1-8. The standard power supply includes a ferro-resonant transformer and resonant capacitor which operates with an incoming single phase power source ranging from 102 to 132 VAC at a frequency of 60 Hz. The optional universal power supply used for international operation is described in section VII.

Line filter L1 suppresses the high frequency transients during printer operation. Thermostat S2 prevents the heat sink temperature of bridge rectifiers CR1 and CR2 from exceeding 75°C. Filter capacitors C1 through C3 filter the unregulated ± 21 VDC and 9 VDC for distribution.

GENERAL DESCRIPTION

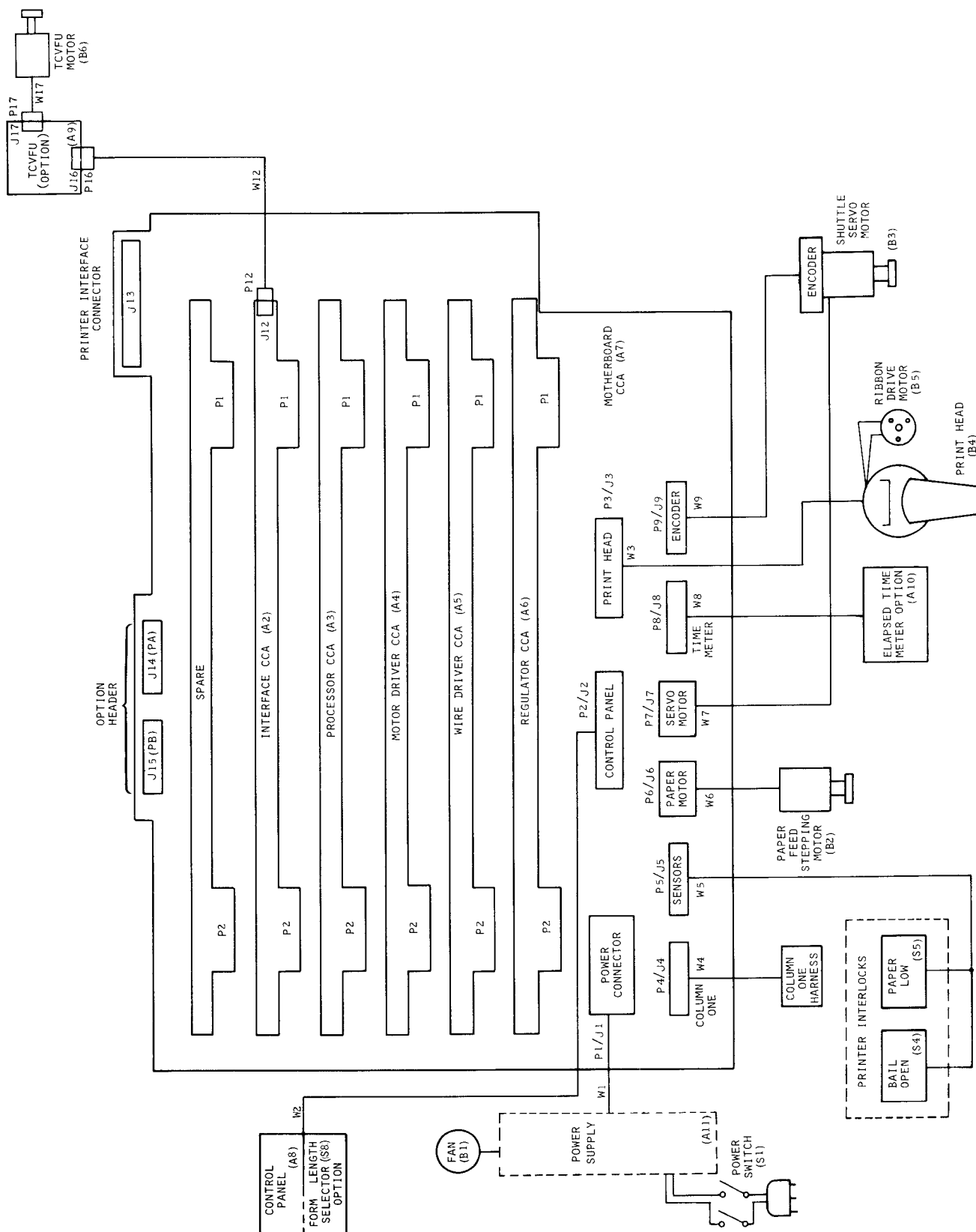


Figure 1-7. Printer Assembly, Interconnection Diagram

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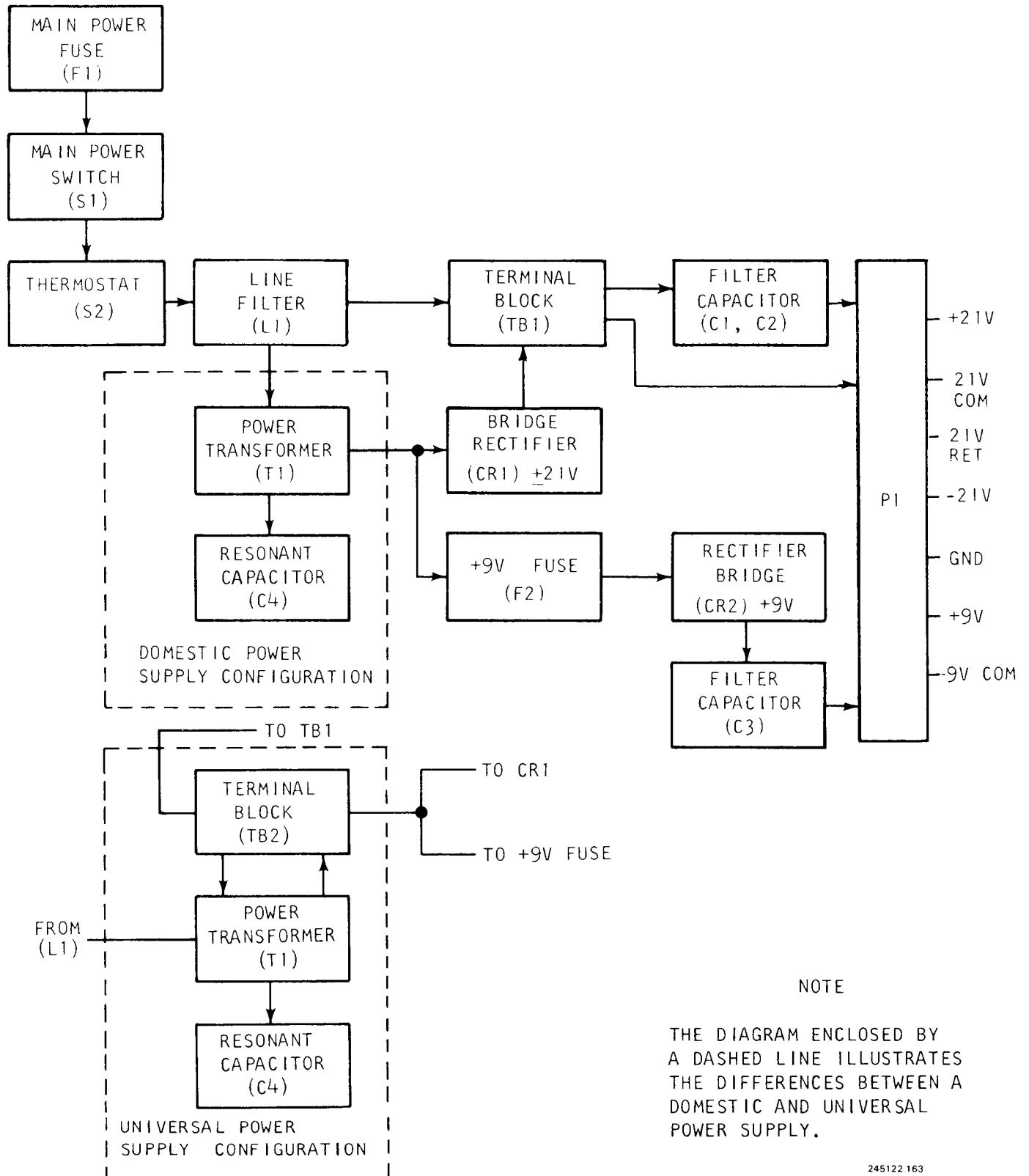


Figure 1-8. Power Supply Block Diagram

GENERAL DESCRIPTION

b. Regulator CCA - The regulator CCA (A6) receives filtered inputs of ± 21 VDC and $+9$ VDC, and outputs regulated ± 12 VDC, $+9$ VDC and an adjustable $+5$ VDC (see section V). The regulated voltage outputs from the regulator CCA are placed on the P1 and P2 buses of the Mother Board CCA and distributed throughout the printer.

1.5.2 Interface Circuit Card Assembly (A2)

The primary function of the Interface CCA is to interface the user system with the printer. Interface requirements differ among the various user systems with which the printer can operate. For this reason, the printer may be configured with the standard Interface CCA described in this section, or with one of the following optional Interface CCAs: DPC Parallel Long Line Interface CCA, DPC Centronics-Compatible Interface CCA, or Serial Interface CCA. Optional interface signals are described in sections IV and VI.

The standard Interface CCA (A2) is a short-line interface circuit card assembly which operates at a maximum cable length of 49 feet (15 meters). It is recommended that the interface cable be constructed of 22 AWG insulated wire. Each signal in the cable should be transmitted over a twisted wire pair, with one of the wires serving as a return. Voltage levels for signals transmitted over this interface are defined as follows:

Logic "1" Signal: Must be greater than $+2.5$ VDC and less than $+5.5$ VDC.

Logic "0" Signal: Must be equal to or greater than 0.0 VDC and less than $+0.5$ VDC.

The short line Interface CCA receives standard codes in bit parallel format. Data transfer between the user system and the printer is on a demand/response basis. Standard interface signals that the printer recognizes are listed below:

DATA STROBE
READY
ON LINE
DEMAND
DATA

The timing relationship of these signals is detailed in section IV. Connector pin and signal assignments and interface cable construction information are provided in section II.

Operation of the standard interface communications (handshaking) is as follows:

a. When the printer is able to be put on line by the operator, the READY signal goes active.

b. After the READY signal goes active, the DEMAND signal will go active to request data from the user.

- c. In response to the DEMAND signal, the user will place data on the data lines and activate the STROBE signal.
- d. The printer samples and stores the character transmitted on the data lines.
- e. Once the data lines have been sampled, the DEMAND signal goes inactive.
- f. When the user detects that the DEMAND line has gone inactive, the STROBE signal can then go inactive.
- g. Once the character has been stored, the printer verifies that the STROBE signal is inactive, then activates DEMAND again for the next character.

1.5.3 Processor Circuit Card Assembly (A3)

The Processor CCA is a microprocessor system which controls all functions of the printer, including character generation, paper motion, head motion, data transfer functions, and operator controls. It allows for maximum print throughput by the use of bi-directional printing. The Processor CCA "looks ahead" at the next line of print to determine the proper starting point for minimum print head motion.

The Processor CCA includes a variable timing circuit which controls the period of time that the wire driver circuits are turned on and off. Procedures for adjustment of this circuit are given in section V.

1.5.4 Motor Driver Circuit Card Assembly (A4)

The Motor Driver CCA provides the means of driving the three motors used in the printer -- the shuttle servo motor, the paper feed stepping motor, and the ribbon drive motor.

The Motor Driver CCA controls the starting, stopping, reversing, and velocity of the shuttle servo motor (B4) which drives the shuttle mechanism. A high efficiency power amplifier is used to drive the motor. Velocity information to the servo circuitry is provided by signals from the encoder disc mounted on the motor shaft. Motor stalling is detected and amplifier shut-down is automatically effected for safety purposes in the event that print head motion is impeded. This assembly also includes the adjustment for controlling the shuttle speed. Procedures for adjusting the speed control are given in section V.

GENERAL DESCRIPTION

The Motor Driver CCA also supplies the drive current pulses to the paper feed step motor (B2) to move the paper and to maintain the position of the paper during the print process.

Current for the ribbon drive motor is supplied from this assembly during printing operation. Ribbon motion occurs only when the shuttle servo motor and/or the paper feed motor is operating.

1.5.5 Wire Driver Circuit Card Assembly (A5)

This assembly supplies current to each of the print head solenoids as determined by control signals from the Processor CCA. The Wire Driver CCA also contains replaceable fuses for each pair of drive circuits. This prevents damage to the solenoids from excess current in the event of a malfunction.

1.5.6 Print Head and Shuttle Mechanism

The printer uses a dual-column 14-wire print head, which generates characters in a 7 x 7 matrix at a rate of 340 characters per second. The print wires are arrayed in two vertical columns of seven wires with each wire actuated by a clapper-type solenoid.

The print head is mounted on a shuttle mechanism that is moved across the print line by a constant velocity DC servo motor. As the shuttle mechanism traverses the printing area, it is guided by means of two parallel bars. Two self-lubricating journal bearings hold the shuttle mechanism to the rear bar, while a single bearing guides the front edge of the shuttle mechanism along the second bar. This arrangement secures the print head in the proper relationship to the platen during printing operation.

The shuttle mechanism is moved bi-directionally at a constant velocity by the shuttle servo motor and belt. Constant tension is maintained on the belt by an idler pulley assembly. Column position information is obtained from an encoder disc mounted on the shuttle servo motor shaft. A transducer is used to indicate column one to ensure that the position information is properly referenced.

1.5.7 Ribbon Advance Components

The ribbon advance components consist of a ribbon cassette and ribbon drive motor. Both components are mounted on the shuttle mechanism and move together with the print head. The ribbon drive motor is energized only during printing and paper motion operations.

1.5.8 Paper Feed Components

The paper feed system consists of a paper feed stepping motor, paper feed drive belt, and tractor drive assembly. Driving power is supplied by the paper feed stepping motor, and coupled by the paper feed drive belt and tractor drive shaft to the tractors. The two tractors, located at either side and

GENERAL DESCRIPTION

above the print station, move the paper vertically past the print head. A tensioning device, located below the print station, holds the form flat against the platen.

1.5.9 Control Panel

The control panel, located at the right front of the printer, contains all electronic controls and indicators necessary to operate the printer, with the exception of the main power switch/indicator. A ribbon cable connects the control panel to the printer control electronics, via the Mother Board CCA (A7).

1.6 SPECIFICATIONS

Table 1-1 summarizes the printer specifications.

TABLE 1-1. SPECIFICATION SUMMARY

Item	Specification	Remarks
<u>Input Power Requirement</u>		
Domestic:	98 to 127 VAC, 60 \pm 1 Hz single phase	
Universal:	90 to 136 VAC or 187 to 257 VAC 50 or 60 Hz, \pm 1 Hz single phase	
<u>Power Consumption</u>		
Idle:	150 watts maximum	
Printing:	275 watts maximum	
<u>Temperature</u>		
Operating:	10°C to 38°C (50°F to 100°F)	
Storage:	-10°C to 50°C (14°F to 122°F)	
Transit:	-40°C to 71°C (-40°F to 160°F)	

GENERAL DESCRIPTION

TABLE 1-1. SPECIFICATION SUMMARY (Contd)

Item	Specification	Remarks
<u>Humidity</u>		
Operating:	20% to 80%	Non-condensing
Storage:	10% to 90%	10% per hour rate of change
Transit:	98% maximum	10% per hour rate of change
<u>Printer Dimensions</u>		
Height		
Cover Closed:	21.3 cm (8.38 inches)	
Cover Open:	57.1 cm (22.48 inches)	
Width:	67.1 cm (26.4 inches)	
Depth:	59.4 cm (23.38 inches)	
Power cord length:	4 meters (13.12 ft)	
<u>Printer Weight</u>		
Net:	30 Kg (67 lbs)	
Shipping:	37.2 Kg (82 lbs)	
<u>Print Characteristics:</u>		
Character Rate:	340 characters per second nominal	
Print Method:	Dot matrix, 7 horizontal by 7 vertical	

TABLE 1-1. SPECIFICATION SUMMARY (Contd)

Item	Specification	Remarks
Printable Columns:	132 columns maximum @ 10CPI	
Pitch (Horizontal Spacing)		
Standard:	10 characters per 25.4 mm (1 inch)	
Condensed:	16.7 characters per 25.4 mm (1 inch)	
Expanded:	5 characters per 25.4 mm (1 inch)	
<u>Interfaces</u>		
Standard:	DPC Short Line Parallel (maximum I/F cable length of 15 meters)	
Options:	a. DPC Long Line Parallel (maximum I/F cable length of 150 meters) b. Serial c. DPC Centronics-compatible	
<u>Line Spacing</u>		
Standard:	6 lines per 25.4 mm (1 inch)	
Optional:	8 lines per 25.4 mm (1 inch)	
<u>Paper Feed</u>		
Step:	50 milliseconds max.	Single line advance
Slew:	254 mm (10 inches)/second	Minimum slew rate

GENERAL DESCRIPTION

TABLE 1-1. SPECIFICATION SUMMARY (Contd)

Item	Specification	Remarks
<u>Throughput</u>		
Full Line:	125 lines per minute	132 characters
Short Line:	300 lines per minute	≤ 40 characters
<u>Format Control</u>		
Coded on the Data Lines:	Line Feed (LF), Form Feed (FF), Carriage Return (CR)	Standard
PI Controlled:	TCVFU, DAVFU	Optional
<u>Paper Form Requirements</u>		
Width:	Standard fan-folded, edge-punched	
	7.62 cm to 40.64 cm (3 inches to 16 inches) overall	
Length:	The basic machine accommodates a 27.94 cm (11 inches) fixed form length	
	A 30.48 cm (12 inch) is available as an option	Requires use of option plug
	Printers equipped with an optional forms length selector switch can accommodate 11 different forms lengths ranging from 7.62 cm (3 inches) to 35.56 cm (14 inches)	
	Printers equipped with the optional TCVFU can accommodate forms lengths of up to 61 cm (24 inches) at 6 LPI, and up to 45.72 cm (18 inches) at 8 LPI	Requires use of option plug

TABLE 1-1. SPECIFICATION SUMMARY (Contd)

Item	Specification	Remarks
Weight	Printers equipped with the DAVFU option can accommodate forms lengths of up to 107 cm (42 inches) at 6 LPI, and up to 76.2 cm (30 inches) at 8 LPI. 38 g/m (10 pound) minimum	Requires use of option plug
Thickness	0.71 mm (0.28 inch) maximum	
Environmental	16°C (60°F), at a relative humidity of 40% to 60%	Recommended operating and storage of forms for best printing.
<u>Ribbon Selection Guide</u>	Fabric ribbon impregnated with non-fading ink, 12.7 mm (1/2 inch) by 36 meters (120 feet), continuous loop cassette	Specifically qualified for matrix printing

1.7 PRINTABLE FORMS

The printer is capable of printing on forms with as many as six parts. The duplicate parts may be printed on either carbonless paper or single shot carbon paper. Other multi-part forms may be used but should be tested under user operating conditions to verify proper paper handling and printout legibility. The recommended storage environment of the paper forms is 60°F (42°C) to 80°F (62°C) at about 40% to 60% relative humidity.

Table 1-2 lists the recommended form thickness and paper weights. Lower paper weight forms may be used in all cases as long as the paper weight is above 10 pounds (37 grams per square meter) for any individual part.

The first column of table 1-2 is labeled "No of Parts", and the numbers 1 through 6 represent the number of parts to a form. The "Form Part Location" heading is divided into six columns, each column corresponding to the page number of a multiple part form. Form Part Location column 1 represents the first part, or original copy, and is the copy closest to the print head after the form has been inserted into the printer and is ready for print.

GENERAL DESCRIPTION

The figures in each of the six Form Part Location columns are suggested paper weights for each form part, expressed in pounds and grams per square meter (gsm). Suggested total form thickness is given in inches and millimeters.

Example: For a carbonless three part paper form, table 1-2 suggests the following weights:

Part 1 (in Form Part Location column 1) - 20 (75)
 Part 2 (in Form Part Location column 2) - 15 (56)
 Part 3 (in Form Part Location column 3) - 100 (63)*

* The 100 (163) gsm is the weight for tab card stock, based upon paper dimensions of 24" x 36" per 500 sheets. All other weight values are based on paper dimensions of 17" x 22" per 500 sheets. The total thickness of all three example parts should be 0.014 inch (0.36 millimeter), as shown in the "Form Thickness" column of table 1-2.

NOTE

The heaviest weight form part should be the last page of a multiple part form located farthest from the print head when the form is inserted into the printer.

TABLE 1-2. PRINTABLE FORMS

Carbonless Paper

No. of Parts	Form Part Location						Form Thickness	
	1	2	3	4	5	6	Inches	Millimeters
1	100(163)						.0070	.17
2	20(75)	100(163)					.0110	.28
3	20(75)	15(56)	100(163)				.0140	.36
4	15(56)	15(56)	15(56)	100(163)			.0175	.44
5	15(56)	15(56)	15(56)	15(56)	20(75)		.0170	.43
6	15(56)	12(45)	12(45)	12(45)	12(45)	20(75)	.0185	.47

TABLE 1-2. PRINTABLE FORMS (Contd)

Carbon Paper

Using 8 lb (19 gsm) Single Shot Carbon

No. of Parts	Form Part Location						Form Thickness	
	1	2	3	4	5		Inches	Millimeters
1	100(163)						.0070	.17
2	20(75)	100(163)					.0130	.33
3	20(75)	15(56)					.0180	.33
4	15(56)	15(56)	15(56)	100(163)			.0240	.61
5	15(56)	15(56)	15(56)	15(56)			.0220	.56
6	15(56)	12(45)	12(45)	12(45)	20(75)		.0240	.61

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SECTION II

PREPARATION FOR USE

2.1 INTRODUCTION

This section contains information necessary to prepare the printer for use. Included are space requirements, unpacking procedures, mounting procedures, power connection and conversion procedures, and interface connection procedures.

2.2 SPACE REQUIREMENTS

Figure 2-1 is an outline drawing of the printer dimensions. Prior to unpacking, select a flat surface with suitable dimensions on which the printer can be placed for operation. Allow sufficient clearance for the printed paper to exit freely from the printer and into a designated printed forms receiver. In addition, allow a minimum of 7.6 cm for ventilation clearance on the right side of the printer per figure 2-1. Outline dimensions for the printer equipped with the optional paper receptacle are illustrated in figure 2-2.

2.3 UNPACKING THE PRINTER

The printer is shipped in a reusable cardboard container, and held in place by molded polystyrene end caps. Included in the container, but packaged separately, is the shipaway kit containing an interface connector, fifty contact pins, a cable clamp kit, the printer Operators Guide and Maintenance Guide, a ribbon cassette, and a print sample.

The procedure for unpacking the printer is as follows:

- a. Open the shipping container and remove the printer. Save the container and packing material for possible future use.

WARNING

Two or more persons may be required to lift the printer onto the mounting surface because of its weight of 67 lbs (30 kg).

- b. Remove all wrapping material from the printer and place it on the mounting surface. The procedure for securing the printer to the optional pedestal is given in paragraph 2.4.
- c. Remove the shipaway kit from the shipping container.
- d. Check the contents of the container against the packing slip attached to the outside of the container.

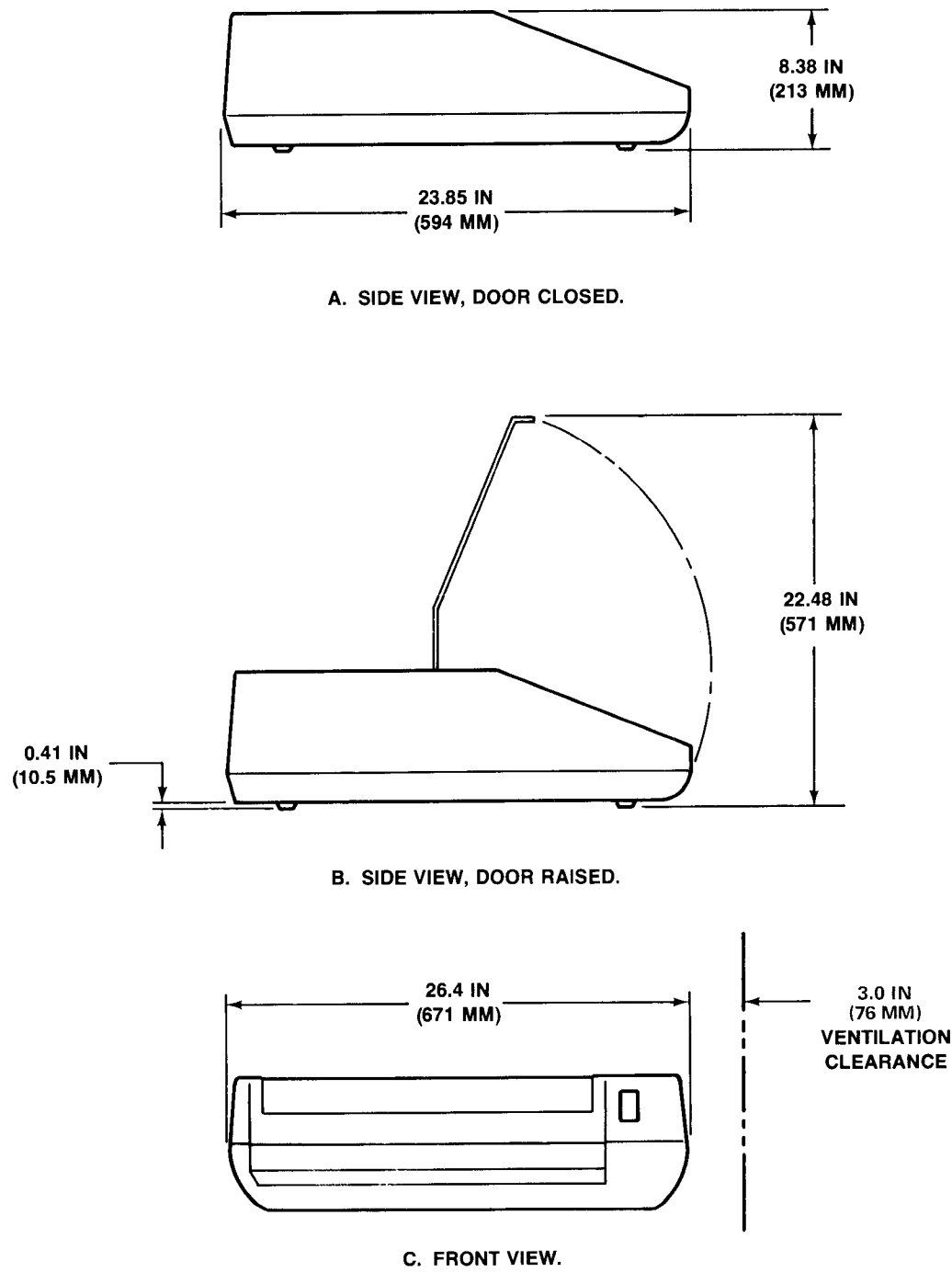


Figure 2-1. Standard Printer Outline Dimensions

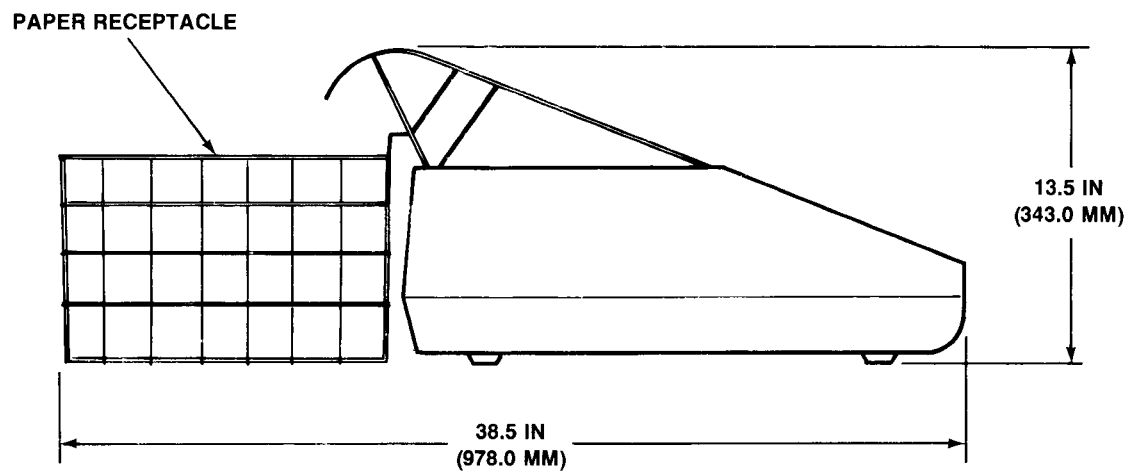
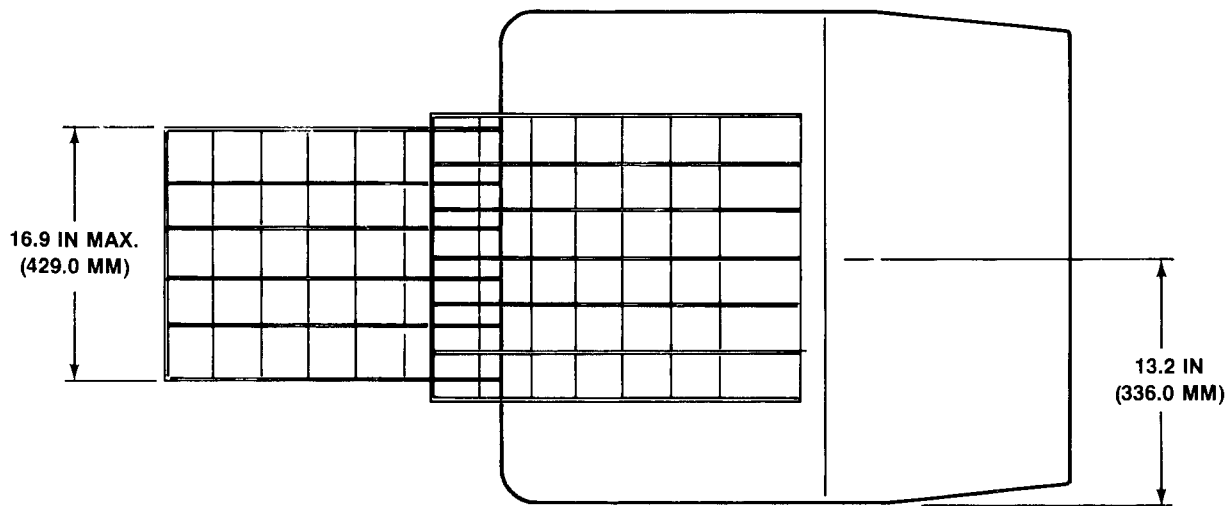


Figure 2-2. Printer with Optional Paper Receptacle, Outline Dimensions

PREPARATION FOR USE

e. Raise the door and remove the two plastic cable ties and the plastic foam block from the shuttle/print head assembly. Save the foam block for possible reshipment.

f. Verify that the shuttle/print head assembly moves freely back and forth on the shuttle rail.

2.4 PRINTER MOUNTING PROCEDURES

The printer may be mounted either to any flat surface which is capable of supporting its weight, or to an optional pedestal when space requirements dictate a floor mount arrangement.

2.4.1 Optional Pedestal Mounting

Perform the following procedure to mount the printer onto the optional pedestal:

a. Assemble the pedestal per figure 2-3, using the parts supplied in the pedestal kit. To do this, secure each side of the center bracket to one of the pedestal legs with two buttonhead screws. Next, place two threaded inserts within the bottom of each pedestal leg, screw an adjustment glide into each insert, and then install the shelf.

b. Referring to figure 2-4, position the printer on top of the pedestal and secure with six screws and applicable washers.

c. Adjust the four glides on the pedestal legs until the printer is level.

2.5 INITIAL POWER CONNECTION

Perform the following procedure to connect power to the printer:

a. Verify that the power cord, plug, and fuse supplied with printer match the specified power indicated on the nameplate located on the back of the printer.

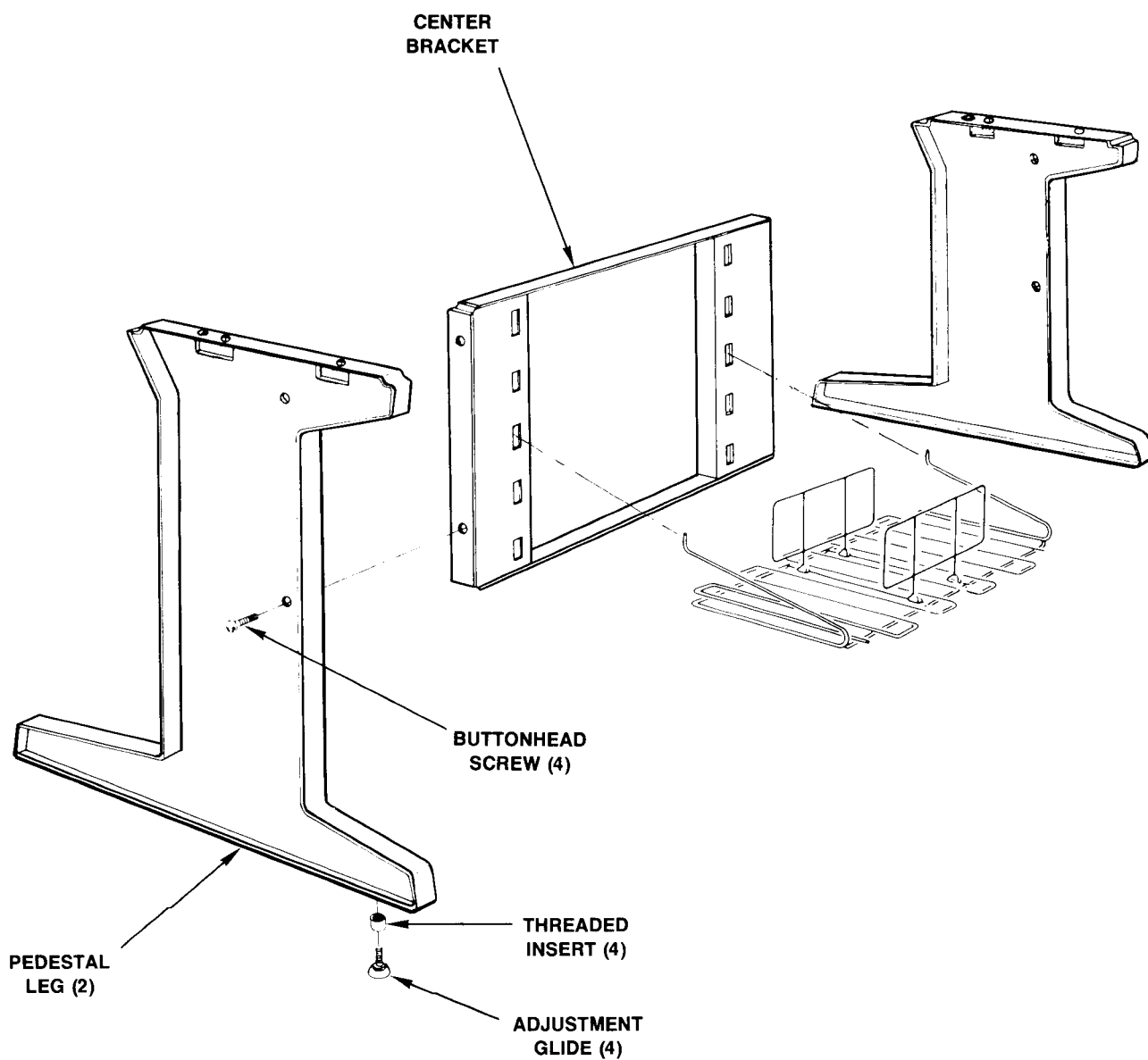
c. Plug the printer power cord into the available power outlet.

d. Set the POWER switch, located at the lower left front of the printer, to the ON position.

2.6 POWER CONVERSION FOR OPTIONAL UNIVERSAL POWER SUPPLY

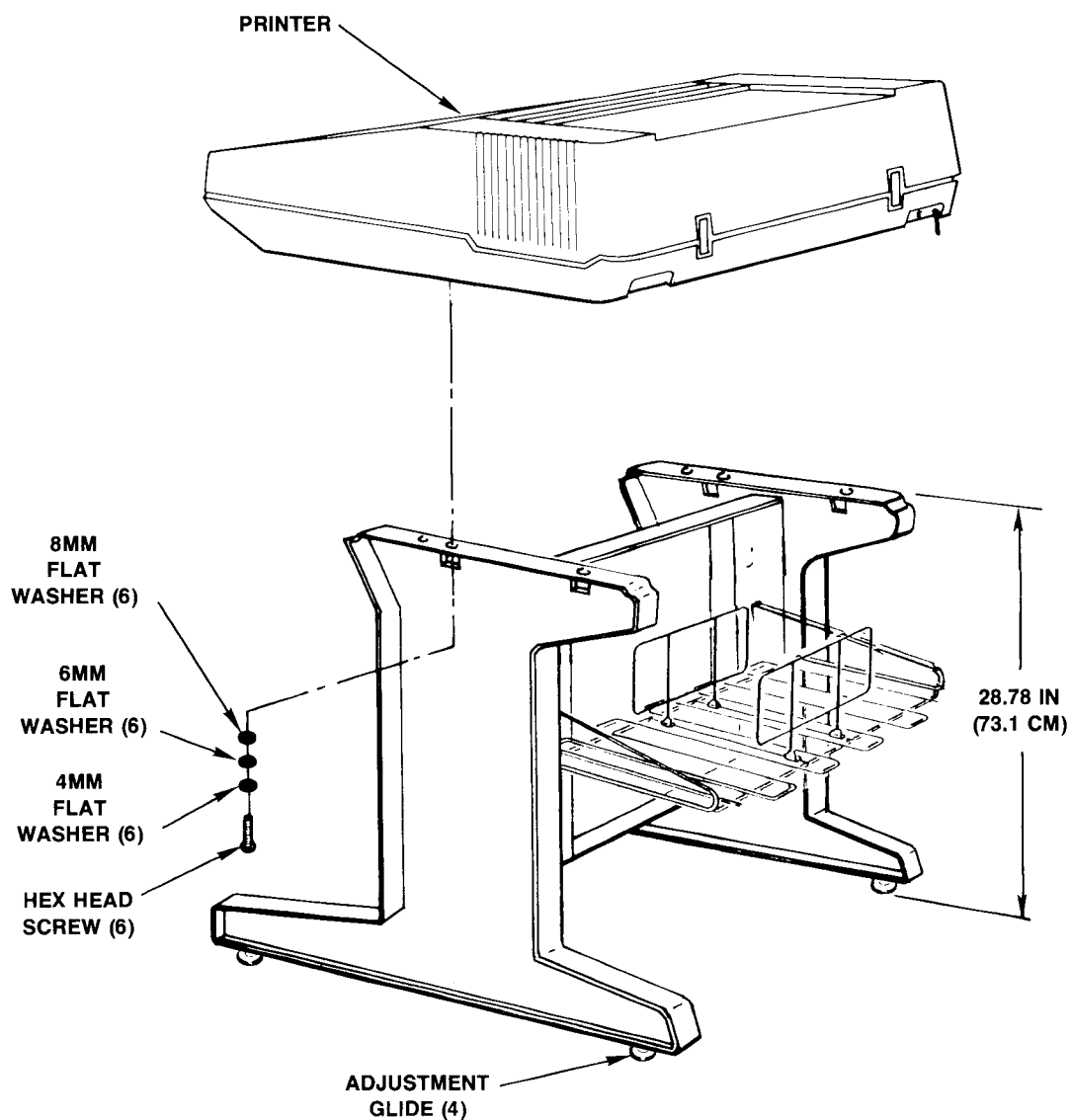
Printers equipped with the optional universal power supply have the capability of operating on one of the following power options:

- a. 90 to 140 VAC, 50 Hz ± 1 Hz
- b. 90 to 140 VAC, 60 Hz ± 1 Hz
- c. 187 to 257 VAC, 50 Hz ± 1 Hz
- d. 187 to 257 VAC, 60 Hz ± 1 Hz



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Figure 2-3. Pedestal Assembly



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Figure 2-4. Pedestal Installation

2.6.1 Power Plugs

The universal power supply is configured at the factory to user specifications. Printers configured at the factory for 90-140 VAC operation are equipped with a power cord terminated in a molded power plug that fits into a standard 3-terminal 115 VAC domestic power outlet. Printers configured at the factory for 187-257 VAC operation are terminated in a standard three-prong 250 VAC domestic power plug.

When changing from 90-140 VAC operation to 187-257 VAC operation, replace the existing power plug with a 250 VAC domestic power plug, Part Number DPC 800827-002. Wiring information shown in figure 2-5. When changing from 187-257 VAC operation to 90-140 VAC operation, replace the existing power plug with a 125 VAC domestic power plug, DPC Part Number 800827-004. When changing to foreign power, replace the existing power plug with one that fits into the applicable foreign power outlet.

2.6.2 Labels

Printers equipped with a universal power supply use two labels to show the transformer power configuration and required fuse size. These labels are located at the rear of the printer as shown in figure 2-6. When changing voltage, or voltage and frequency, both the voltage/frequency label and the fuse label must be replaced. When changing frequency only, only the voltage/frequency label must be replaced.

2.6.3 Optional 115 VAC/60 Hz

WARNING

Do not attempt to perform any power conversion procedure with the power cord connected.

Disconnect from TB2 the color-coded wires listed in table 2-1, and reconnect them as shown in the 115/VAC 60 Hz column of table 2-1. Replace fuse F1 with 3A slo-blo fuse, and the two labels as appropriate.

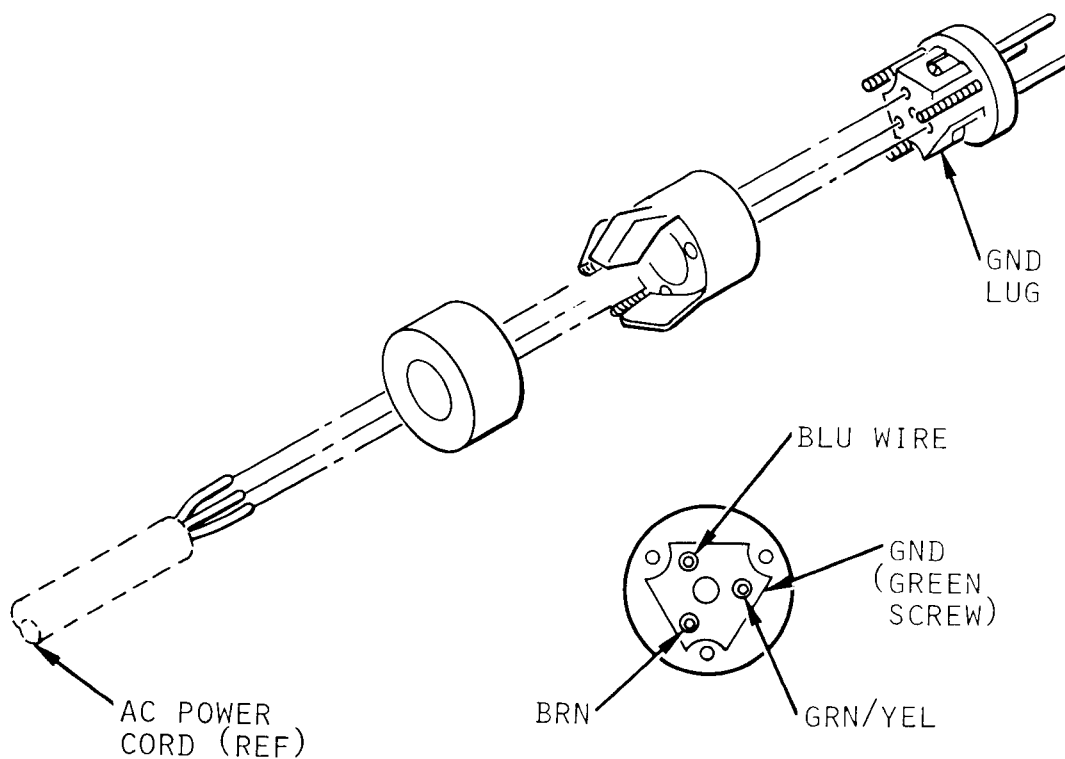
2.6.4 Optional 115 VAC/50 Hz

WARNING

Do not attempt to perform any power conversion procedure with the power cord connected.

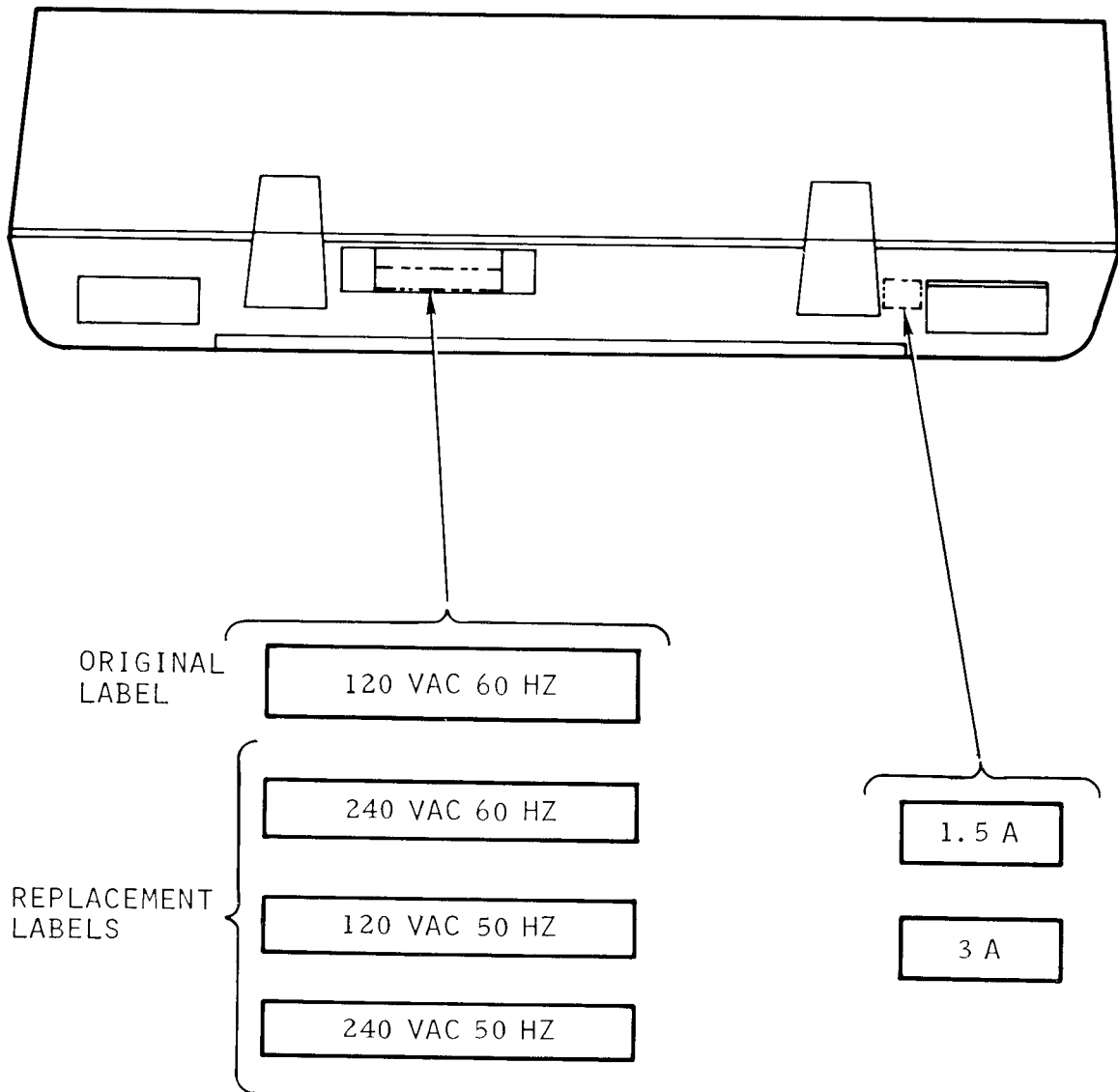
Disconnect from TB2 the color-coded wires listed in table 2-1, and reconnect them as shown in the 115 VAC/50 Hz column of table 2-1. Replace fuse F1 with 3A slo-blo fuse, and the two labels as appropriate.

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Figure 2-5. 250V Power Plug Wiring Details



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Figure 2-6. Power and Fuse Labels

PREPARATION FOR USE

The printer equipped with the universal power supply is configured to operate at one of the POWER options described above, as specified by the user. If the universal power supply should require reconfiguration, refer to table 2-1 and figure 2-7, and perform the following procedure:

WARNING

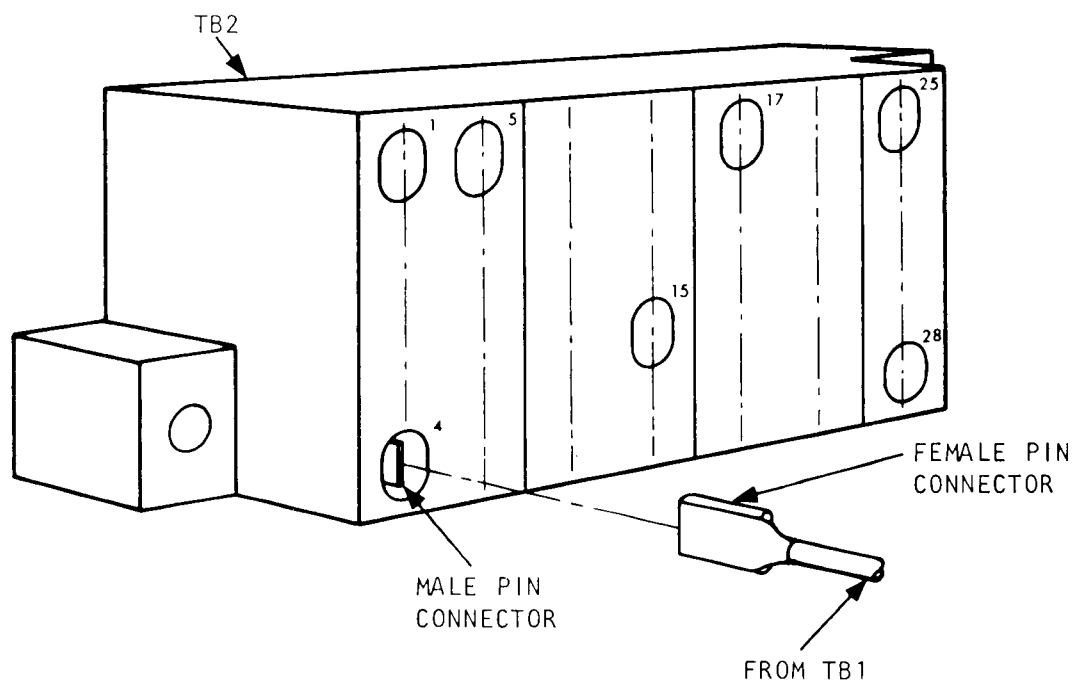
Disconnect the power cord from the power outlet. Do not make any power configuration changes with the power cord connected to the power outlet, as injury to personnel may occur.

NOTE

To reconfigure the universal power supply from one power option to another, wires on TB2, C4, and the base terminals must be relocated. Note that the listed color-coded wires shown in table 2-1 may be connected at any one of several possible locations.

TABLE 2-1. OPTIONAL UNIVERSAL POWER SUPPLY TB2, C4, AND BASE TERMINAL WIRE CONFIGURATION

Wire Color	TB2 Pin Position Number			
	115 VAC 60 Hz	115 VAC 50 Hz	250 VAC 60 Hz	250 VAC 50-Hz
Red	8	8	16	16
Green/Yellow	6	10	6	10
Green/White	9	6	9	6
Brown	3	3	7	7
Brown/Yellow	7	14	12	14
Brown/White	13	7	13	12
White/Orange	27	26	27	26
White	23	24	23	24
Violet/White	22	21	22	21
* Red/White	Base Term	C4	Base Term	C4
* Red/Black	C4	Base Term	C4	Base Term
* Wires not located on TB2				



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Figure 2-7. Power Terminal Block TB2

PREPARATION FOR USE

2.6.5 Optional 250 VAC/60 Hz

WARNING

Do not attempt to perform any power conversion procedure with the power cord connected.

Disconnect from TB2 the color-coded wires listed in table 2-1, and reconnect them as shown in the 250 VAC/60 Hz column of table 2-1. Replace fuse F1 with 1.5A slo-blo fuse, and the two labels as appropriate.

2.6.6 Optional 250 VAC/50 Hz

WARNING

Do not attempt to perform any power conversion procedure with the power cord connected.

Disconnect from TB2 the color-coded wires listed in table 2-1, and reconnect them as shown in the 250 VAC/50 Hz column of table 2-1. Replace fuse F1 with a 1.5A slo blo fuse, and the two labels as appropriate.

2.7 PRINTER/USER SYSTEM INTERFACE PREPARATION

The printer interfaces with the user system via an interface cable. The standard interface connector on the printer is a 50-pin AMP that mates with cable connector AMP Part No. 66506-9 (not supplied) on the interface cable. Pin assignments are listed in table 2-2.

There are three optional cables available, used with the following connectors:

NOTE

The adapter cable is not an interface cable. It mates an interface cable with a non-standard connector to the standard interface connector on the printer.

- a. 50-pin Winchester Connector, used with a DPC Parallel Interface.
- b. 25-pin connector, used with a serial interface.
- c. 36-pin connector, used with a DPC Centronics-compatible interface.

Pin assignments for the optional connectors are described in section VI.

Referring to table 2-2 (or section VI if an optional adapter cable is used), proceed as follows:

a. Build up the cable strands into one main cable harness. Be sure that the cable length does not exceed 15 meters (150 meters if the optional long-line parallel interface is used).

b. Crimp the pins supplied in the skipaway kit onto the base ends of the wire strands, then install the cable leads within the appropriate cable connector, pin by pin, per table 2-2.

c. Using a multimeter, measure the continuity from each end of the cable, pin by pin, per table 2-2.

d. Connect one end of the interface cable to the printer interface connector, and the other to the user's system.

TABLE 2-2. STANDARD DATAPRODUCTS 50-PIN AMP,
PARALLEL SHORT LINE CABLE CONNECTOR
PIN ASSIGNMENTS

Pin	Signal	Definition
22	READY (Twisted Pair)	A printer-generated signal which indicates that the printer is ready to be put on line. When READY is true, the following are true: <ul style="list-style-type: none"> a. Power and DC voltages are on. b. All interlocks are closed. c. Paper has been loaded. d. No printer fault exists. e. SELF TEST is not selected.
6	READY RTN	

PREPARATION FOR USE

TABLE 2-2. STANDARD DATA PRODUCTS 50-PIN AMP
PARALLEL SHORT LINE CABLE CONNECTOR
PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
21	ON LINE (Twisted Pair)	A printer-generated signal which indicates that the printer has been put on line. When ON LINE is true, the following are true: <ul style="list-style-type: none"> a. The ALARM light is off. b. The printer operator has pressed the ON LINE switch. c. The printer is ready to accept data from the user. d. SELF TEST is not selected.
5	ON LINE RTN	
23	DEMAND (Twisted Pair)	A printer-generated signal which synchronizes data transmission between the printer and the user system. The DEMAND LINE signal requests a character from the user and remains active until the DATA STROBE is received. It is disabled while the character is being stored in memory and during the print operation. DEMAND LINE will never be active unless ON LINE is active.
7	demand RTN	The user must follow handshaking timing procedures described in section IV.
19	DATA 1 (Twisted Pair)	User Data.
3	DATA 1 RTN	
20	DATA 2 (Twisted Pair)	User Data.
4	DATA 2 RTN	
1	DATA 3 (Twisted Pair)	User Data.
2	DATA 3 RTN	

TABLE 2-2. STANDARD DATA PRODUCTS 50-PIN AMP
PARALLEL SHORT LINE CABLE CONNECTOR
PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
41	DATA 4 (Twisted Pair)	User Data.
40	DATA 4 RTN	
34	DATA 5 (Twisted Pair)	
18	DATA 5 RTN	
43	DATA 6 (Twisted Pair)	User Data.
42	DATA 6 RTN	
36	DATA 7 (Twisted Pair)	User Data.
35	DATA 7 RTN	
28	DATA 8 (Twisted Pair)	User Data.
44	DATA 8 RTN	
46	INTERFACE IN (Twisted Pair)	Two interface connector pins are jumpered together to allow the user to verify that the interface connector is plugged into the printer.
45	INTERFACE OUT	

PREPARATION FOR USE

TABLE 2-2. STANDARD DATAPRODUCTS 50-PIN AMP
PARALLEL SHORT LINE CABLE CONNECTOR
PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
38	STROBE (Twisted Pair)	A user-generated signal which defines when information on data lines is stable and may be stored in the printer buffer. Each time a DATA STROBE occurs, the printer samples the data lines.
37	STROBE RTN	After the data lines have been sampled, the DEMAND LINE signal will go inactive. Once a format control character has been transferred to the printer, the DEMAND LINE will remain inactive until printing is complete. Handshaking for the format control character and for print data is identical. The user must follow the handshaking timing procedures described in section IV.
31	BUFFER CLEAR* LOADED. (Twisted Pair)	This user-generated signal, when active, will clear the printer buffer and allow a new line of data to be loaded. <div>NOTE BUFFER CLEAR* is treated like data; it will be sampled only when the DEMAND LINE signal is active. If the PARITY ERROR option is installed, the BUFFER CLEAR* signal will reset the PARITY ERROR signal.</div>
15	BUFFER CLEAR RTN	
12	+5 VOLTS	
39	GND	
27	PARITY ERROR (Twisted Pair)	Option (See section VI)
11	PARITY ERROR RTN	

TABLE 2-2. STANDARD DATAPRODUCTS 50-PIN AMP
PARALLEL SHORT LINE CABLE CONNECTOR
PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
25	BOTTOM OF FORM (Twisted Pair)	Option (See section VI)
9	BOTTOM OF FORM RTN	
26	PAPER MOVING (Twisted Pair)	Option (See section VI)
10	PAPER MOVING RTN	
24	TOP OF FORM (Twisted Pair)	Option (See section VI)
8	TOP OF FORM RTN	
29	PARITY BIT (Twisted Pair)	Option (See section VI)
13	PARITY BIT RTN	
30	PAPER INSTRUC- TION (Twisted Pair)	Option (See section VI)
14	PAPER INSTRUC- TION RTN	

[illegible]

SECTION III

OPERATOR INSTRUCTIONS

3.1 INTRODUCTION

This section contains information necessary to the operation of the printer, and includes the following topics:

- a. Operator Controls and Indicators
- b. Preliminary Procedures
- c. Operating Procedures
- d. Operator Care

3.2 OPERATOR CONTROLS AND INDICATORS

Operator controls and indicators are illustrated in figures 3-1 through 3-3 and described in tables 3-1 through 3-3.

3.3 PRELIMINARY PROCEDURES

Prior to operation of the printer, one or more of the following procedures, as applicable, must be performed by the operator.

TABLE 3-1. ELECTRICAL CONTROLS AND INDICATORS

Figure & Index No.	Item	Function
3-1 1	ON LINE switch/indicator	Indicator illuminates when printer is on line. Pressing the switch will alternately place the printer on line and off line.
2	ALARM/CLEAR switch/indicator	ALARM indicator illuminates when a fault condition exists. Pressing the CLEAR switch clears the printer logic.
3	TOP OF FORM switch	Momentary action switch. When pressed, advances paper to the top of the next form. When pressed and held, paper will advance continually. Not effective when printer is on line.

TABLE 3-1. ELECTRICAL CONTROLS AND INDICATORS (Contd)

Figure & Item No.	Item	Function
4	PAPER STEP switch	Momentary action switch. When actuated, advances paper a single line. When pressed and held, paper will advance continually. Not effective when printer is on line.
5	TEST switch	When set to ON, allows operator to exercise printer without an external data source. Effective only when printer is on line.
6	POWER switch	Applies primary AC power to the printer.
7	PITCH switch (optional)	This two-position switch allows the operator to select the standard horizontal spacing of 10 characters per inch or the condensed spacing of 16.7 characters per inch.
8	LPI switch	This two-position switch allows the operator to select 6 or 8 lines per inch vertical line spacing. The standard line spacing is 6 lines per inch.
9	FORM LENGTH switch (optional)	Allows operator to select 11 different forms lengths.
10	STATUS indicator (optional)	Two-digit numerical display. When a malfunction occurs, the number displayed corresponds to the last function performed by the printer.

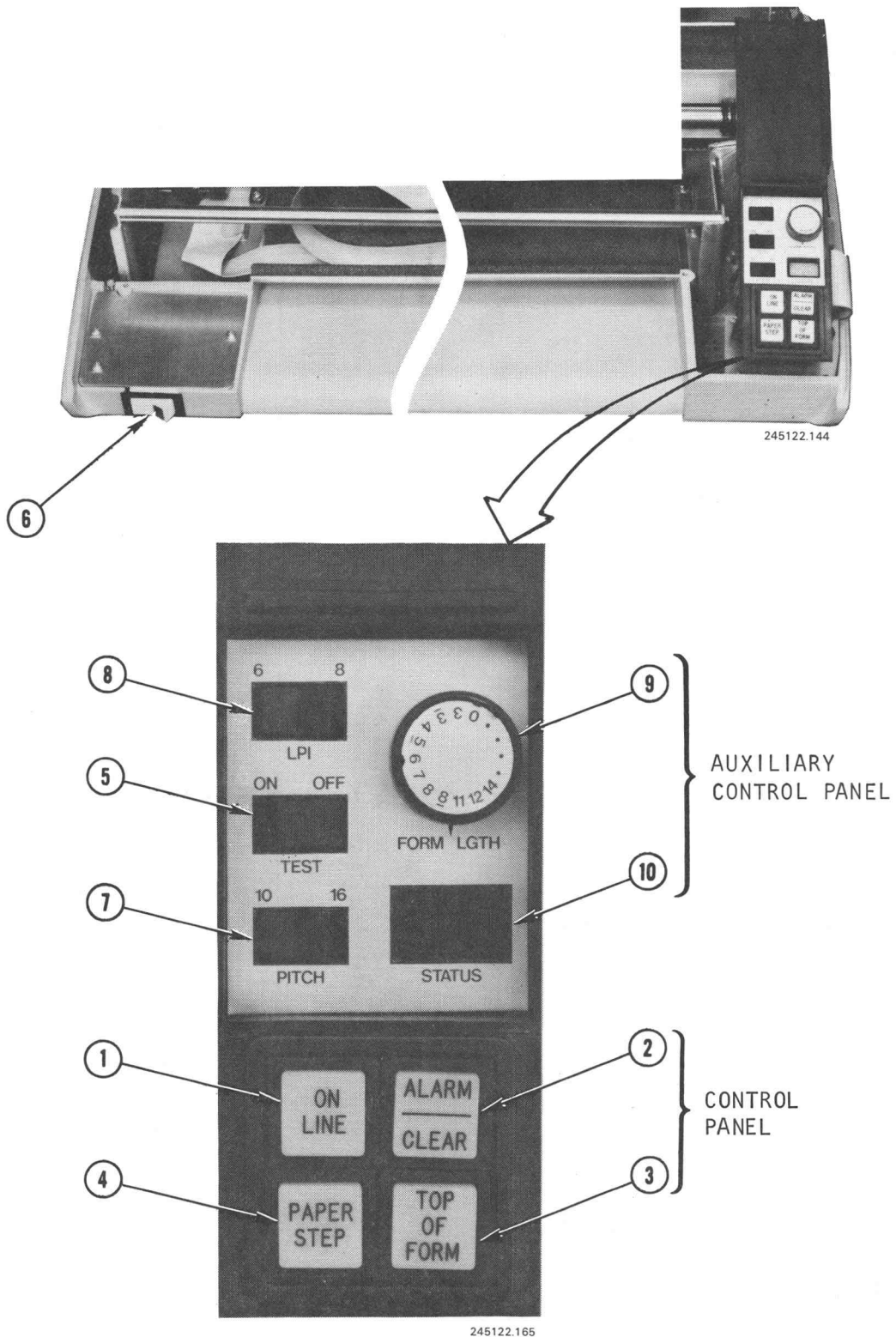


Figure 3-1. Controls, Connectors, and Indicators

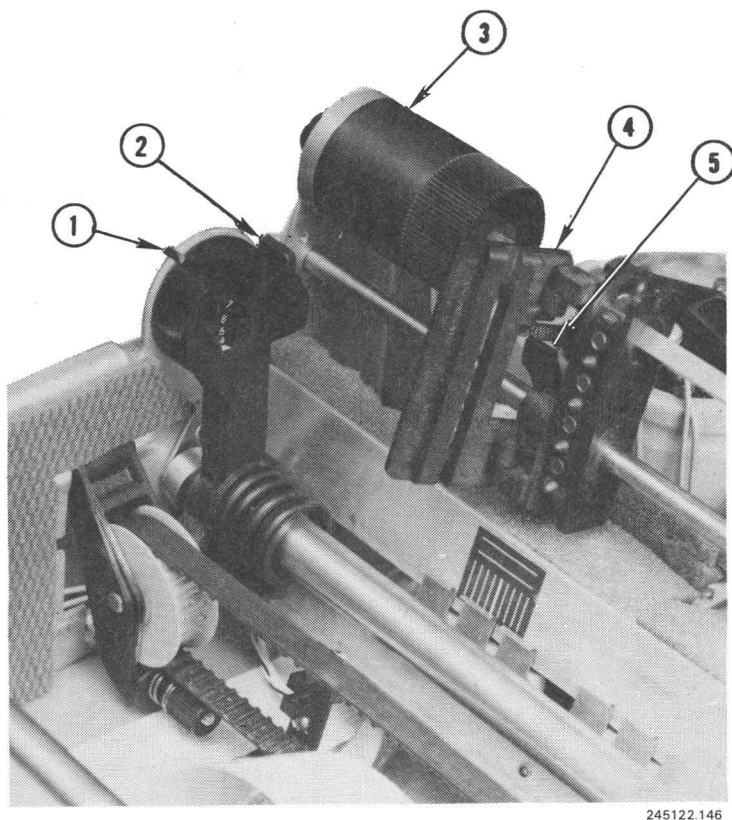


Figure 3-2. Mechanical Controls

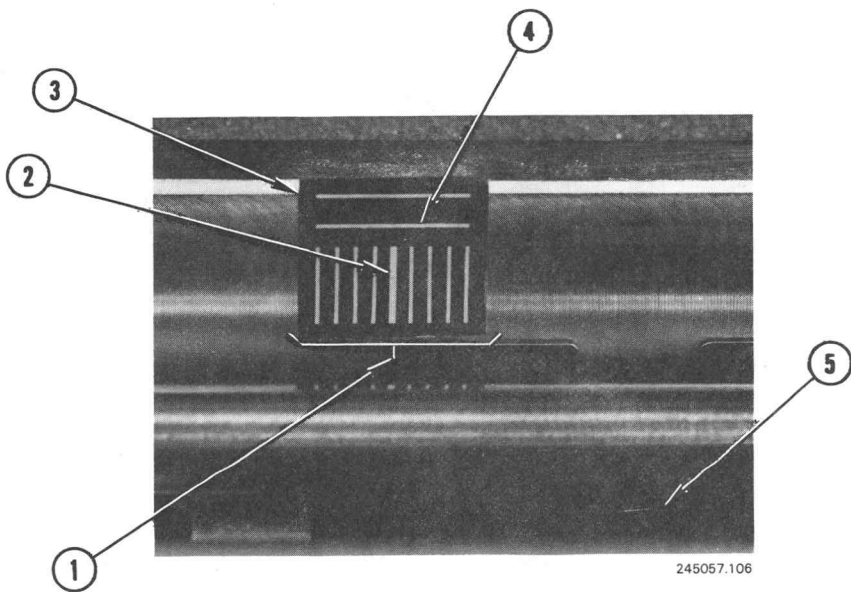


Figure 3-3. Miscellaneous Controls

TABLE 3-2. MECHANICAL CONTROLS

Figure & Index No.	Item	Function
3-2 1	Forms thickness control	Moving this lever controls the platen gap, thus allowing printing of forms from one to six parts.
2	Platen gap lever	Moving this lever away from the platen releases the paper tensioner and increases the distance between the print head and the platen to facilitate paper loading, ribbon replacement, and print head replacement.
3	Vertical adjust	While applying a downward pressure, this knob may be rotated and the paper manually moved to achieve a vertical paper registration.
4	Pressure plate	The pressure plates may be opened and closed to allow the loading of paper.
5	Tractor locks	Rotating the tractor locks downward allows the tractor to be moved horizontally to achieve a horizontal paper alignment or to accomodate various paper widths.

TABLE 3-3. MISCELLANEOUS OPERATOR CONTROLS

Figure & Index No.	Item	Function
3-3 1	Forms alignment scale	Allows the operator to visually align paper both vertically and horizontally to get proper print-to-form registration.
2	Horizontal lines	The two horizontal lines represent the line spacing when the printer is printing at six lines per inch. The bottom horizontal line indicates the vertical position of the top of the characters of the print row.
3	Vertical lines	The vertical lines are 1/10 inch apart and indicate horizontal margin.
4	Center heavy line	Placing the edge of the paper directly over the center heavy line will provide a 1/2 inch margin.
5	Paper low interlock switch	Detects the end of the last form. Prevents printer operation when the paper supply is exhausted.

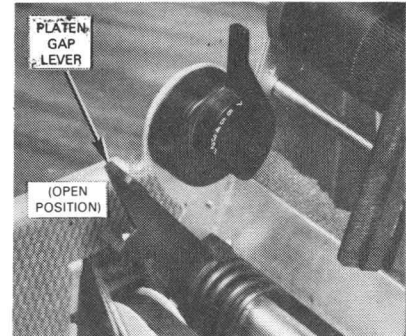
OPERATOR INSTRUCTIONS

3.3.1 Paper Loading

Paper loading may be accomplished with the printer powered up or shut down. However, to achieve vertical registration of the print line to the paper, as well as proper top of form alignment, the printer must be powered up. To load the paper, perform the following procedure:

a. Raise the top cover. Rotate the platen gap lever to its open position (away from the platen).

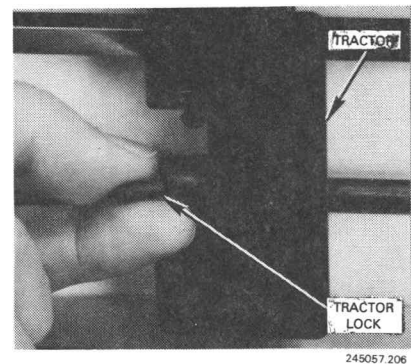
Press the TOP OF FORM switch to set the printer mechanism to the top of form position.



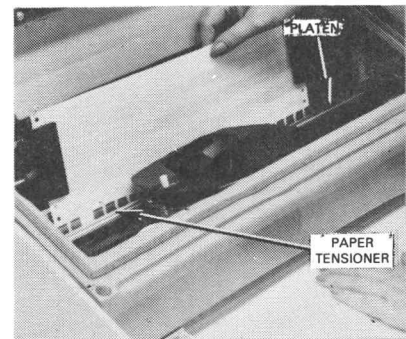
b. Rotate both tractor locks downward (only one shown). Move the tractors to their respective outermost positions.

NOTE

This step is only required if changing to a different width paper or a different margin from that previously used.

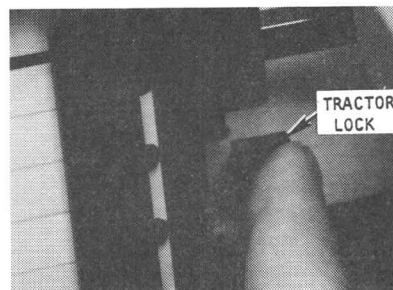


c. Insert paper into the desired paper loading port (the front is shown, although the bottom optional rear port may also be used). Slide the paper up between the platen and the paper tensioner.



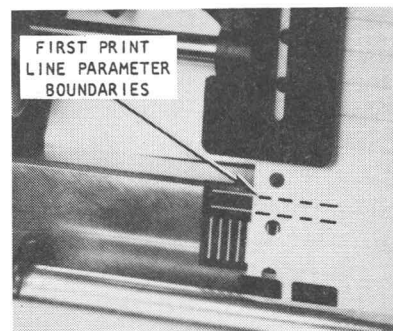
OPERATOR INSTRUCTIONS

h. Close the pressure plate and rotate the tractor lock upward.



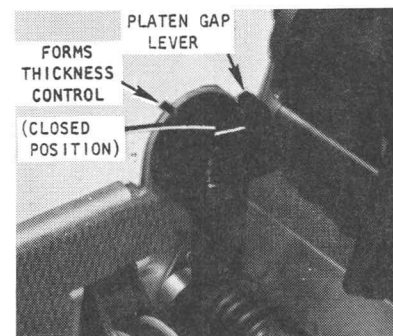
245057.211

i. Rotate the vertical paper adjust knob to vertically position the paper to the desired first print line position. This line will be printed within the parameters of the two horizontal lines of the forms alignment scale.



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j. Rotate the platen gap lever to its closed position (toward the platen) and set the forms thickness control to the number that matches the thickness of the forms being used. Close the top cover.



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k. Press the ALARM/CLEAR switch. The printer may now be placed on line.

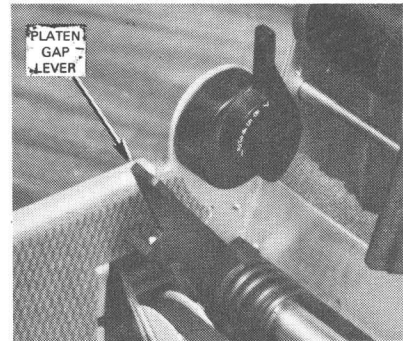


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3.3.2 Ribbon Replacement

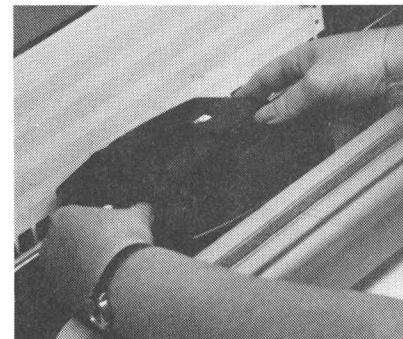
The ribbon used on this printer is a cassette ribbon assembly and may be replaced with the printer powered up or shut down. To replace the ribbon cassette, perform the following procedure:

a. Raise the top cover. Rotate the platen gap lever to its open position (away from the platen).



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b. Lift the ribbon cassette off the print head. Install the new ribbon cassette over the print head. Press down evenly until the cassette snaps into place.

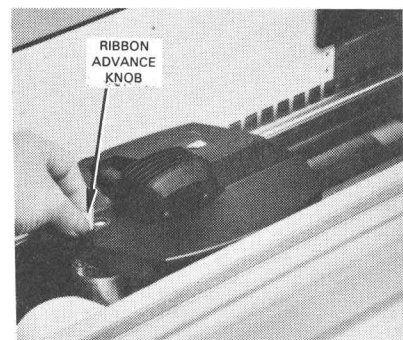


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NOTE

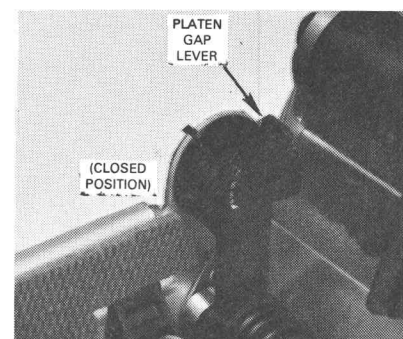
It may be necessary to rotate the ribbon advance knob clockwise while seating the ribbon cassette on the head carriage to ensure that the ribbon drive mechanism meshes properly (see step c).

c. Rotate the ribbon advance knob clockwise to ensure that the ribbon is taut and properly positioned in front of the print head.



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d. Rotate the platen gap lever to its closed position (toward the platen). Close the top cover and press the ALARM/CLEAR switch. If the printer has been powered up and properly loaded with paper, the printer may now be placed on line.



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OPERATOR INSTRUCTIONS

3.3.3 Print Head Replacement

To remove and replace the print head, perform the following procedure:

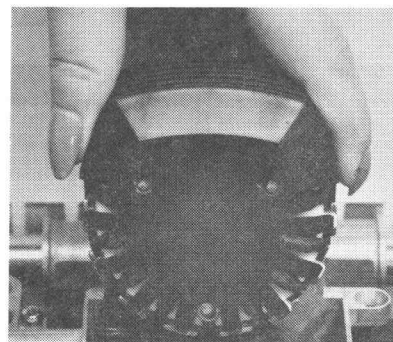
CAUTION

The printer must be shut down prior to head replacement. Allow sufficient time for the print head to cool before proceeding.

Removal

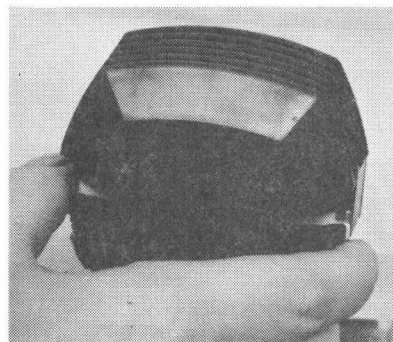
CAUTION

During removal or replacement, the print head must be grasped at the top (not the front) as shown.



RIGHT

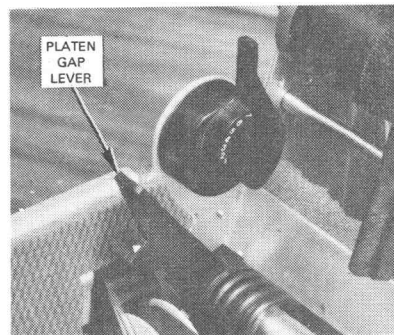
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WRONG

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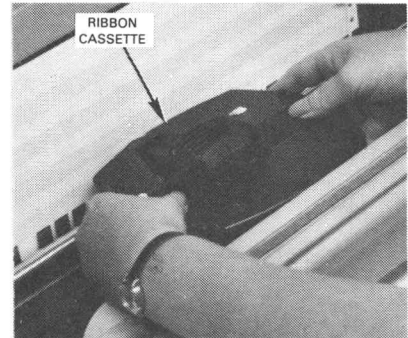
- a. Open the printer cover, Rotate the platen gap lever to its open position (away from the platen).



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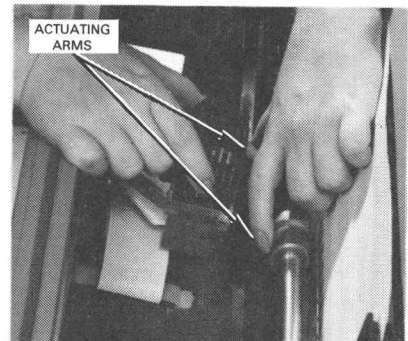
OPERATOR INSTRUCTIONS

b. Remove the ribbon cassette from the print head per paragraph 3.3.2.



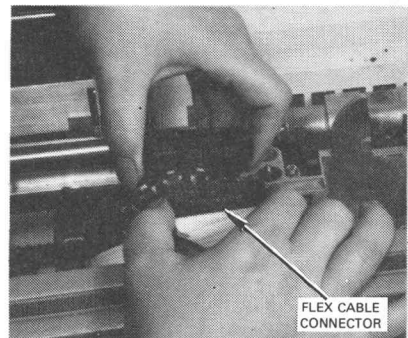
245057A 217

c. To remove the print head: squeeze the print head locking mechanism actuating arms, then pull the print head approximately 3/16 inch toward the front of the printer and lift clear of the shuttle assembly.



245057A 220

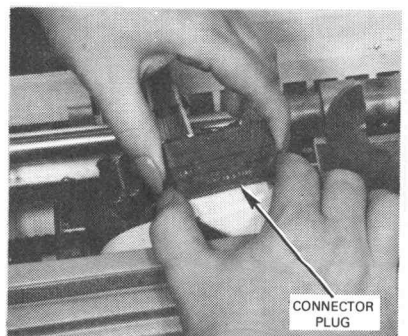
d. Disconnect the print head flex cable connector from the print head per paragraph 5.3.21.



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Replacement

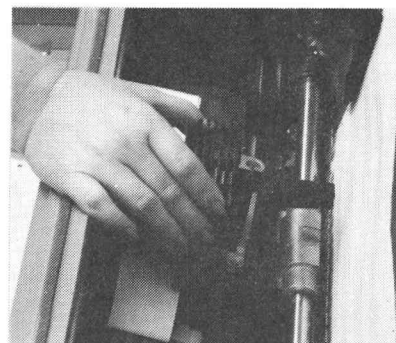
e. To install the new print head, connect the print head flex cable to the new print head per paragraph 5.3.21.



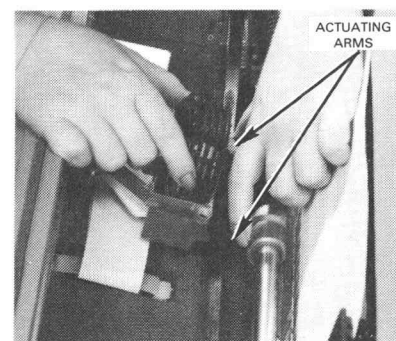
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OPERATOR INSTRUCTIONS

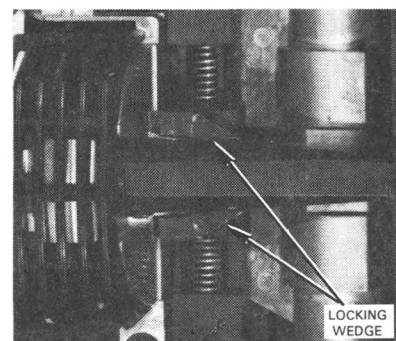
f. Position the new print head over the shuttle mechanism.



g. Squeeze the print head locking mechanism actuating arms together, slide the print head down the shuttle mechanism, push the print head toward the rear of the printer, and remove pressure from the locking mechanism actuating arms.



h. Ensure that the locking wedge is properly seated.



i. Install the ribbon cassette over the print head. Press down evenly until the cassette snaps into place.

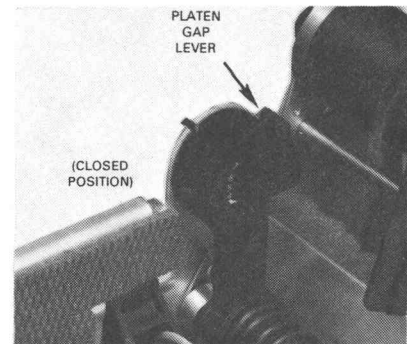


NOTE

It may be necessary to rotate the ribbon advance knob clockwise while seating the ribbon cassette on the print head carriage to ensure that the ribbon drive mechanism meshes properly (see step j).

OPERATOR INSTRUCTIONS

j. Rotate the platen gap lever to its closed position (toward the platen). Close the printer top cover. The printer may now be powered up.



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OPERATOR INSTRUCTIONS

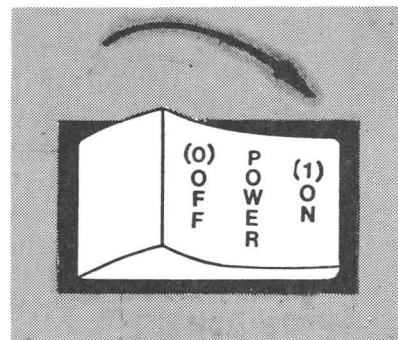
3.4 OPERATING PROCEDURES

Operating procedures include the power-up, shut-down, and self-test procedures.

3.4.1 Power Up

The power up procedure assumes that the printer is properly loaded with paper, the ribbon is properly installed, and all doors and latches are closed. Refer to the applicable procedure in paragraph 3.3.

a. Place the POWER switch to ON.



b. Ensure that the ALARM indicator is extinguished. If it is illuminated, press the CLEAR switch. If the indicator remains illuminated, a fault condition exists.

(If the optional STATUS indicator is installed, refer to section VI to determine if problem can be repaired locally).

c. Perform step e of paragraph 3.4.3.

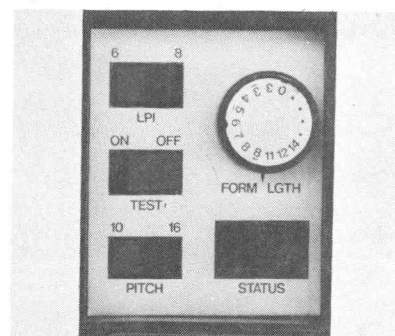


d. Slide open the auxiliary control panel access door and ensure that the TEST switch is set to OFF.

(1) If the optional LPI switch is installed, set it to the desired position.

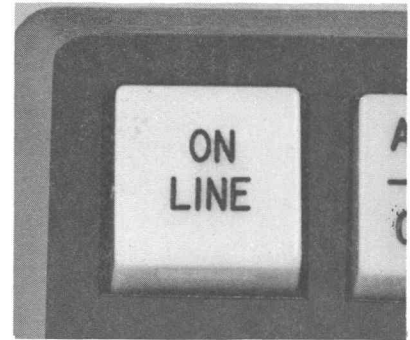
(2) If the optional PITCH switch is installed, set it to the desired position.

(3) If the optional FORM LGTH selector is installed, ensure that the setting corresponds to the form length being used.



(4) Slide the auxiliary control panel access cover closed.

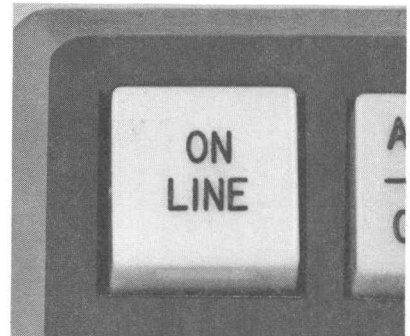
e. To operate the printer, press the ON LINE switch/indicator and verify that it is illuminated.



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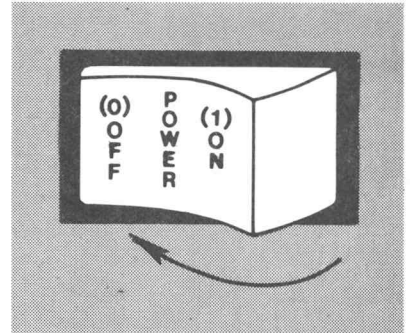
3.4.2 Shut Down

a. If the ON LINE switch/indicator is illuminated, press one time. After completion of the print cycle (current print line) the printer will go off line.



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b. Place the POWER switch OFF.



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3.4.3 Self Test

The printer has a self-test feature which allows the user to determine its operational readiness. To initiate a self test operation, ensure that ribbon and paper are loaded in the printer, then proceed as follows:

- a. Connect the power cord into the service power outlet.
- b. Place the POWER switch to ON.

OPERATOR INSTRUCTIONS

- c. Place the TEST switch to ON.
- d. Momentarily press the ON LINE switch and verify that the ON LINE indicator illuminates. Verify that the printer is printing out a test pattern as shown in figure 3-6. Printout will stop automatically after 264 lines.
- e. To terminate the self test operation in less than 264 lines, place printer in the off-line mode by pressing the ON LINE switch, and verify that the ON LINE indicator goes off.
- f. Disable the self-test mode by placing the TEST switch to the OFF position.

NOTE

If malfunctions occur during a self test operation, refer to section VII for failure analysis.

3.5 OPERATOR CARE

3.5.1 Cleaning

During ribbon/paper loading procedures, inspect the printing area for the presence of ink, lint, or other foreign material. If a build-up of foreign material is evident, remove the ribbon cassette and print head as required, then clean the area with a soft cloth moistened with an approved solvent.

CAUTION

Be careful not to saturate the cloth to the point where solvent can drip into the bearings of the printer.

The recommended cleaning solvent for all sub-assemblies on the printer is isopropyl alcohol. Denatured alcohol and Loctite safety solvent are other cleaning solutions that may be used. NEVER USE tri-chlorethylene, methylethyl-ketone or acetone.

3.5.2 Operator Maintenance Schedule

Although there are no regularly scheduled preventative maintenance procedures, periodically inspect and vacuum the area immediately accessible when raising the top cover. Remove the ribbon cassette prior to vacuuming.

Figure 3-4.

3-17

“**%&’()*+”

REPRESENTS
4
FORMS

4643 PRINTER SERVICE



SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section describes the functional and logical operations of the printer system. A description of the input data is provided, followed by two levels of circuit description: functional and detailed.

4.2 INPUT DATA DESCRIPTION

Data is transmitted from the user system in an 8-bit (7-bit optional) format. An optional ninth bit, termed PI (paper instruction) is used for coding certain types of paper motion commands and loading DAVFU format codes.

The DPC Parallel Interface is the standard interface. Two other types of interfaces are available on an optional basis: the Serial Interface and the DPC Centronics-Compatible Interface. Interface details are described in paragraph 4-4.

Regardless of the type of interface used, information carried by the eight data bits and PI bit includes print characters, ASCII-coded paper motion characters, VFU-coded paper motion characters, direct access VFU (DAVFU) data, and condensed and expanded print codes. A fifth type of information, SELECT and DESELECT codes, is reserved for use by the optional DPC Centronics-Compatible Interface. All print characters, some of the paper motion characters, SELECT and DESELECT codes, and condensed and expanded print codes are normally ASCII-coded. As an option, the user may transmit data in a code of his own choosing. A special code converter then translates the user-coded data into ASCII characters for internal use. Table 4-1 lists the ASCII-coded characters recognized by the printer.

4.3 FUNCTIONAL DESCRIPTION

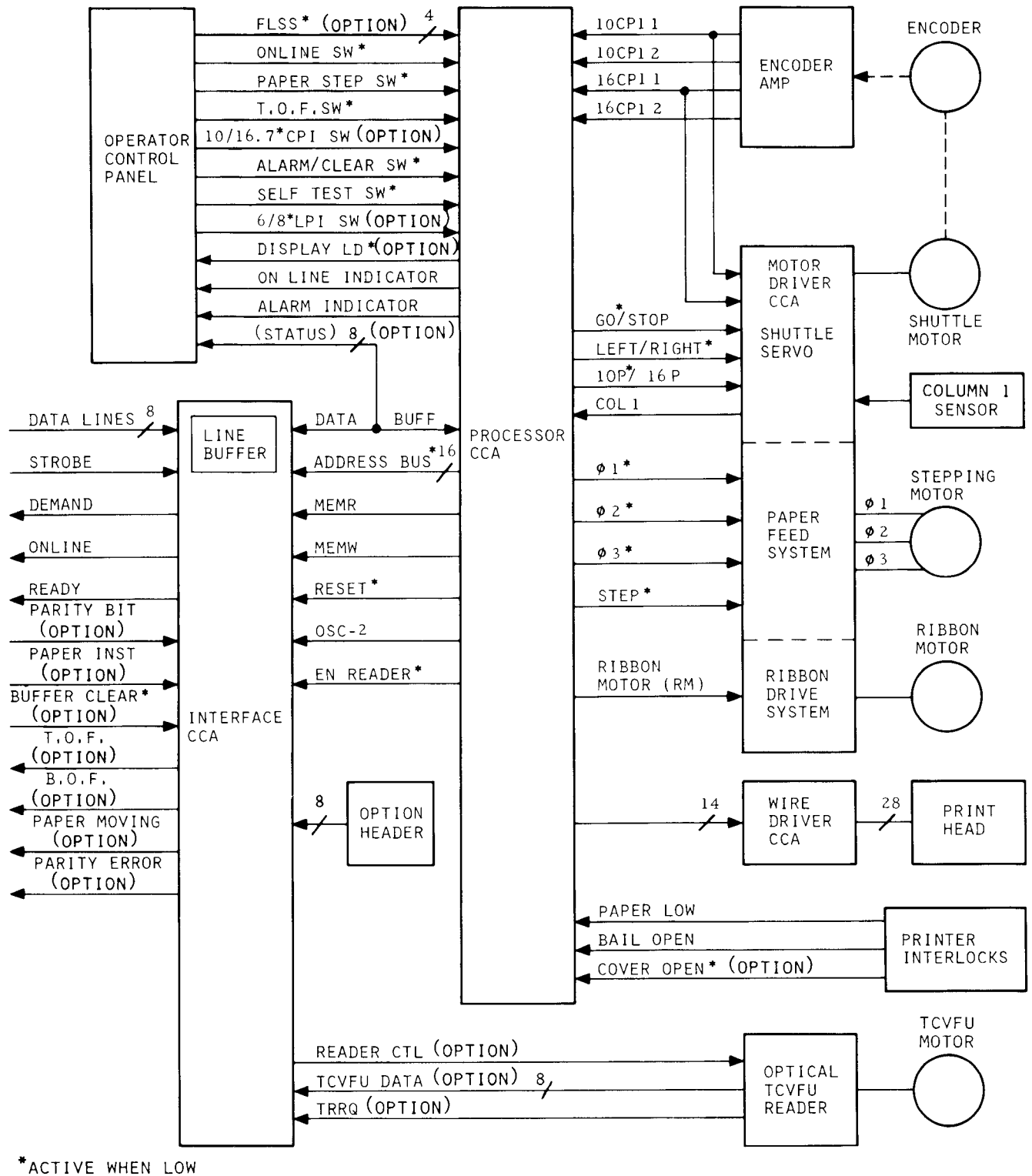
Figure 4-1 is a functional block diagram of the major printer assemblies and components. These include the Interface CCA, Processor CCA, Wire Driver CCA, Motor Driver CCA, operator control panel, shuttle servo motor and encoder, ribbon motor, and printer interlocks. In addition to the standard components, the printer may include two optional items: the tape controlled vertical format unit (TCVFU) and the option header. The following paragraphs describe the data flow and interaction among the printer components during different modes and phases of printer operation.

Table 4-1. ASCII-CODED CHARACTERS

ASCII 128 CHARACTER PRINTING SET							
NON-PRINTING				ASCII 96 CHARACTER PRINTING SET			
b8 b7 b6 b5 b4 b3 b2 b1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
0 0 0 0 0				SPACE			À Á Â Ã Ä Å Æ Ç È É
0 0 0 0 1				SELECT**			Ê Ë Ì Í Î Ï Ñ Ò Ó
0 0 0 1 0				CD*			Ô Õ Ö × Ø Ù Ú Û Ü
0 0 0 1 1				DESELECT			Ý Þ ß à á â ã
0 1 0 0 0				\$ % & ' () * + , - . /			ä å æ ç è é ê ë
0 1 0 0 1							ì í î ï ð ñ ò ó
0 1 0 1 0							ô õ ö ÷ ø ù ú û
0 1 0 1 1							ü ý þ ÿ
1 0 0 0 0							ÿ
1 0 0 0 1							
1 0 0 1 0							
1 0 0 1 1							
1 1 0 0 0							
1 1 0 0 1							
1 1 0 1 0							
1 1 0 1 1							
1 1 1 0 0							
1 1 1 0 1							
1 1 1 1 0							
1 1 1 1 1							

*CD IS DELETE CODE FOR DPC CONTRONICS-COMPATIBLE I/F ONLY

**SELECT AND DESELECT CODES FOR DPC CONTRONICS-COMPATIBLE I/F ONLY



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Figure 4-1. 4643 Printer, Functional Block Diagram

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4.3.1 Modes of Operation

The printer operates in four basic modes, as follows:

1. Initialization
2. On Line
3. Self Test
4. Off Line

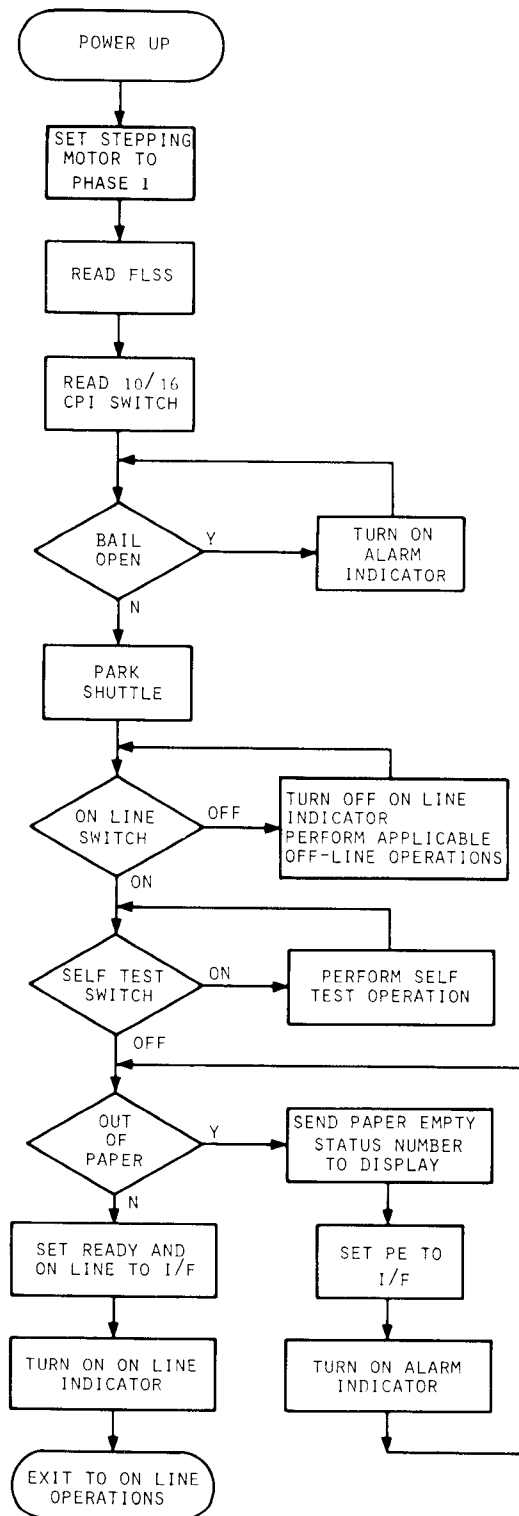
a. Initialization (Figure 4-2)

Figure 4-2 is a simplified flow diagram of activities that occur during the initialization mode of operation. Following power up, the printer enters the initialization mode of operation. During this mode, the Processor CCA locks the three-phase stepping motor in phase 1, stores the form length select switch (FLSS) information, reads the 10/16 CPI switch, and monitors the condition of the bail. If the bail is open, the ALARM indicator on the control panel will be turned on. The ALARM indicator will remain illuminated until the bail-open condition has been corrected.

The Processor CCA will then park the shuttle in the home position. To park the shuttle, the Processor CCA first checks the position of the shuttle with respect to column 1. If the shuttle is positioned to the left of column 1, the Processor CCA will signal the shuttle servo circuit within the Motor Driver CCA (via signals GO/STOP, LEFT/RIGHT) to move the shuttle to the right of column 1. If the shuttle is not positioned to the left of column 1 after the power is first turned on, the Processor CCA will signal the shuttle servo circuit to move the shuttle from right to left. Then, when column 1 is sensed, the Processor CCA will signal the shuttle servo circuit to reverse direction from left to right, and will again stop the shuttle servo motor to the right of column 1.

Direction of the shuttle servo motor travel and shuttle position is computed from information supplied by the encoder, which is mounted on the same shaft as the shuttle servo motor. When the shuttle servo motor travels, the encoder supplies a continuous stream of four output signals: 10CPI 1, 10CPI 2, 16CPI 1, and 16CPI 2. Only one pair of signals is used at any given time, depending upon the position of the optional 10CPI/16 CPI pitch select switch. With the switch not installed, the Processor CCA monitors signals 10CPI 1 and 10CPI 2. From these, the Processor CCA computes both direction of shuttle travel and shuttle position.

After the shuttle is parked, the Processor CCA monitors the position of the on line flip-flop. If the on line flip-flop is reset, off-line operations are performed. If the on line flip-flop is set, the position of the self test switch is monitored. Assuming that the self test switch is off, the printer interlocks are monitored for an out-of-paper condition. If the printer is out of paper, a paper empty status word is sent on the data bus to the control panel along with the DISPLAY LD signal. This will cause the optional status indicator to display



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Figure 4-2. Initialization Mode of Operation

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a two-digit number that corresponds to the out-of-paper condition. In addition, when an out-of-paper condition has been detected, a PE error signal is sent to the Interface CCA via the data bus, and the ALARM indicator on the control panel turns on.

After the out-of-paper condition has been eliminated, or if no out-of-paper condition existed in the first place, the READY and ON LINE signals are sent to the Interface CCA, and the ON LINE indicator is turned on. The Interface CCA then raises the READY and ON LINE signals to the user system.

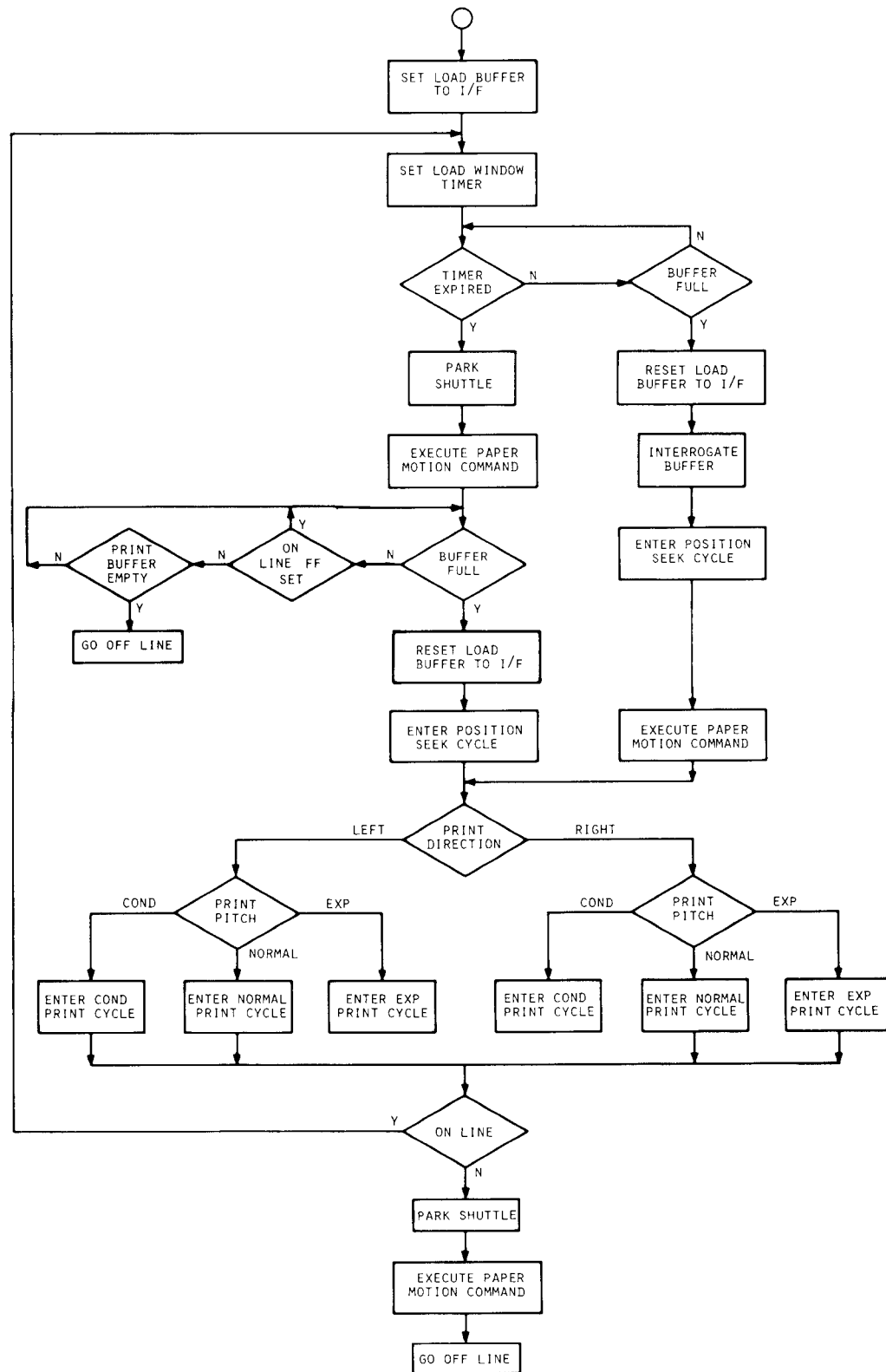
b. On Line (Figure 4-3)

Figure 4-3 is a simplified flow diagram of the activities that occur during the on-line mode of operation, which include:

1. Load Buffer Cycle
2. Buffer Interrogate Cycle
3. Position Seek Cycle
4. Print Cycle
5. Paper Motion Cycle

The first event in the online mode of operation, the load buffer cycle, is initiated when the Processor CCA transmits a load buffer signal to the Interface CCA and ends when the Interface CCA returns a buffer full signal. Along with the load buffer signal, the Processor CCA sets a load window timer. If the buffer full signal is returned before the timer expires, the Processor CCA will reset the load buffer signal, interrogate the line buffer, enter the position seek cycle, execute the paper motion command, and will then enter the print cycle. If the timer expires before the buffer full signal is received, the Processor CCA will park the shuttle, execute the paper motion commands, and then wait for the buffer full signal. Upon receipt of the buffer full signal, the Processor CCA will reset the load buffer signal, interrogate the buffer, enter the position seek cycle, and enter the print cycle.

1. Load Buffer Cycle - Once initiated by the Processor CCA, the load buffer cycle is under control of the Interface CCA and is used to load user data into the line buffer. Typically, the user will transmit one line of 132 print characters, followed by a paper motion (control) character. Receipt of the paper motion character terminates the load buffer cycle, causing the Interface CCA to transmit the buffer full signal to the Processor CCA. In standard printers configured as shown in figure 4-1, each character is requested and strobed on a demand/strobe basis, transmitted over the eight data lines, and stored sequentially within the line buffer. In those printers configured with either the optional Serial Interface CCA or optional DPC Centronics-Compatible Interface CCA, interface communication and character transmission are as described in paragraph 4.4.



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Figure 4-3. On Line Mode of Operation

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2. Buffer Interrogate Cycle - During this cycle, the Processor CCA examines the contents of the line buffer one character at a time, starting with the last character loaded, and in a descending order. Each character found to be valid is restored in its original form. Non-printable characters are replaced by a question mark. Parity errors are replaced by a space code in the standard printer, and by a dollar sign in printers configured with a Serial Interface CCA. At the end of the buffer interrogate cycle, the paper motion character, the buffer address of the end of the line, and the buffer address of the beginning of the line are stored within the Processor CCA.

3. Position Seek Cycle - The position seek cycle is used by the Processor CCA to compute the print direction of the line of data received during the preceding load buffer cycle. To accomplish this, the Processor CCA first determines the current position of the shuttle. This information, along with the beginning and end of line information obtained during the buffer interrogate cycle, is then used to determine the most efficient direction for printing the upcoming line.

4. Print Cycle - The print cycle consists of three interrelated operations: shuttle motion, printing, and ribbon motion. Once started, shuttle motion is normally a continuous activity, lasting for the duration of the printing operation. Shuttle motion is under control of the Processor CCA. The Processor CCA uses the GO/STOP and LEFT/RIGHT signals along with 10P/16P to control the time, direction, and rate of shuttle travel to the shuttle servo circuit. In turn, the shuttle servo circuit supplies driving power accordingly to the shuttle motor. Exception: if more than one line of paper advance is executed, or if the buffer full signal from the Interface CCA is received after the load window timer has expired, shuttle motion will be interrupted and the shuttle will be parked.

Printing involves converting the ASCII-coded print characters stored in the line buffer into dot patterns, and then selectively firing the print wires in the left and right wire columns of the print head. Assume that the computation made during the position seek cycle has resulted in a left to right print direction. Accordingly, the Processor CCA accesses, via the data bus, the first valid print character stored in the line buffer. Within the Processor CCA, the ASCII-coded character is converted into seven distinct dot patterns, one for each character column, and three blanks. The three blanks account for the intercharacter spacing. When the print head reaches the position where the first character is to be printed, the Processor CCA, via the Wire Driver CCA, selectively fires the print wires of the left and right wire columns. This procedure is repeated for each character until all valid print characters currently stored in the line buffer are printed.

Figure 4-4 is an example of a typical print sequence character in a line consisting of 14 print characters and a paper motion character. The first character in the line, the letter "F", is in buffer location 52; the last character, the letter "W", is in buffer location 65; and the control code is in buffer location 66. Direction of print is from left to right, determined during the position seek cycle. Accordingly, printing starts when the shuttle reaches character column 52, and the first character to be printed is the letter "F". Similarly, printing stops in column 65 with the letter "W". Note that when print direction is from right to left, printing starts with the letter "W" and ends with the letter "F".



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Character conversion and dot pattern generation is implemented by a character generator ROM. As shown in figure 4-5, each of the 128 valid characters is assigned sixteen 8-bit ROM locations - eight locations for the right wire column, and eight locations for the left wire column. Only seven of the eight locations contain dot information; the eighth location is blank and forms one of the three intercharacter spaces. Information contained in a given location and identified in figure 4-5 by the letter "X" determines whether or not a dot is to be printed. Since there are only seven wires per wire column, bit 8 is always a blank. Each time a character is accessed from the line buffer, its ASCII code is used as a general address, pointing to eight locations within each half of the character generator ROM. One of eight locations is then selected by the column counter, a 4-bit BCD counter. When printing from left to right, the column counter is incremented from 0 to 9 with each encoder mark derived from the 10 CPI 1/10 CPI 2 (or 16 CPI 1/16 CPI 2) output of the encoder. Similarly, when printing from right to left, the column counter is decremented from 9 through 0 with each encoder mark. To account for the two additional intercharacter spaces (the other space is obtained from the blank column of the character generator), the character generator is not accessed. Instead, blanks are generated during counts 8 and 9 of the column counter when printing in either direction.

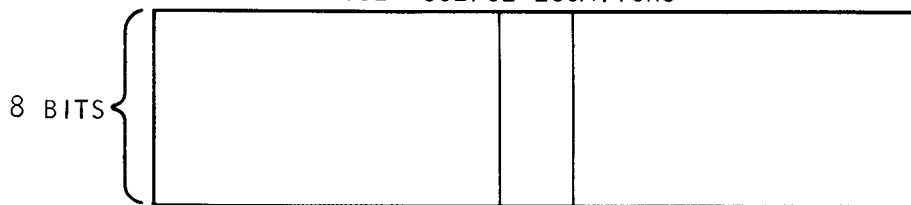
Figure 4-6 is a simplified flow diagram of activities that occur during the print operation. For initial conditions, assume that the line buffer contains ten valid print characters in the first ten locations of the line buffer, that the column counter is at count 0, and that print direction is from left to right. When the first character is accessed from the line buffer, its ASCII code is combined with the dot column counter count to form a ROM address. This address is then used to access the character generator ROM to obtain the dot pattern of the first column of the first character. Next, the encoder mark is monitored. When the encoder mark occurs, the print wires are fired in a pattern corresponding to the pattern of dots contained in the addressed ROM location.

After the first column of the first character has been printed, and because the print direction is toward the right, the column counter is incremented to 1. Next, the column counter is tested for the counts of 0, 8, and 9. Since the count is 1, the sequence returns to access another location in the character generator ROM. Since the ASCII code did not change, the new location will contain the dot pattern for dot column 2 of character 1. After dot column 2 of character 1 has been printed, five more passes are made through the character generator ROM, printing dot columns 3 through 7. When the dot column counter reaches the count of 7, another pass is made through the character generator ROM. This time, no printing will occur, leaving column 8 of the first print character blank. On the counts of 8 and 9, the character generator is not accessed, and blanks are in dot columns 9 and 10 of the first character.

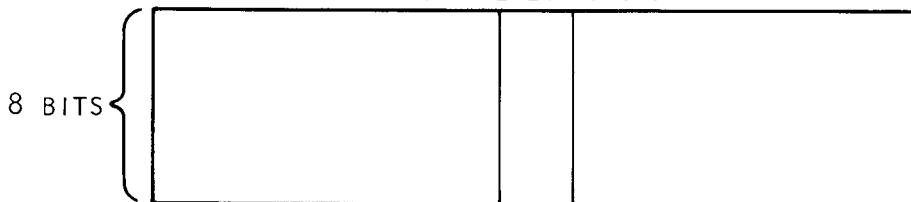
When the column counter is incremented from 9 to 0, the character counter is incremented, and a new ASCII-coded character is accessed from the line buffer. The entire sequence is repeated nine more times until all ten valid print characters are printed.

RIGHT HALF OF
CHARACTER GENERATOR ROM
1024 USEFUL LOCATIONS

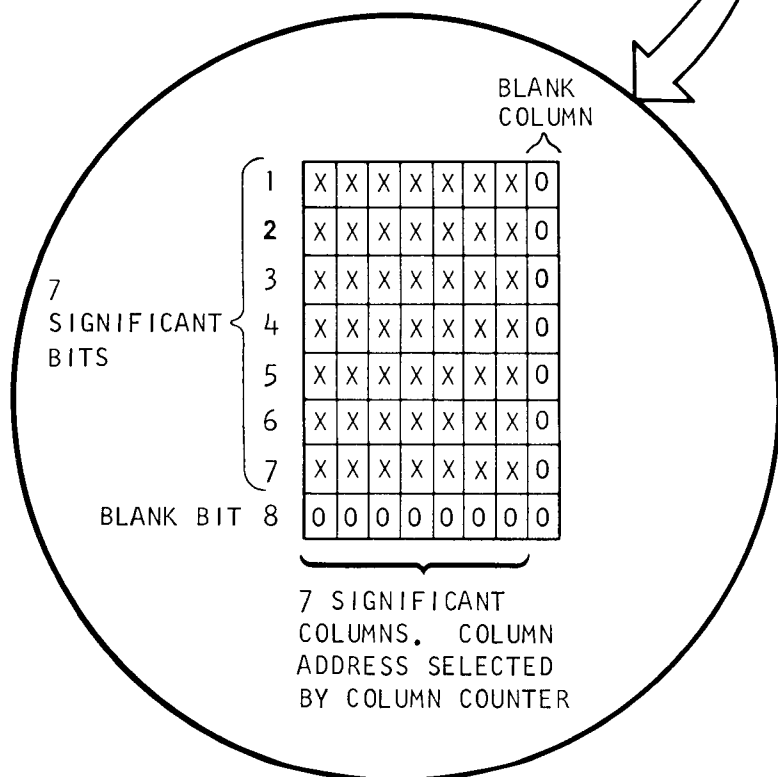
THEORY OF OPERATION



LEFT HALF OF
CHARACTER GENERATOR ROM
1024 USEFUL LOCATIONS



8 LOCATIONS/CHARACTER
CHARACTER ADDRESS
SELECTED BY ASCII
CODE



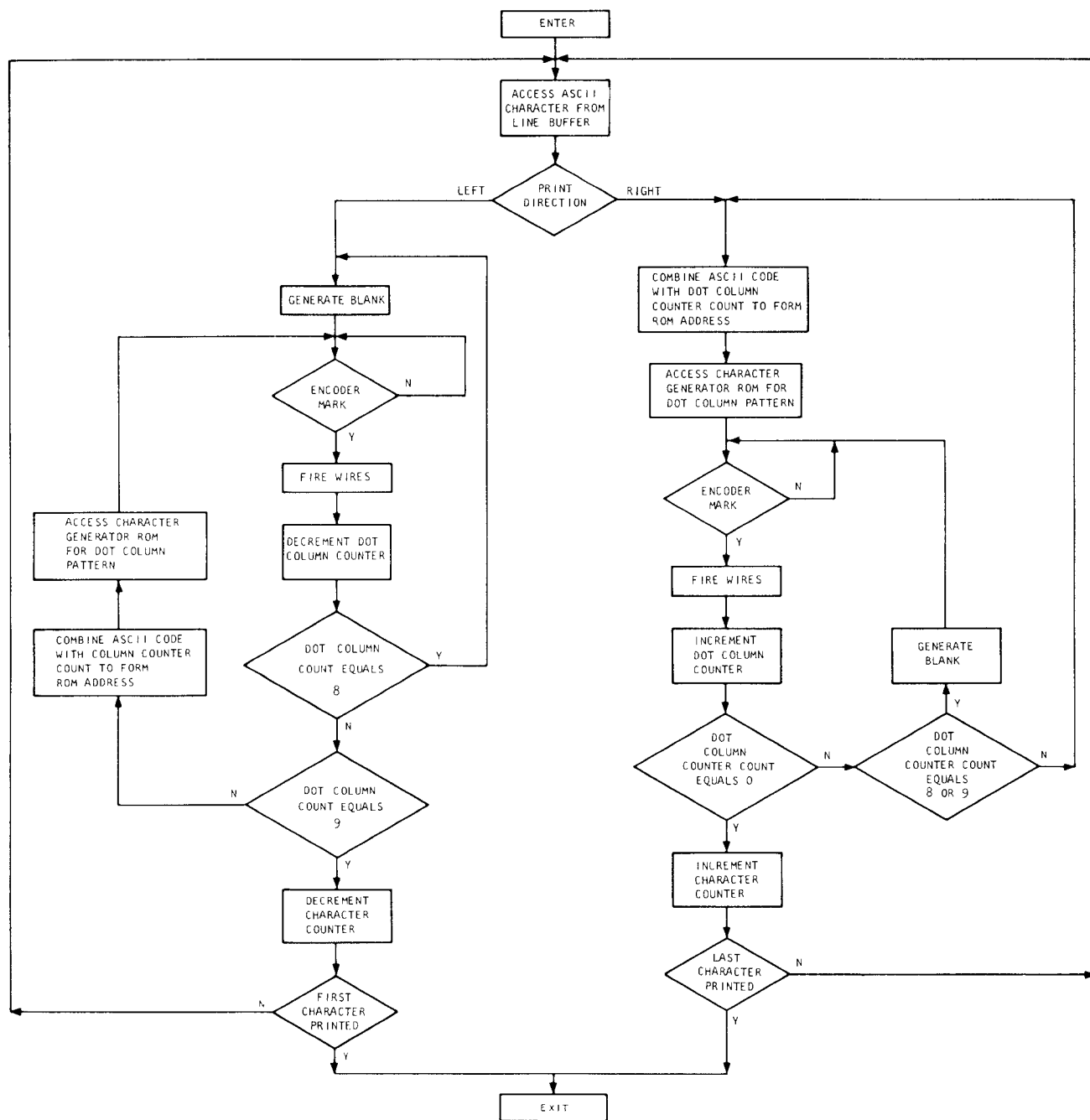
TYPICAL CHARACTER

NOTE:

X = EITHER 0 (BLANK)
OR 1 (DOT)

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Figure 4-5. Character Generator ROM Structure



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Figure 4-6. Print Operation, Simplified Flow Diagram

When printing from right to left, both the character counter and dot column counter start at the highest count, and are decremented during each applicable pass. Since the dot column counter is initially at 9, a blank is generated immediately, and also during the next pass when the dot column count is at the count of 8. On the count of 7, the character generator is accessed for the first time. When the dot column counter recycles from 0 to 9, the character counter is decremented and a new ASCII character is accessed. The print operation ends when the first and final character is printed. In all other respects, the sequence of events is the same as that of the left-to-right print operation.

Ribbon motion is initiated by the Processor CCA at the start of the print cycle through the ribbon drive system of the Motor Driver CCA, turning on the ribbon motor. Once started, ribbon motion is continuous for the duration of the print operation. Exception: as in the case of the shuttle motion, when the load buffer time exceeds the load window, ribbon motion is stopped and resumed at the start of the next print cycle.

5. Paper Motion Cycle - During the paper motion cycle, the command contained within the previously stored paper motion character is now executed. To do so, the Processor CCA decodes the paper motion character, and accordingly issues a series of stepping motor phase and step signals to the Motor Driver CCA. In turn, the Motor Driver CCA generates a series of stepping motor power signals. These signals are transmitted to the stepping motor, causing paper to advance a fixed number of lines (or one line).

c. Self Test

The self-test feature provides the means of testing the printer under dynamic conditions. It operates with the printer on line and in the test mode (self-test signal supplied by the control panel to the Processor CCA). However, the printer does not communicate with the user system. Instead, a fixed pattern of print and control characters is obtained from a memory area within the Processor CCA. In all other respects, the self-test operation is identical to a normal on-line operation. Once started, printing is automatic and continuous for 264 lines (see figure 3-6). After printing stops, the printer goes off line. To resume test operations, the operator must press the ON LINE switch on the control panel.

d. Off Line

When the printer is off line, the Processor CCA routinely checks the state of the various control panel switches. Two operations may be initiated at this time: paper step, and top of form. When the operator presses the PAPER STEP switch, signal PAPER STEP SW is applied to the Processor CCA. In turn, the Processor CCA, through signals Ø1, Ø2, Ø3, and STEP, turns on the stepping motor and causes paper to advance a single line. Similarly, when the operator presses the TOPOF FORM switch, signal T.O.F. SW causes the Processor CCA to turn on the stepping motor until the paper reaches the top of the next form. Pressing and holding of either the TOP OF FORM or PAPER STEP switch will cause paper to advance continuously. To prevent the ribbon from smearing the paper, the ribbon drive system is active during the top of form operation.

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4.3.2 Optional Printer Features and Components (Figure 4-1)

Optional printer components depicted in figure 4-1 and discussed in this paragraph include the Tape Controlled Vertical Format Unit (TCVFU) and the Option Header. An optional feature, the Direct Access Vertical Format Unit (DAVFU), not shown in figure 4-1, is also discussed here. For a complete list of print options, refer to section VI of this manual.

a. Vertical Formatting

Printers equipped with either a TCVFU or DAVFU option can accept a group of paper motion characters termed vertical format or VFU. These characters are not ASCII coded, but are accompanied by the optional print instruction signal PI. Upon recognition of the PI-coded paper motion character, the printer advances paper according to a pattern stored in the VFU area of the line buffer within the Interface CCA.

There are two categories of VFU-type paper motion characters, tape channel, and step count, as specified by bit 5 of the character. When bit 5 is a zero, paper is moved to a tape channel number specified by the value field encoded within the four least significant bits of the character. When bit 5 is a one, paper is advanced a number of lines encoded within the value field. Table 4-2 lists the binary codes used to transmit VFU-type paper motion characters.

b. TCVFU

The TCVFU option consists of an optical reader and motor. VFU information contained on the tape is loaded during the off line mode into the VFU area of the line buffer. Once loaded, the Processor CCA reads the VFU information directly from the line buffer, and the TCVFU becomes inactive. Note that the TCVFU option requires an option header.

To load VFU information from the tape to the line buffer, the operator first places the printer off line. Next, the operator presses a start switch on the optical reader, generating tape request signal TRRQ. Signal TRRQ is channelled through the Interface CCA and data bus to the Processor CCA. In response, the Processor CCA returns signal READER CTL through the data bus and Interface CCA, turning on the TCVFU motor. While the motor is running, TCVFU data is routed through Interface CCA and over the data bus, one byte at a time, to the Processor CCA. From there, the TCVFU data is routed over the data bus and loaded in the line buffer. When all lines of the TCVFU tape are read and loaded, the Processor CCA disables the READER CTL signal, turning off the TCVFU motor.

TABLE 4-2. VFU-TYPE PAPER MOTION CHARACTERS

Code									Command	
b8	b7	b6	b5	b4	b3	b2	b1	PI	Description	Group
X	0	0	0	0	0	0	0	1	Move paper to Channel 1	Tape Channel
X	0	0	0	0	0	0	1	1	Move paper to Channel 2	
X	0	0	0	0	0	1	1	1	Move paper to Channel 3	
X	0	0	0	0	0	1	0	1	Move paper to Channel 4	
X	0	0	0	0	1	0	0	1	Move paper to Channel 5	
X	0	0	0	0	1	0	1	1	Move paper to Channel 6	
X	0	0	0	0	1	1	0	1	Move paper to Channel 7	
X	0	0	0	0	1	1	1	1	Move paper to Channel 8	
X	0	0	0	1	0	0	0	1	Move paper to Channel 9	
X	0	0	0	1	0	0	1	1	Move paper to Channel 10	
X	0	0	0	1	0	1	0	1	Move paper to Channel 11	
X	0	0	0	1	0	1	1	1	Move paper to Channel 12	
X	0	0	1	0	0	0	0	1	Move paper 0 line	Step Count
X	0	0	1	0	0	0	1	1	Move paper 1 line	
X	0	0	1	0	0	1	0	1	Move paper 2 lines	
X	0	0	1	0	0	1	0	1	Move paper 3 lines	
X	0	0	1	0	1	0	0	1	Move paper 4 lines	
X	0	0	1	0	1	0	1	1	Move paper 5 lines	
X	0	0	1	0	1	1	0	1	Move paper 6 lines	
X	0	0	1	0	1	1	1	1	Move paper 7 lines	
X	0	0	1	1	0	0	0	1	Move paper 8 lines	
X	0	0	1	1	0	0	1	1	Move paper 9 lines	
X	0	0	1	1	0	1	0	1	Move paper 10 lines	
X	0	0	1	1	0	1	1	1	Move paper 11 lines	
X	0	0	1	1	1	0	0	1	Move paper 12 lines	
X	0	0	1	1	1	0	1	1	Move paper 13 lines	
X	0	0	1	1	1	1	0	1	Move paper 14 lines	
X	0	0	1	1	1	1	1	1	Move paper 15 lines	

X = Don't care condition

c. DAVFU

Printers equipped with a DAVFU option are loaded with vertical format data by the user. DAVFU data, like print and paper motion characters, is transmitted over the 8-bit data path on a time-shared basis. The first character in a DAVFU stream is the DAVFU start code, which signifies that the next block of characters contains DAVFU tape channel information. The last character in a DAVFU stream is a DAVFU stop code, which marks the end of the DAVFU transmission cycle. DAVFU data is transmitted in pairs of characters. Therefore, the total DAVFU character count must always be even; an odd number of characters is interpreted by the printer as a DAVFU error. Refer to table 3-4 for DAVFU loading details.

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d. Option Header

The option header provides a means for configuring the printer with available options, as detailed in section VI of this manual. Information from the option header is supplied on a 16 bit bus to the interface CCA. Part of the information is used internally by the Interface CCA, while the remainder is routed over the data bus to the Processor CCA. Periodically, the Processor CCA examines the information supplied by the option header and accordingly, decides the manner in which data is to be processed.

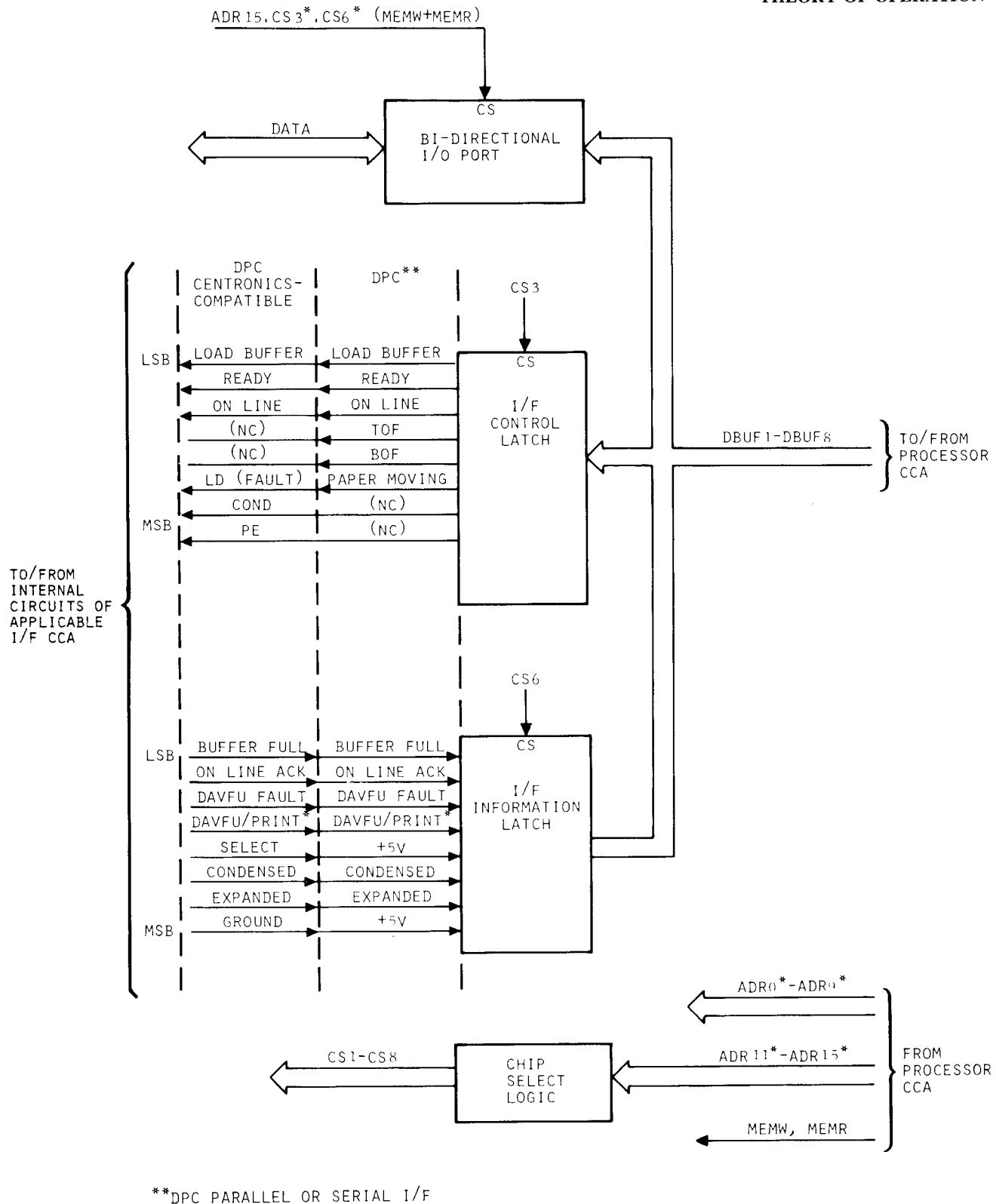
4.4 INTERFACE DESCRIPTION

The standard M200 printer is designed to operate with a DPC eight bit (seven bits optional) parallel interface, and is configured with a DPC Parallel Interface CCA as depicted in figure 4-1. As an option, the printer can be configured to operate with a Serial Interface or with a DPC Centronics-Compatible Interface. To implement either option, the standard DPC Parallel Interface CCA is replaced with the applicable Interface CCA.

The Processor CCA cannot distinguish between a DPC Parallel Interface CCA and a Serial Interface CCA; both connect to the Processor CCA through the same data and address buses and have identical bit assignments within the buses. Connections between the DPC Centronics-Compatible Interface CCA and the Processor CCA are also made through the same buses as the DPC Parallel and Serial interfaces. However, a selected number of bits have been assigned different functions to accommodate the special needs of the DPC Centronics-Compatible Interface.

Figure 4-7 shows the circuits that are common to all Interface CCAs and the signals connected between any Interface CCA and the Processor CCA. Also shown are the bit assignment differences between the Centronics-Compatible Interface CCA and the other two Interface CCAs, labelled DPC. Information between the Interface CCA and Processor CCA is exchanged over a single 8-bit data bus, DBUF1-DBUF8, and then divided into three time-shared groups. One group is channelled by the bi-directional I/O port, and includes all I/O data such as print, DAVFU, TCVFU, VFU, etc. The second and third signal groups are channelled, respectively, by the interface control latch and interface information latch, and together form a two-way communications path. The interface control latch stores input signals supplied by the Processor CCA, while the interface information latch stores output signals destined for the Processor CCA. Note the differences in bit assignments between the DPC Centronics-Compatible Interface CCA and the two DPC Interface CCAs. For example, bit 6 of the interface control latch is used for "paper moving" status with DPC-type interfaces, but it indicates a fault condition (LD) to a DPC Centronics-Compatible Interface. To differentiate between the two types of interfaces, the Processor CCA monitors bit 8 of the information latch; bit 8 is at ground level in the DPC Centronics-Compatible Interface CCA, and at +5V in the other two Interface CCAs.

In addition to the data bus, the Processor CCA supplies a 15-bit address bus (bit ADR10* is not used), along with signals MEMW and MEMR. Bits ADR11*-ADR15* are resolved in the chip select logic into chip select signals



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Figure 4-7. Common Interface CCA Circuits

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CS1-CS8, and are used within the Interface CCA to multiplex different devices that share a common data bus. Table 4-3 lists the function of each chip select signal.

TABLE 4-3. CHIP SELECT FUNCTIONS

Signal	Binary Address					Function
	A15	A14	A13	A12	A11	
CS1	1	0	0	0	0	Allows the Processor CCA to write into or read from the line buffer.
CS2	1	0	0	0	1	Allows the Processor CCA to read the last line-buffer address.
CS3	1	0	0	1	0	Allows the Processor CCA to write into the interface control latch.
CS4	1	0	0	1	1	Allows the Processor CCA to read the upper TCVFU bits.
CS5	1	0	1	0	0	Not used.
CS6	1	0	1	0	1	Allows the Processor CCA to read the interface information latch.
CS7	1	0	1	1	0	Allows the Processor CCA to read the lower TCVFU bits.
CS8	1	0	1	1	1	Allows the Processor CCA to read the option header.

Signals MEMW and MEMR specify the direction of the data flow. Address bits ADR0* - ADR9* are used to specify the line buffer (not shown in figure 4-7) location when accessed by the Processor CCA.

The following paragraphs provide detailed information on each of the three Interface CCAs.

4.4.1 DPC Parallel Interface (Figure 4-8)

NOTE

The following functional description applies to the standard, short-line DPC Parallel Interface CCA, referred to as the Parallel Interface CCA in the following discussion. Except for additional input differential drivers and receivers, this description also applies to the optional, long-line DPC Parallel Interface CCA (see section VI).

The Parallel Interface CCA is designed to enable parallel data transfer between the user system and the Processor CCA. In addition, the the Parallel Interface CCA provides the Processor CCA with information concerning print density, parity errors, system fault indications, on line/off line acknowledgement, and line buffer status.

a. Data Transfer Modes

Data transfer between the user system and the Parallel Interface CCA may be performed in two modes: normal, or fixed pulsed strobe mode. See figure 4-9 for the parallel interface timing relationships.

1. Normal Mode - In the normal mode of data transfer a demand/response or handshake technique is used which is initiated as follows: The Processor CCA generates clock signal OSC2, which is divided by two, to produce CK/2. While the CK/2 clock is operating, the Processor CCA raises signal READY, fed out of control latch U54 under the control of signals CS3* and MEMW*. When signal READY is high, the Processor CCA raises signal ON LINE, also fed out of control latch U54.

Next, the Processor CCA initiates the data transfer by raising LOAD BUFFER, also fed out of control latch U54. At this time, the Parallel Interface CCA demand control U5B generates signal DEMAND during the trailing edge of clock CK/2. While signal DEMAND is high, signal USER DEMAND is raised by user demand U15A. The user system is requested to transmit signal DATA STROBE, which is raised at the same time that print data characters or paper motion characters (represented by data bits DATA1-DATA8) are received on the leading edge of clock CK/2. Signal DATA STROBE clocks internal strobe U11A to generate STBINT*, which goes low at the same time that signal DATA STROBE goes high. Signal STBINT* affects the operation of the WRITE* signal and the loading of the line buffer, discussed in subsequent paragraphs.

2. Fixed Pulsed Strobe Mode - The fixed pulsed strobe mode of data transfer is similar to the normal mode, with one exception: when the printer raises DEMAND to request data, the user may respond by pulsing and dropping the DATA STROBE signal. This way, DATA STROBE drops while DEMAND is still high; i. e., before the character is stored in the line buffer. In such cases, the Interface CCA acknowledges DATA STROBE immediately to the user, but also generates a strobe signal for internal use termed STBINT*. This strobe signal is delayed until DEMAND drops, i. e.; until the data character is stored in the line buffer.

Circuits implementing the delayed strobe communication scheme include flip-flops U15A and U11A. Flip-flop U15A, together with its associated gate and inverter, control signal USER DEMAND. Normally, USER DEMAND follows DEMAND. When DATA STROBE is pulsed and goes low before DEMAND, USER DEMAND goes low, effectively acknowledging DATA STROBE. At the same time, flip-flop U11A activates signal STBINT*, and maintains STBINT* in an active state until DEMAND* goes low. Signal STBINT* is used to gate off the J-input to demand control flip-flop U5B, preventing DEMAND from being raised again until after the current character has been stored.

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b. Enabling and Timing Signals

To enable the various parallel interface circuits, the parallel Interface CCA uses internally generated signals, chip select signals, and timing signals generated by the Processor CCA.

1. Internally Generated Signals - Signal FF1 and its complement FF1* are generated by flip-flop U13A, and are active when the Interface CCA is loading data. The data load cycle is initiated when the Processor CCA raises LOAD BUFFER; a pulsed version of LOAD BUFFER, signal LDBUFPULA*, sets flip-flop U13A. Once set, flip-flop U13A remains set until the user transmits any termination character. Upon receipt of a termination character, signal CONTROL CODE* goes active. Once the termination character has been stored in the line buffer, signal DEMAND* is deactivated, clocking flip-flop U13A into the reset state and terminating the data load cycle.

Signals FF2 and FF2* are generated by U6A. The DEMAND signal clears U6A, and a pull-up sets U6A for an FF2 output. Flip-flop U6A is set on the rising edge of CK/2 after the user responds to DEMAND by raising DATA STROBE. Signal FF9*, when high, is a parity error signal which is generated by optional parity checker U2/U20 whenever a parity error is detected in the user data bit configuration.

2. Chip Select Signal Generation - Chip select signals CS1* through CS4* and CS6* through CS8* are generated by chip select generator U51 from the five most significant bits of the Processor CCA's address input, ADR11* through ADR15*. Processor CCA input signals MEMW* and MEMR* are combined to produce signal MEM R/W*, which is used to enable U51. Refer to table 4-4 for the enabling function of each chip select signal.

3. Timing Signal Generation - Signal OSC 2 from the Processor CCA or signal FF2 produces print control clock signal OSCFF, which clocks print control U43B whenever OSCFF goes low.

c. User Input Character Transfer

User system print or paper motion data characters (represented by data bits DATA1-DATA8) enter the Parallel Interface CCA and are strobed in data input latch U16 by signal DATA STROBE. The data characters are transferred to ASCII driver U21 if the data characters are ASCII-coded (i.e., if signal FF1* is active, and signals FF9 and CODE CONVERSION* are inactive).

Seven data bits, D1-D7, are transferred to ASCII driver U21 directly. The eighth bit, signal TB8, is controlled in one of two ways. When transmitting print characters, signal TB8 follows DABT8 when an 8-bit interface is used and is low when a 7-bit interface is used. When transmitting a paper motion control character, DABT8 is controlled by paper instruction bit TP1. Signal TP1 is controlled by signal PI when either the TCVFU or DAVFU is enabled, and implies a vertical format type paper motion control character. When signal PI is low, the paper motion character, if any, is ASCII-coded.

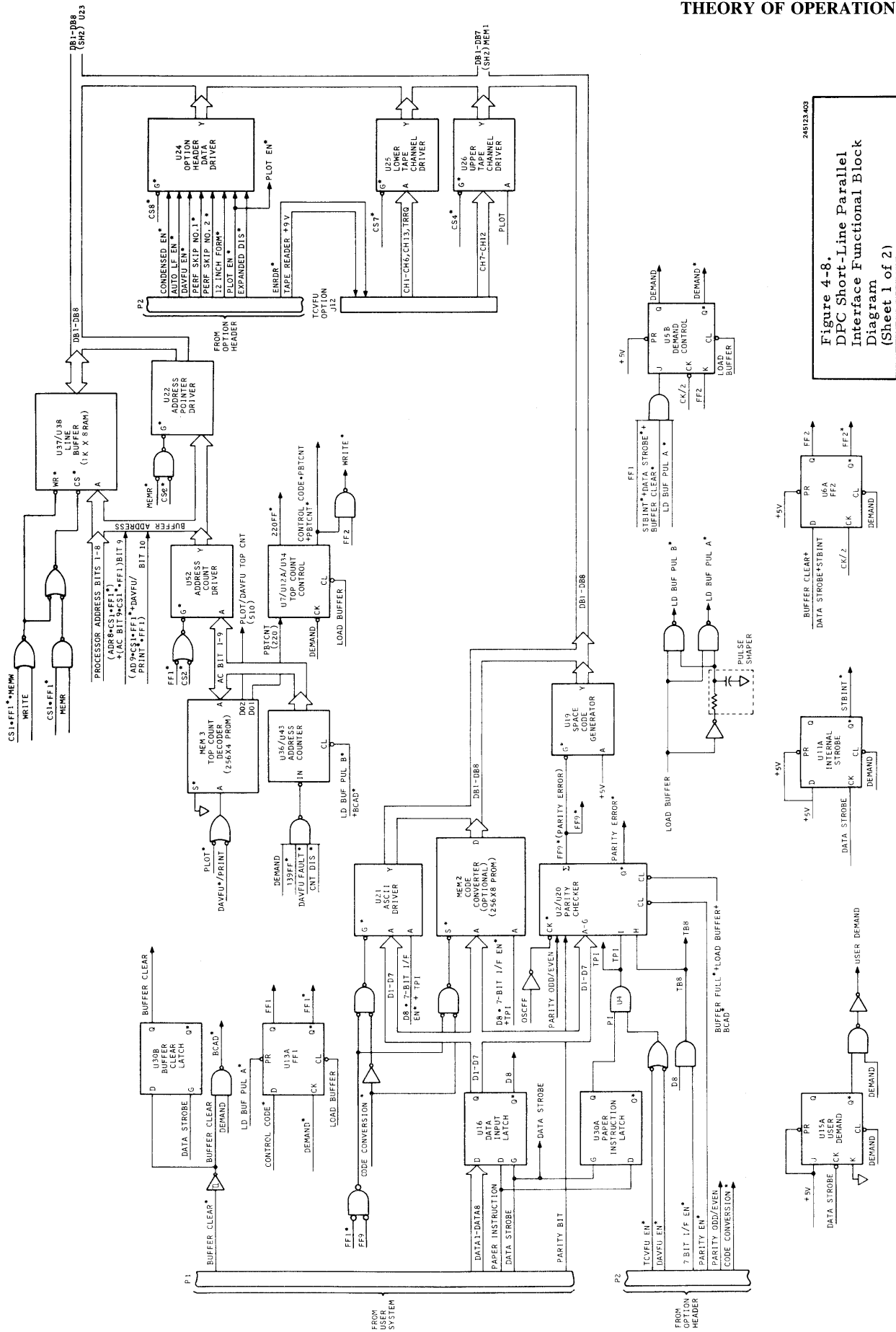


Figure 4-8.
DPC Short-Line Parallel
Interface Functional Block
Diagram
(Sheet 1 of 2)

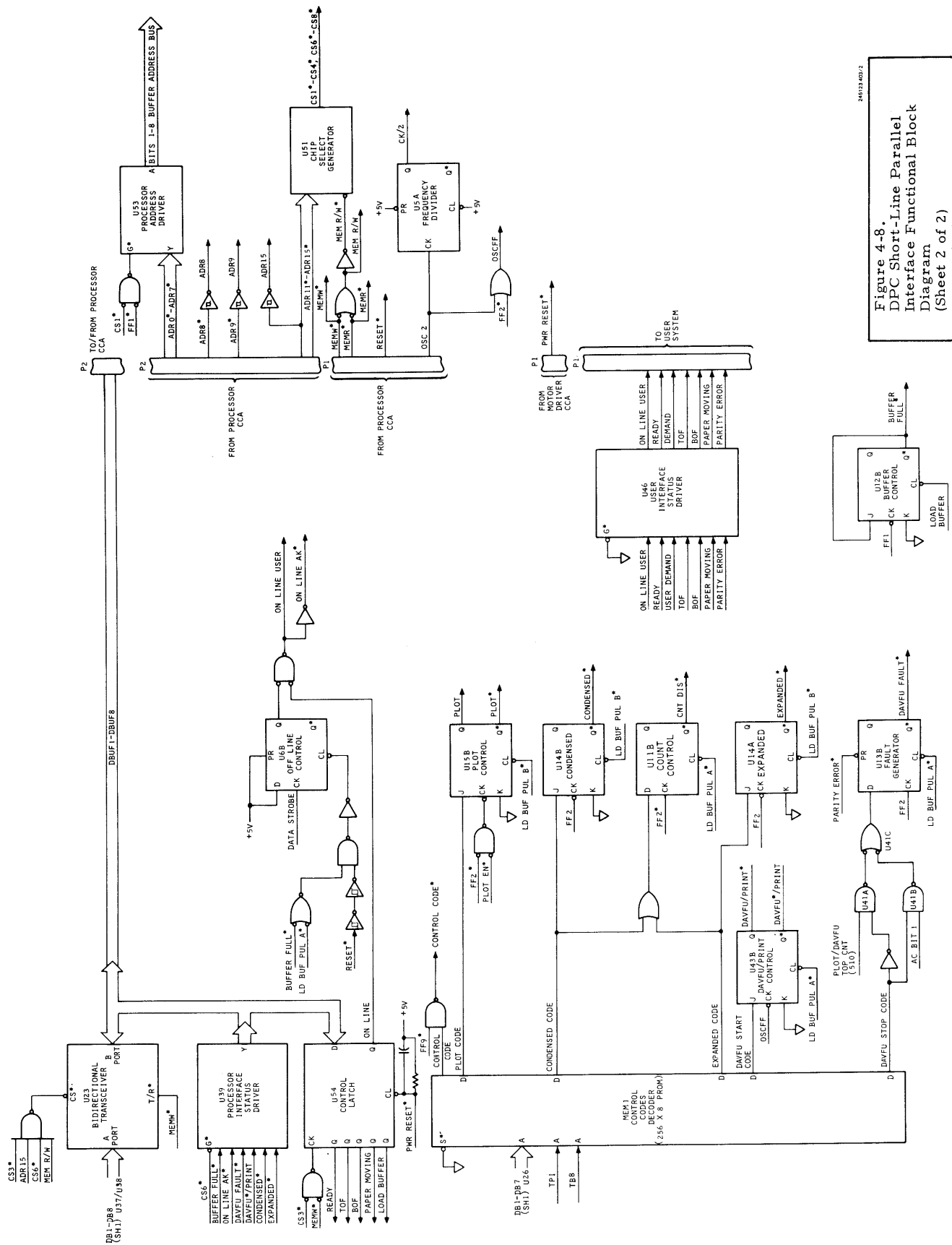
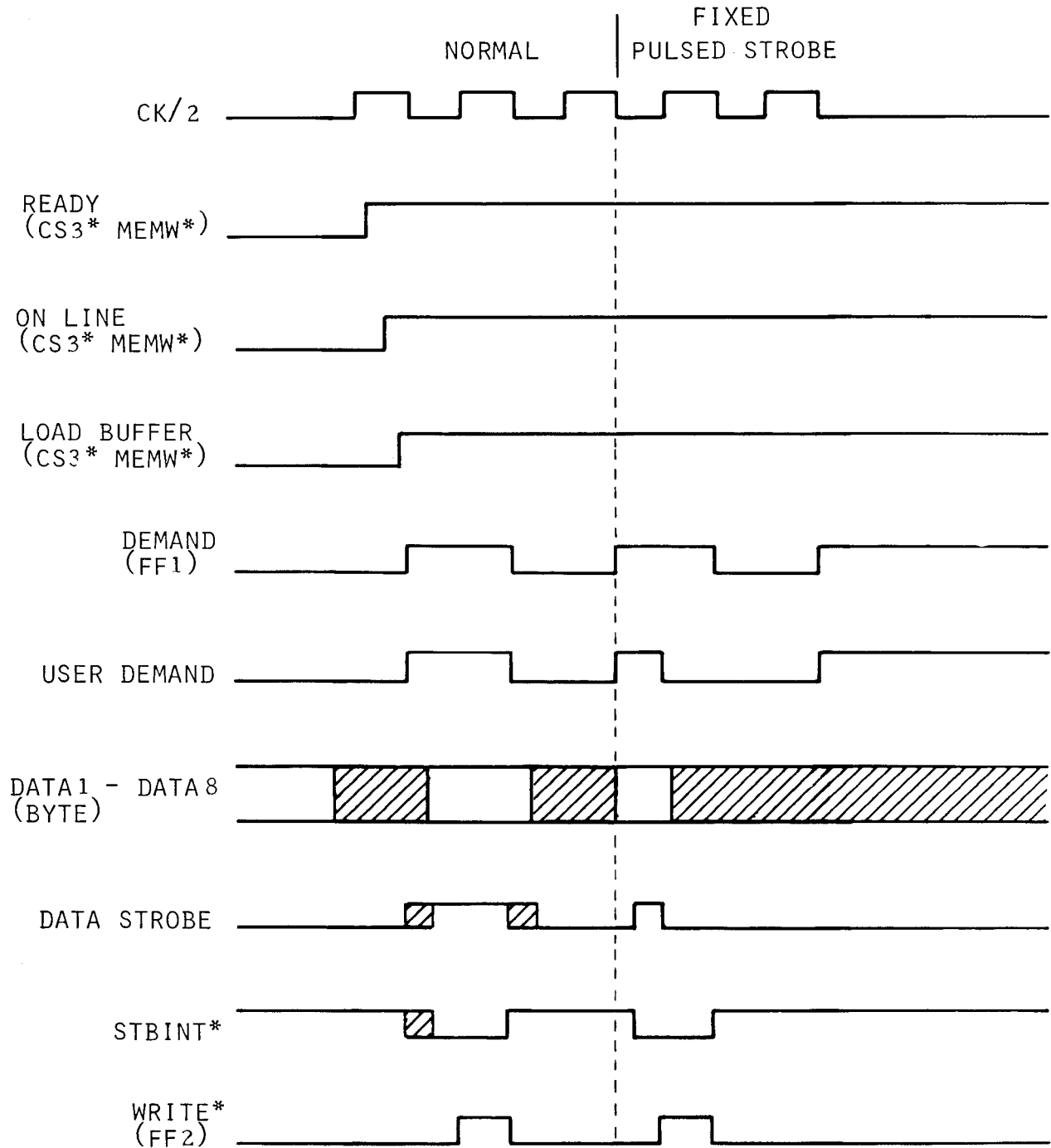


Figure 4-8.
DPC Short-Line Parallel
Interface Functional Block
Diagram
(Sheet 2 of 2)



NOTE

UNDEFINED AREA

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Figure 4-9. Parallel Interface Timing Diagram

THEORY OF OPERATION

If the characters are not ASCII-coded, they are transferred to an optional code converter PROM, MEM2, which encodes the characters into an equivalent ASCII format. MEM2 is enabled when signals CODE CONVERSION* and FF1* are active and signal FF9 is inactive. While MEM2 is enabled, ASCII driver U21 is disabled.

The output of ASCII driver U21 or code converter MEM2 is fed via data bus DB1-DB8 into the line buffer locations specified by address bits 1 through 10 obtained from address counter U36/U43A and DAVFU print control flip flop U43B.

d. Line Buffer Operation

Line buffer U37/U38 is a 1K by 8 RAM used to store ASCII-coded print data and vertical format data characters. Data may be written into the line buffer by either the Processor CCA or Parallel Interface CCA. Data is read out of the line buffer only by the Processor CCA. The Parallel Interface CCA may write into the line buffer by using signal WRITE for chip select and enabling purposes. The Processor CCA may write into the line buffer by using signals CS1 and MEMW and FF1*, and may read from the line buffer by using signals CS1, FF1* and MEMR. The Processor CCA uses the DBUF1-DBUF8 bus and through bi-directional transceiver U23, the DB1-DB* bus to access the line buffer. Bi-directional transceiver U23 is enabled by the expression $ADR15* \cdot CS3* \cdot CS6*$ (MEM R/W). In addition, the direction of the data flow within U23 CCA is controlled by signal MEMW*. When low, signal MEMW* allows the Processor CCA to write into the line buffer. When high, signal MEMW* allows the processor to read from the line buffer.

When loading user data, nine of the ten line buffer address bits are supplied by the address counter on lines ACBIT1-ACBIT9. The tenth address bit is obtained from the DAVFU/PRINT control U43B. When the line buffer is either read or written into by the Processor CCA, addressing is controlled by Processor address bits ADR0*-ADR9*.

1. Line Buffer Loading Completed - After loading a line of print data into the line buffer U37/U38, the user system must send a paper motion control code to terminate that line. Control codes decoder MEM1 issues signal CONTROL CODE*, provided that signal FF9* is not active. Signal CONTROL CODE*, when active, allows U13A to reset, which in turn clocks buffer signal BUFFER FULL*. Signal BUFFER FULL* is routed through processor interface status driver U39 to bus DBUF1-DBUF8, thereby informing the Processor CCA that the load operation has been completed.

2. Line Buffer Interrogation - In order to read from the line buffer U37/U38 memory locations, the Processor CCA must determine the beginning and end of the line just stored. To do so, the Processor CCA first reads the current address counter count, using the expression $CS2* \cdot MEMR*$ to enable both address count driver U52 and address pointer driver U22. Since the last character location on a line of print is the paper motion control code, the Processor CCA knows where the end of the line is. The address count is then placed on the low 8 bits of the processor address bus ADR0*-ADR7*. By decrementing

the address bus, each location of the line buffer is addressed and its contents examined. Processor address driver U53, which accesses the buffer address bus, is enabled by active signal CS1*, with signal FF1 inactive.

3. Line Buffer Address Counting - Address counter U36/U43A provides the location address for the line buffer when loading user data. A line may have up to 132 print characters and one control code. Address counter U36/U43A is a 9-bit binary counter which is cleared by the LD BUF PUL B* or BCAD* signal when low. Provided that signals 139FF*, DAVFU FAULT*, and CNT DIS* are high, signal DEMAND will initially preset the address counter to a count of one before the user input character is received (signal DATA STROBE not raised yet). Each time that signal DEMAND is raised, the address counter will be incremented by one count.

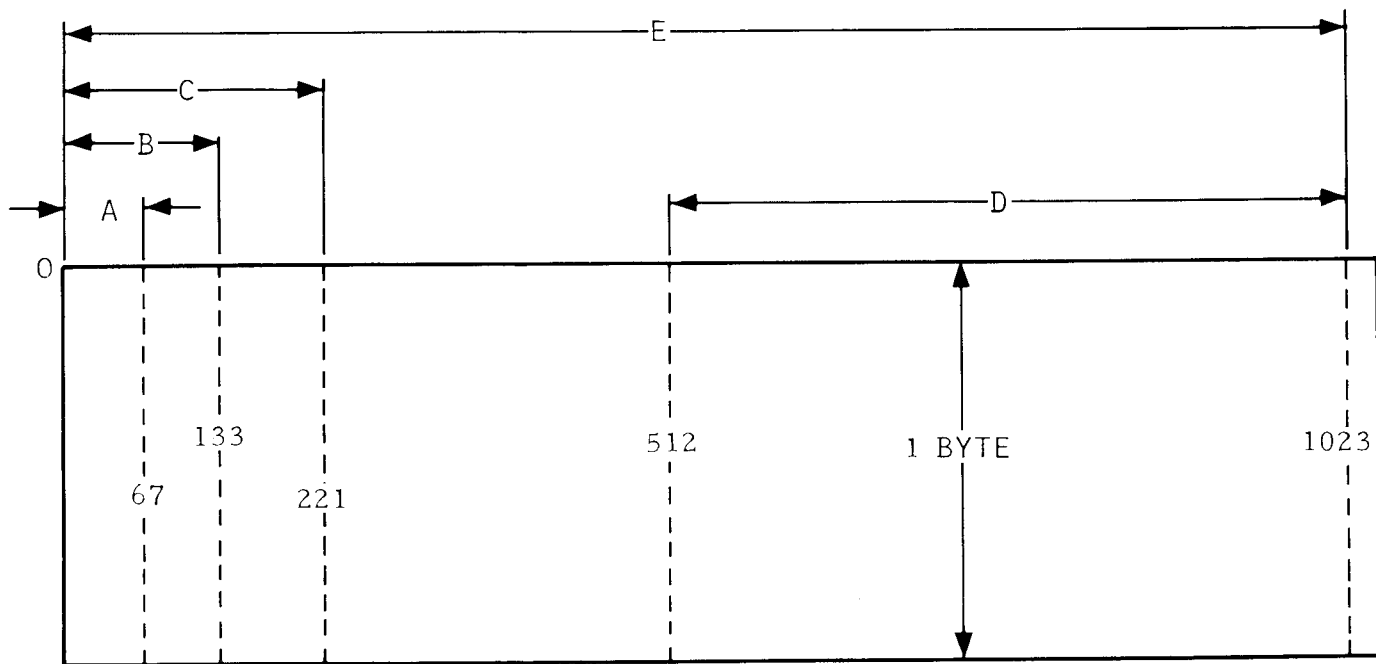
Address counter U36/U43A is only a 9-bit counter, and 10 bits are required to access the 1024 line buffer locations. A tenth bit is generated by wire-ORing Processor CCA address bit ADR9* with the DAVFU/PRINT* signal. When signal FF1* is active, the tenth address bit is controlled by signal DAVFU/PRINT*.

Figure 4-10 is a memory map of line buffer U37/U33. Location 0 is used for Processor CCA testing. Locations 1 through 222 are dedicated for print data and format control characters. Locations 223 through 511 are not used. Locations 512 through 1022 are dedicated for TCVFU or DAVFU characters. Note that the actual print data and format control character location is dependent upon the print density in use. If normal printing is used, 132 print data characters plus one paper motion control code character will make the maximum characters (total characters per line to be printed) total 133. If optional expanded printing is used, the maximum number of characters will be 67. For optional condensed printing, the maximum number of characters will be 221.

The maximum number of print data characters per line may not always be used. A terminating code is sent by the user system whenever a line of print data is completed, and that code will add one additional character to the total character count. For example, if in the normal printing mode 70 print data characters were sent by the user system, a total count of characters would be 71. Total memory space allotted for TCVFU or DAVFU characters is 512, spread over locations 512 through 1023. Not all locations are used.

4. Maximum Count - The DPC Parallel Interface CCA can accept a maximum of 220 print characters per line, and a maximum of 510 DAVFU characters per DAVFU load operation. Characters beyond the number of 220, or 510 when loading DAVFU data, are not registered. This function is implemented by top count decoder MEM3, a 256x4 PROM. MEM3 monitors the address counter bits ACBIT1-ACBIT9 along with signal DAVFU*/PRINT. When signal DAVFU*/PRINT is high, MEM3 generates print buffer top count signal PBTCNT when the count reaches 220. Similarly, when signal DAVFU*/PRINT is low, MEM3 generates top count signal PLOT/DAVFU TOPCNT when the count reaches 510. Signal PBTCNT inhibits, through the top count control, WRITE*, preventing the excess characters from being written in the line buffer. Signal PLOT/DAVFU TOPCNT, through signal 139FF*, also disables the address counter.

THEORY OF OPERATION



NOTE

1. A = LOADING PRINT DATA (EXPANDED)
2. B = LOADING PRINT DATA (NORMAL)
3. C = LOADING PRINT DATA (CONDENSED)
4. D = LOADING TCVFU OR DAVFU DATA
5. E = TOTAL MEMORY SPACE
6. LOCATION ZERO IS USED FOR TESTING ONLY

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Figure 4-10. Line Buffer Memory Location Mapping

Signal PLOT/DAVFU TOP CNT forms part of the logic that generates DAVFU FAULT*; if signal PLOT/DAVFU TOP CNT is encountered while DA STOP CODE is inactive, signal DAVFU FAULT* is generated. This signal is transmitted through the processor interface status drive U39 to the Processor CCA, generating a printer fault condition. Signal DAVFU FAULT* also inhibits the address counter.

5. DAVFU Fault Signal Generation - DAVFU fault signal is generated by fault generator U13B under one of three conditions:

- (a) Excessive number of characters
- (b) Odd number of characters
- (c) Parity error (if parity option is installed).

Gate U41A is activated when the number of DAVFU characters is excessive; i. e., when top count has been reached (510) and no stop code has been detected (DAVFU STOP CODE*). When gate U41A is active, it is ORed through gate U41C, allowing fault generator flip-flop U13B to be set.

Gate U41B is activated when the number of characters is odd (AC BIT 1), and a stop code has been detected (DAVFU STOP CODE). As in the previous case, when U41B is active, it is ORed through U41C, setting U13B.

A parity error condition sets U13B directly. When U13B is set, signal DAVFU FAULT* is activated. With DAVFU FAULT* active, the address counter is inhibited, and the Processor CCA is notified of the fault condition via the Processor Interface Status Driver U39.

6. DAVFU Character Storage - DAVFU characters are stored in line buffer U37/U38 memory locations 512 through 1022, as follows: The user system sends a DAVFU START CODE signal (156 in octal notation) via the DB1-DB8 bus to control codes decoder MEM1. The DAVFU START CODE signal is decoded and routed to print control U43B, which sets when signal OCSFF goes low. Signal DAVFU/PRINT* is generated and is used in conjunction with signal FF1, when high, to store DAVFU data characters in the line buffer. Up to 510 DAVFU data characters may be stored; however, the total count must add up to an even number or a DAVFU fault is generated which prevents any further line buffer storage while the fault exists.

At the end of the DAVFU character storage operation, the user system sends a DAVFU STOP CODE signal (157 in octal notation), which is decoded by MEM1 into the DAVFU STOP CODE and CONTROL CODE signals. Signal CONTROL CODE* disables signal FF1, which goes low and inhibits any further line buffer storage of DAVFU characters.

e. Paper Motion Characters and Paper Instruction

Paper motion characters fall into two categories: ASCII-coded and VFU type. ASCII-coded paper motion characters include CR, LF, and FF, with paper instruction bit PI low. VFU-type paper motion characters are accompanied by a high level PI signal, and are coded as follows: the four least significant bits of the character comprise a value field, while the fifth least significant

THEORY OF OPERATION

bit defines the method used to read the value field. For example, if the value field equals 7 and bit 5 is zero (tape channel), paper is moved until tape channel 7 is encountered, and is then stopped. On the other hand, if the value field equals 7 and bit 5 is a one (step count), paper is moved seven lines and then stopped.

f. Parity Checking

When optional parity checking is enabled, the user system adds a parity bit to the complement of data bits and PI bit, if any. Parity checker U2/U20 monitors the odd/even content of the character bits along with the parity bit, and qualified PI bit TPI. If the content is different from that specified by odd/even parity selection signal PARITY O*/E, two signals are generated: FF9* and PARITY ERROR. Signal FF9* enables space code generator U19, causing it to replace the erroneous character with a blank. Signal PARITY ERROR is transmitted as a status signal to the user. In addition, it is used to set fault generator flip-flop U13B. Note that signal FF9* is either set or reset once per character, whereas signal PARITY ERROR is reset once per line.

g. Clearing Data

The user system may transmit signal BUFFER CLEAR* at any time to reset all Interface CCA circuits. Signal BUFFER CLEAR* is gated into signal BCAD* when signal DEMAND is active. The BUFFER CLEAR* signal also sets buffer clear latch U30B to issue signal BUFFER CLEAR. Signal BUFFER CLEAR conditions latch FF2 to be reset, causing signal FF2 to go low. With signal FF2 low, signal WRITE* goes high, and line buffer loading is inhibited. Signal BCAD* resets address counter U36/U43A and parity checker U2/U20.

Another method used to clear the parallel interface circuitry is the use of signal LOAD BUFFER, sent by the Processor CCA via control latch U54. Signal LOAD BUFFER, when high, is processed by a pulse shaper to produce two signals: LD BUF PUL A* and LD BUF PUL B* (load buffer pulse A and B, respectively). These pulses, when active, clear the following circuitry:

- Address Counter U36/U43A
- Expanded Flip-flop U14A
- Condensed Flip-flop U14B
- Count Control U11B
- Fault Generator U13B
- DAVFU/PRINT Control U43B
- Line Control U6B

When signal LOAD BUFFER goes low, the following circuitry is cleared:

- FF1 Latch U13A
- Top Count Control U7/U12A/U34
- Buffer Control U12B
- Parity Checker U2/U20
- Demand Control U5B

h. TCVFU Operation

The TCVFU option allows vertical format data from a punched paper tape to be routed to the Processor CCA. Data is routed via the DB1-DB8 bus through bi-directional transceiver U23 and over the DBUF1-DBUF8 bus. Since there are 12 TCVFU data channels plus a TRRQ (Tape reader request) channel, the Processor CCA must read each TCVFU character in two steps. Lower TCVFU channel signals CH1-CH6, plus CH13, (representing a sprocket clock), and TRRQ (tape reader request) are routed through lower tape channel driver U25. Upper TCVFU signals CH7-CH12 are routed through upper tape channel driver U26. The Processor CCA utilizes chip select signals CS7* and CS4* to access TCVFU data. However, to transfer the TCVFU data from the tape reader to the Processor CCA, the printer operator must press the READ pushbutton located on the tape reader. This action sends the TRRQ signal to the Processor CCA via the DB1-DB8 bus, through bi-directional transceiver U23, and over the DBUF1-DBUF8 bus. The Processor CCA, in turn, activates signal ENRDR* (enable reader). Signal ENRDR* is routed to the TCVFU CCA to enable the TCVFU motor.

Each time the Processor CCA reads a TCVFU character off the tape, it stores it in the VFU portion of the line buffer within the Interface CCA. When all TCVFU characters have been read once and stored, the Processor CCA performs another complete read operation. This time, each character read off the tape is compared against the same character stored during the first read operation. If all characters compare, the TCVFU load operation is complete. If a mismatch occurs in at least one character portion, a third read operation is performed and compared against the contents of the VFU memory stored during the second read operation. If necessary, a fourth or fifth read operation is performed until two successive read operations match. If no comparison is obtained within five read operations, the TCVFU load operation is aborted and the number 10 is displayed on the optional status display.

Unlike the loading of DAVFU characters, the printer must be off line while loading TCVFU characters, and all handshaking operations are inactive.

4.4.2 Serial Interface CCA (Optional)

The Dataproducts Serial Interface CCA is designed to accept data from the user system in serial form, convert it to parallel form, and then to transfer the converted data to the Processor CCA. The following paragraphs describe the interface considerations between the Serial Interface CCA and the user system, the serial interface hardware, data management, and sequential operation.

a. Interface Considerations

Two types of serial data transmission can be accommodated by the Serial Interface CCA: RS232C, and 20 mA Current Loop. A selector switch within the Serial Interface CCA selects either type.

THEORY OF OPERATION

1. RS232C - In this type of serial interface, discrete voltage levels are used for transmitting data as well as for interface communication. A signal is ON or SPACING when its voltage level is more positive than +3V; a signal is OFF or MARKING when its voltage level is more negative than -3V. The data bits are low true.

2. 20-mA Current Loop - In this type of serial interface, data and communication signals are transmitted by means of two current loops: receive and transmit. The receive loop is made up of a two-wire (RXD+, RXD-) current source supplied by the user to the Serial Interface CCA. Within the Serial Interface CCA, the two wires of the receive current source are terminated in a current-sensing device.

The transmit current loop is controlled by the printer and terminated in a current-sensing device at the user end. Its purpose is to provide the user with printer status information. The presence of current in the transmit loop indicates that the printer is able to receive data. The absence of current in the transmit loop indicates that the printer is busy.

b. Interface Signals

Table 4-4 lists and defines the interface signals connected between the Serial Interface CCA and the user for both RS232C and current loop systems. Pin assignments are given for a standard 50-pin connector. Pin assignments for the optional 25-pin connector are given in Section VI of this manual.

TABLE 4-4. SERIAL INTERFACE 50-PIN AMP CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Definition
39	(AB)	Signal Ground - This conductor establishes the common ground reference potential for all interface circuits.
33	(AA)	N/C
22	(BB)	Received Data - This user-generated signal transmits all print, format and control code information to the printer. This signal will only be looked at when the following signals are in the ON condition: (1) Data Terminal Ready (2) Data Set Ready (Optional) (3) Received Line Signal Detector (Optional)

TABLE 4-4. SERIAL INTERFACE 50-PIN AMP CONNECTOR PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
7	(CD)	<p>Data Terminal Ready -DTR - This printer-generated signal indicates that the printer is able to receive data. This signal is on when:</p> <ol style="list-style-type: none"> (1) Printer power is on (2) No printer faults exist (3) Printer is on line (4) Print buffer is not full <p>If the DTR signal goes off due to a PAPER OUT condition, it is possible that valid data may still be stored in the printer buffer. In order to print the remaining data, paper must be reloaded and the on line mode re-entered via the ON LINE control panel switch. Any data remaining in the buffer will be printed and the printer will receive more data as soon as the DTR signal goes on.</p>
5, 3		<p>Busy - This printer-generated signal is used to send status to the user. BUSY will be in the on condition whenever:</p> <ol style="list-style-type: none"> (1) Data Terminal Ready is in the off condition. (2) The print buffer is more than 3/4 full. <p>Data loading can continue after the BUSY signal goes active; however, any data transmitted after the buffer is full will not be stored in the printer and the DTR signal will go off.</p> <p>Data Loading can continue after the BUSY signal goes active; however, any data transmitted after the buffer is full will not be stored in the printer and the DTR signal will go off.</p>
27	(RxD+)	<p>Receive Data Plus - This user-generated signal transmits all print and control code information to the printer. This pin is positive with respect to (RxD-) when loop current is flowing (marking). This signal also indicates the status of the user equipment. Current is to be maintained in the loop, except while data is being transmitted, to indicate that the user equipment is in a ready condition. The absence of loop current for the period of one full transmission character will be interpreted by the printer as BREAK, indicating that the user equipment is not in a ready condition.</p>

TABLE 4-4. SERIAL INTERFACE 50 PIN AMP CONNECTOR PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
11	(RxD-)	Receive Data Minus - This signal is the current loop return for Receive Data.
20	(TxD+)	<p>Transmit Data Plus - This printer-generated signal indicates that the printer is able to receive data. Current is allowed to flow in the transmit loop when:</p> <ol style="list-style-type: none"> (1) Printer power is on (2) No printer fault exists (3) Printer has been placed on line (4) Print buffer is not full (5) Printer is not BUSY <p>This pin is positive with respect to (TxD-) when loop current is flowing ("READY").</p>
4	(TxD-)	Transmit Data Minus - This signal is the current loop return for Transmit Data.
6	(CC)	Data Set Ready - This user-generated signal indicates the status of the user equipment. The off condition of the DSR signal indicates that the printer must disregard signals on the other interface lines. The on condition indicates that the user equipment is in a ready condition.
23	(CA)	Request to Send - This printer-generated signal is held in the off condition to maintain the printer in the receive-only mode.
8	(CF)	Received Line Signal Detector - This user-generated signal, when in the on condition, indicates that the data communication equipment is receiving a signal (from the signal source) which meets its suitability criteria. These criteria are established by the data communication equipment manufacturer.
9	(CB)	Clear to Send - Not implemented.
21	(BA)	Transmitted Data - Not implemented.
24	(CE)	Ring Indicator - Not implemented.

c. Hardware Description (Figure 4-11)

Figure 4-11 is a block diagram of the circuits which implement the Serial Interface CCA, including microprocessor chip U3, USART chip U26, input buffer U14-U4, print buffer U29-U30, and associated devices and logic circuits. The Serial Interface CCA performs three main functions:

1. Converts serial data of either the RS232C or Current Loop type into parallel form.
2. Processes and stores the converted data, and upon request, transfers it to the Processor CCA.
3. Channels, but does not process, data from the optional TCVFU reader and the option header to the Processor CCA.

1. Control - Operation of the Serial Interface CCA is under control of two processors: internal, and external. The internal processor, hereafter referred to as the interface processor, is comprised of microprocessor chip U3, system controller chip U25, and clock generator chip U2. The external processor, hereafter referred to as the print processor, in general refers to the Processor CCA.

Each processor has an 8-bit data bus, an 16-bit address bus, and memory-write and memory-read control signals. Each 16-bit address bus is used to select a device from the complement of input/output devices connected to it, and where applicable, to specify the location within the selected device. The 8-bit data bus throughputs data between the applicable processor and the selected device. The memory-write and memory-read signals specify the direction of the data flow.

For example, when the print processor intends to transmit data to one of the devices within the Serial Interface CCA, it first places data on bus DBUF1-DBUF8. Then, it activates control signal MEMW, deactivates control signal MEMR, and places the address of the applicable device on address bus ADR0*-ADR15*. The procedure is similar when routing data from the Serial Interface CCA to the print processor, except that read control signal MEMR is activated, and write control signal MEMW is deactivated. Note that, when the print processor addresses the Serial Interface CCA (or any Interface CCA), address bit ADR15* must always be active.

THEORY OF OPERATION

Channeling data internally between the Interface Processor and one of the devices connected to it involves internal data bus D1-D8, internal address bus A0-A15, and internal read/write control signals IMEMR* and IMEMW*, with print processor address bit ADR15* inactive.

Table 4-5 lists the data bus, address bus, and control signals associated with each processor.

TABLE 4-5. PROCESSOR I/O AND CONTROL SIGNALS

Processor	Data Signal	Address Signal	Control Signal
Interface (Internal)	D1 - D8	A0 - A15	IMEMW IMEMR
Print (External)	DBUF1 - DBUF8	ADR0* - ADR9* ADR11* - ADR15* (ADR10* not used)	MEMW* MEMR*



THEORY OF OPERATION

From the standpoint of control, the complement of devices within the Serial Interface CCA may be divided into three groups. One group of devices is under the exclusive control of the interface processor, while the second group of devices is under the exclusive control of the print processor. The third group of devices is accessible to either processor on a time-shared basis. Device control is effected by means of two sets of chip-select signals developed from the five (or six) most significant address bits of each processor. Chip select signals CS3* - CS8* and CS12* are generated by external address decoder U34 from print processor address bits ADR11* - ADR15*. Similarly, chip select signals ICS1* - ICS10* and ICS16* are generated by internal address decoder U1 from interface processor address bits A11 - A15.

Another internal address bit, A10, is selectively used to distinguish between two devices that share a common chip select signal. External chip-select signals are listed in table 4-3. Signal CS12 is generated within the Serial Interface CCA by ORing CS1 with CS2.

Table 4-6 lists the internal chip select signals and describes their functions.

TABLE 4-6. INTERNAL CHIP SELECT SIGNALS

Signal	Binary Address						Function
	A15	A14	A13	A12	A11	A10	
ICS1A*	0	0	0	0	0	0	Select Program ROM MEM1
ICS1B*	0	0	0	0	0	1	Select Program ROM MEM2
ICS3*	0	0	0	1	0	X	Select I/F Control Latch U16
ICS4*	0	0	0	1	1	X	Select I/F Info. Latch U17
ICS5A*	0	0	1	0	0	0	Select Input Buffer U14, U4
ICS5B*	0	0	1	0	0	1	Select Optional RAM U15, U5
ICS6*	0	0	1	0	1	X	Select Scratch Pad U12, U13
ICS7*	0	0	1	1	0	X	Select Output Latch U27
ICS8*	0	0	1	1	1	X	Select Input Port U8
ICS9*	0	1	0	0	0	X	Select Print Buffer U29, U30 for internal write, together with internal buffer address driver U28, U45.
ICS10*	0	1	0	0	1	X	Select Mode Status Port U7
ICS16*	0	1	1	1	1	X	Select USART U26
X = Don't care condition							*Active When Low.

2. Data Bus Structure and Device Description - There are a total of three data buses within the Serial Interface CCA: DBUF1 - DBUF8, DB1 - DB8, and D1 - D8. Bus DBUF1 - DBUF8 channels data between the Serial Interface CCA and the Processor CCA. Three devices connect to bus DBUF1-DBUF8: interface information latch U17, interface control latch U16, and bi-directional driver U18. Latch U17 stores status information supplied by the Serial Interface CCA from data bus D1 - D8, under control of internal chip-select signal ICS4 along with IMEMW. The contents of U17 are periodically sampled by the Processor CCA under control of external chip-select signal CS6.

Latch U16 stores status information supplied by the Processor CCA under control of external chip-select signal CS3 along with MEMW. The contents of U16 are periodically sampled by the interface processor under control of internal chip-select signal ICS3.

Bi-directional driver U18 serves as the bi-directional port between the Processor CCA and the Serial Interface CCA. With the exception of status information, which is channelled through U16 and U17, all other information is routed to data bus DB1 - DB8 through U18, under control of the Processor CCA. The expression $\text{MEM W/R} \cdot \text{ADR15} \cdot \text{CS3}^* \cdot \text{CS6}^*$ implies that U18 is selected any time the Processor CCA performs a memory write or read from the Serial Interface CCA (ADR15), as long as CS3 and CS6 are inactive. Signal MEMW* controls the direction of data flow. When MEMW* is low, data flows from the Processor CCA to the Serial Interface CCA. When MEMW* is high, data flows from the Serial Interface CCA to the Processor CCA.

Data routed through U18 includes the following:

- (a) TCVFU lower channels through driver U21 to the Processor CCA under control of external chip-select signal CS7.
- (b) TCVFU upper channels through driver U20 under control of external chip-select signal CS4.
- (c) Option header data through driver U19, under control of external chip-select signal CS8.
- (d) Print or DAVFU data from the print buffer U29, U30 to the Processor CCA, under control of external chip-select signal CS12 along with MEMW/R. Note that when CS12 is active, the 10-bit print buffer address is supplied by the external address driver U31, U45, and U46.
- (e) Character validation data from the Processor CCA, written into the print buffer under control of external chip-select signal CS12, along with MEMW/R. As in the case described in (d) above, buffer address is supplied from U31, U45, U46 under control of CS12.
- (f) Print buffer address pointer, from location 0 of print buffer U29-U30, to the Processor CCA, under control of external chip-select signal CS12, along with MEMW/R. Buffer address 0 is supplied by the external address driver U32, U45, and U46.

THEORY OF OPERATION

Bus DB1 - DB8 channels data between devices U19, U20, U21, U29-U30 and bus DBUF1 - DBUF8 through bi-directional driver U18. In addition, bus DB1 - DB8 channels print and DAVFU data from bus D1-D8 through either U6 or MEM3 to the print buffer as follows:

Assume that the interface processor intends to write a print character at a certain location in print buffer U29-U30 and that the code conversion option is disabled. To do this, the interface processor places the ASCII-coded print character on bus D1-D8, specifies the character location on internal address bus A0 - A9, and activates internal chip-select signal ICS9 along with IMEMW. With ICS9 and IMEMW active, and with no code conversion, U6, U29-U30, and U28-U45 are chip-selected. Accordingly, the print character is routed from D1-D8 to DB1 - DB8, and written into U29-U30 at the location specified by internal address driver U28-U45. Note that the interface processor can only write into print buffer U29-U30 but cannot read from it. With code conversion enabled, the data path is similar to that described above, with MEM3 replacing U6. Device MEM3, when selected, converts the coded character of D1-D8 into an equivalent ASCII-coded character and places it on bus DB1 - DB8.

Bus D1-D8 serves as the bi-directional data path between the interface processor and the various memory and I/O devices connected to it. The function of each device is listed below.

(1) Input Port U8 - When selected by ICS8, this buffered port reads and inverts the state of the DAVFU ENABLE, and TCVFU ENABLE lines supplied by the option header. Bit designations are as follows:

MSB	D8	RESET
	D7	-
	D6	-
	D5	-
	D4	RESET DELAYED
	D3	DAVFU ENABLE*
	D2	TCVFU ENABLE*
LSB	D1	-

(2) Output Port U27 - This latched port stores various conditions of the Serial Interface CCA. It is updated by the interface processor with ICS7 • IMEMW. Bit designations are as follows:

MSB	D8	USART and BAUD rate generator reset
	D7	-
	D6	-
	D5	-
	D4	-
	D3	-
	D2	RLSD DLY RST
LSB	D1	BUSY*

(3) Scratch Pad U12-U13 - This random access memory stores various flags, counters, status words, and pointers. It is selected by ICS6 on the interface processor and is mapped as shown in table 4-7.

TABLE 4-7. SCRATCH PAD MEMORY MAP

Location (Hex)	Contents
2800	OPST (Output Port Status)
2801	RBFLAG (Reset Busy Flag)
2802	LTFLAG (Line Transfer Flag)
2804	HLFLAG (Halt Flag)
2805	BSFLAG (Busy Flag)
2806	CMNDST (USART Command Word Status)
2807	LLCNT (Lines Loaded Counter)
2808	BLCNT (Buffer Length Counter)
2809	BOFLAG (Busy Off Line Flag)
280A	HALTPT (Halt Pointer, LSB)
280B	HALTA (Halt Pointer, MSB)
280C	BUSYPT (Busy Pointer, LSB)
280D	BUSYA (Busy Pointer, MSB)
280E	BUFTOP (Input Buffer Top + 1, LSB)
280F	BUFTPA (Input Bufer Top - 1, MSB)
2810	HLCNT (Halt Counter)
2811	COUNT1 (Counter #1)
2812	COUNT2 (Counter #2)
2813	TRLNST (Transfer Line Status Word)
2814	PTBST (Port B Status)
2815	DBLCNT (DAVFU Buffer Length Cntr., LSB)
2816	DBLCTA (DAVFU Buffer Length Cntr., MSB)
2817	DABPT (DAVFU Buffer Pointer, LSB)

TABLE 4-7. SCRATCH PAD MEMORY MAP (Contd)

Location (Hex)	Contents
2818	DABPTA (DAVFU Buffer Pointer, MSB)
2819	DAFLAG (DAVFU FLAG)
281A	DAFLT (DAVFU Fault Flag)
281B	PBTAS (PBPT Temp. Store, LSB)
281C	PBTASA (PBPT Temp. Store, LSB)

(4) Input Buffer U14-U4-This random access memory serves as a temporary storage device for all print and control characters supplied by the user system and converted by USART chip U26. It is accessed under control of signal ICS5 when A10 is inactive. Input buffer detailed information, including data structure, is given in paragraph 4.4.2, subparagraph c.

(5) Program PROM MEM1-MEM2 - PROMs MEM1 and MEM2 store the main program for the interface processor and are accessed under control of internal chip-select signals ICS1A and ICS1B.

(6) Optional RAM U15-U5 - This device is an optional extension of input buffer U14-U4, under control of signal ICS5 with bit A10 active.

(7) Mode Status Port U7 - This device defines the operating parameters of the USART chip, such as number of stop bits, type of parity, if any, character length, and BAUD rate. Input to this device is supplied in part by the option configuration header and selected in part by parameter switches within the Serial Interface CCA. It is accessed under control of internal chip-select signal ICS10, and has the following bit assignments:

MSB	D8	} Number of Stop Bits	D8	0	0	1	1
	D7		D7	0	1	0	1
			Stop Bits	X	1	1½	2
	D6	Even Parity					
	D5	Parity Enable					
	D4	} Character Length	D4	0	0	1	1
	D3		D3	0	1	0	1
			No. Bits	5	6	7	8

LSB	D2	} Baud Rate	D2	0	0	1	1
	D1		D1	0	1	0	1
			Factor	SYNC	X1	X16	X64

(8) USART Chip U26 - In its application as a component of the Serial Interface CCA, USART chip U26 is used as an asynchronous receiver. Operating under control of internal chip-select signal ICS16, along with IMEMW and IMEMR, it converts the serial bit stream into parallel characters, inserting or deleting bits as required by the communications technique used. In addition to converting serial data into parallel form, U26 tests each character for parity (if applicable), overrun, and frame errors. If an error condition is detected, it is reported when interrogated by the interface processor. Inputs to U26 include signals REC DATA, REC CLOCK, and 2MHZ CLOCK. Signal REC DATA is a gated version of the serial data stream supplied by the user system and processed by the interface control circuits. Signal REC CLOCK is supplied by the BAUD rate generator, and is used to synchronize U26 with the BAUD rate of the serial data stream. Signal 2mHz serves as a time base for internal device timing. Output signal DTR indicates that the printer is able to receive data.

Communications between the USART chip and the interface processor are performed over data bus D1-D8 under control of signals C/D*, RD*, WR* in one of three modes, as follows:

(1) Data Transfer Mode: C/D* = 0, RD* = 0, WR* = 1

LSB:	D1	} Parallel data word transferred from USART to the interface processor
	D2	
	D3	
	D4	
	D5	
	D6	
	D7	
MSB:	D8	

(2) Status Mode: C/D* = 1, RD* = 0, WR* = 1

LSB:	D1	= Transmitter Ready	} Status word from USART to the interface processor
	D2	= Receiver Ready	
	D3	= Transmitter Empty	
	D4	= Parity Error	
	D5	= Overrun Error	
	D6	= Framing Error	
	D7	= Sync Detect	
MSB:	D8	= Data Set Ready	

THEORY OF OPERATION

(3) Command Mode: C/D* = 1, RD* = 1, WR* = 0

LSB	D1 = Transmit Enable	} Command word from interface processor to USART
	D2 = Data Terminal Ready	
	D3 = Receive Enable	
	D4 = Send Break Character	
	D5 = Error Reset	
	D6 = Request To Send	
	D7 = Internal Reset	
MSB	D8 = Sync	

(9) BAUD Rate Generator U36-U35-U51 - This circuit group supplies the REC CLOCK signal to USART chip U26. Input to the BAUD rate generator is the 18-mHz clock supplied by the interface processor. With BAUD rate select switch S3 set to the desired BAUD rate, the frequency of the output REC CLOCK is 16 times the expected BAUD rate of the serial data.

(10) Interface Control - This circuit group controls communication and data flow between the user system and the USART chip U26. The user system may be either the RS232C or 20 mA current loop type. With either type of system, the interface control presents a uniform interface to USART chip U26.

The main output from the interface control to the USART chip U26 is serial data signal REC DATA. This signal is derived either from the RxD input signal of the RS232 type interface, or from the current variation in the RxD+/RxD- receive loop, as applicable. Output to the RS232C interface includes signals DTR and BUSY. Signal DTR is derived from DTR* supplied by the USART chip U26. Signal BUSY is derived from BUSY* obtained from output port U27. When the interface is a 20-mA current loop type, the TxD+/TxD- transmit loop is used to transmit the BUSY status; a BUSY condition is signified by an absence of current flow in the TxD+/TxD- loop.

3. Data Management (Figure 4-11)

Two buffer memories are incorporated in the Serial Interface CCA: input buffer U14/U4, and print buffer U29/U30. The input buffer stores, in a circular fashion, all print and control characters received from the user system, line after line. Upon request by the print processor, one complete line is transferred to the print buffer, one character at a time. When the transfer is completed, the print processor examines the contents of the print buffer and eventually prints it. Line transfer is initiated when the print processor sets the load buffer signal. This signal is latched in bit D3 of the interface control latch U16. When the transfer is completed, the interface processor informs the print processor by latching signal BUFFER FULL in bit D1 of the interface information latch U17. In response, the print processor resets the load buffer signal and then the interface processor resets the BUFFER FULL signal. Note that the load buffer and buffer full signals operate in a handshaking fashion.

Therefore, there are two major operations taking place in the Serial Interface CCA: loading the input buffer with user-supplied data, and transferring complete lines to the print buffer. A third operation, involving DAVFU data, is treated in a special way and is discussed in paragraph 4.3.2.

Note that the transfer of data from the print buffer to the print processor is an operation involving the print processor but not the interface processor.

To keep track of the buffer status and preserve the integrity of the data, the interface processor maintains a group of pointers, counters, and flags in designated locations within the scratchpad buffer U12/U13. Following initialization, all pointers are reset to the status shown in figure 4-12. The main loop pointer (MLPT) points to the location where the next user-supplied character is to be loaded in the input buffer, in this case, location 0. Start transfer pointer (STPT) points to the first character location of the next complete line to be transferred to the print buffer, in this case location 0. Starting from zero, the line length counter (LLCT) increments with each complete line received from the user, and decrements with each complete line transferred to the print buffer. The print buffer pointer (PBPT) points to the location in the print buffer where the next character is to be stored and increments with each transferred character. BUSY pointer (BUSYPT) points to the address where the input buffer is 3/4 full. The halt pointer (HALPT) points to the top location of the input buffer.

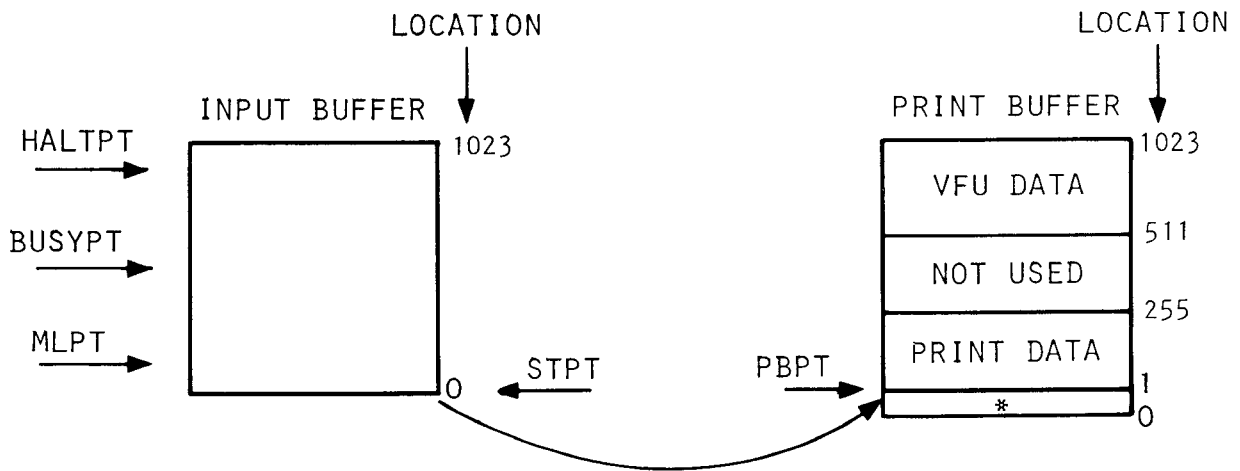
(a) USART to Input Buffer Data Transfer - Figure 4-13 shows the data structure of the input buffer. When a character is received from the USART, it is stored at the location pointed to by main loop pointer MLPT. Since MLPT initially always points to the start of the buffer, the first print character received from the USART is always stored at the start or bottom of the buffer. With each character received from the USART, MLPT is incremented.

Subsequent print characters are treated the same way, each stored sequentially in the next highest location. Receipt of a control character (paper motion) marks the end of that print line. The control character is stored above the last print character, MLPT is incremented by one, and a dummy character ($1F_H$) is stored one location above the control character. The dummy character serves as a demarcation for each print line. Next, a transfer line status code is stored one location above the control character. The transfer line status code contains the horizontal pitch (normal, condensed, or expanded) of the current line. Transfer line status information is derived from a coded character supplied by the user at any time, but it is not loaded in the input buffer until the line has been terminated. Finally, the lines loaded counter (LLCNT) is incremented to indicate that one complete line is ready to be transferred to the print buffer.

To circulate the input buffer, the main loop pointer is continually compared with the top of buffer pointer (BUFTOP). If BUFTOP is one location higher than the physical top of the input buffer, the main loop pointer is returned to the physical bottom address of the input buffer.

To avoid overfilling the input buffer, the main loop pointer is continually compared to the busy pointer BUSYTP. When the two are equal, indicating that the input buffer is 3/4 full, a BUSY signal is sent to the user system. Under these circumstances, the user is allowed to complete transmission of the current line, then stop until the BUSY condition is lifted. If the user ignores BUSY and keeps transmitting, the input buffer will eventually fill

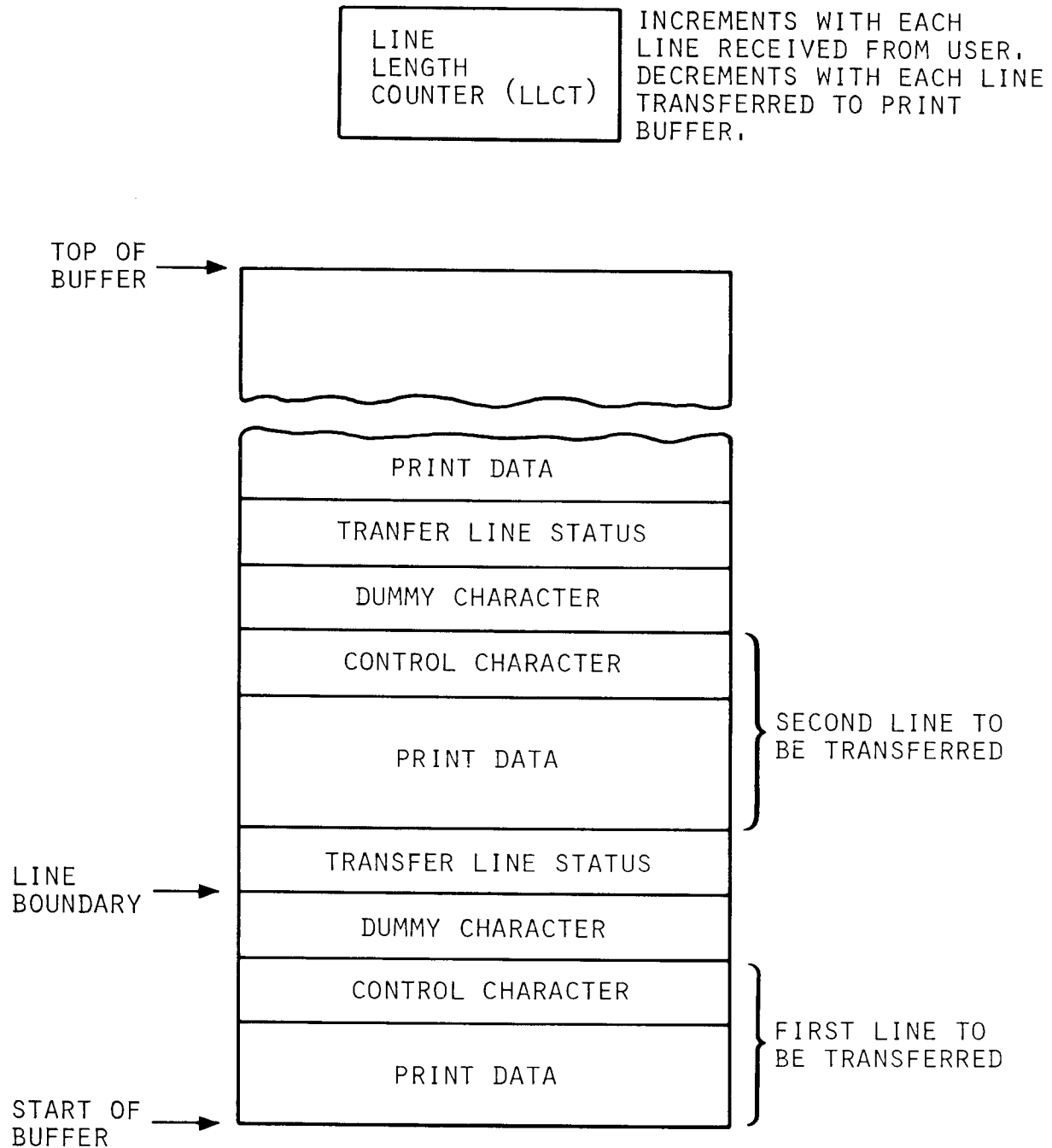
THEORY OF OPERATION



* LOCATION 0 IS RESERVED FOR LOCATION ADDRESS OF THE CONTROL CHARACTER

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Figure 4-12. Buffer Pointers



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Figure 4-13. Input Buffer Structure

THEORY OF OPERATION

up, and the HALT flag will be set. With the HALT flag set, the interface control circuit will disable Data Terminal Ready signal DTR, and any further data will be ignored until the BUSY condition is lifted. The BUSY condition will be lifted when enough data has been transferred to the print buffer to make the input buffer less than 3/4 full.

(b) Input Buffer to Print Buffer - This operation involves the transfer of one line of data, character by character, from the input buffer to the print buffer. One line of data includes print data and control character, but not the dummy character or the transfer line status character. The source of the first character to be transferred is the location address pointed to by the select transfer pointer STPT. The destination of the first character to be transferred is the location address pointed to by the print buffer pointer PBPT. Both pointers are incremented with each transferred character.

The operation is initiated when the print processor sets control signal LOAD BUFFER in bit D1 of interface control latch U16. With bit D1 set, the transfer operation can start if the line length counter is greater than zero. Before a character is transferred, it is first compared with the dummy character. If it is not a dummy character, then it is stored in the designated location within the print buffer. Following transfer of each non-dummy character, the USART chip is interrogated. Interrogation of the USART chip involves testing for the presence of a newly assembled character, and if applicable, storing that character in the designated location within the input buffer.

When the dummy character is detected, the location address of the control character is stored in location 0 of the print buffer. Next, the contents of the transfer line status is examined to determine if the line pitch is expanded, condensed, or normal. This information, along with the BUFFER FULL signal, is sent via the interface information latch U17 to the print processor.

Each time a character is transferred to the print buffer, the memory space in the input buffer increases. Accordingly, the BUSYPT (input buffer 3/4 full) and HALTPT are incremented. When a complete line has been transferred to the print buffer, the conditions of the HALT flag (HLFLAG) and 3/4 BUSY flag (BSFLAG) are reexamined. If either flag is set, and the input buffer is no longer 3/4 full, both flags are reset, and the BUSY signal to the user system is deactivated.

In addition, when transferring characters from the input buffer to the print buffer, the input buffer pointers are checked against the value of BUFTOP. If either the start transfer pointer, BUSY pointer, or HALT pointer equals BUFTOP, it is reinitialized to the physical bottom of the input buffer. This allows the input buffer to operate in a circular fashion.

(c) DAVFU Data Transfer - Unlike print data, DAVFU data is not loaded first in the input buffer, but is transferred directly from the USART chip to the VFU portion of the print buffer. When a DAVFU start code is received, the BUSY signal to the user is activated and DTR is deactivated. Next, the contents of the input buffer, if any, are transferred to the print buffer.

Once the input buffer is completely empty, DTR is activated again and BUSY is deactivated. Upon receipt of a LOAD BUFFER signal from the print processor, loading of DAVFU data may then be resumed.

DAVFU loading operations are terminated upon one of the following conditions:

(1) When a DAVFU load error is detected. Under this condition, the interface processor will transmit a DAVFU FAULT signal on bit D3 of the interface information latch U17 to the print processor.

(2) When a DAVFU start character is received from the user system. This condition will restart the DAVFU load operation.

(3) When a DAVFU stop character is received and no error conditions exist. Following a successful DAVFU load operation, the location address of the last DAVFU character is stored in location 0 of the print data portion of the print buffer.

(d) Sequential Operation - The following paragraphs describe, in simplified form, the sequence of events associated with the transfer of data from the USART chip through the input buffer to the print buffer. The discussion is divided into the following topics, each keyed to a flow diagram:

(1) Overall Operation

(2) Input Operation

(3) Print Data Transfer Operation

(4) DAVFU Data Transfer Operation

(1) Overall Operation (Figure 4-14) - Figure 4-14 is a general flow diagram of events associated with the operation of the Serial Interface CCA. Following initialization, the ON LINE signal is monitored; the serial interface will remain in this loop until the print processor enters the on-line state. When the ON LINE signal goes high, the serial interface returns an on line ACKNOWLEDGE signal to the print processor and clears BOFLAG (BUSY flag set when the processor goes off line). Next, the conditions of DAFLAG (set following receipt of a DAVFU start code) and BSFLAG (set when the input buffer is 3/4 full) are tested. If neither flag is set, the BUSY signal to the user system is reset and DTR (Data Terminal Ready) is enabled.

NOTE

The serial interface will go BUSY and activate the BUSY signal to the user under any of the following conditions:

- (1) When the print processor goes off line, and will stay BUSY until the print processor goes on line again.

THEORY OF OPERATION

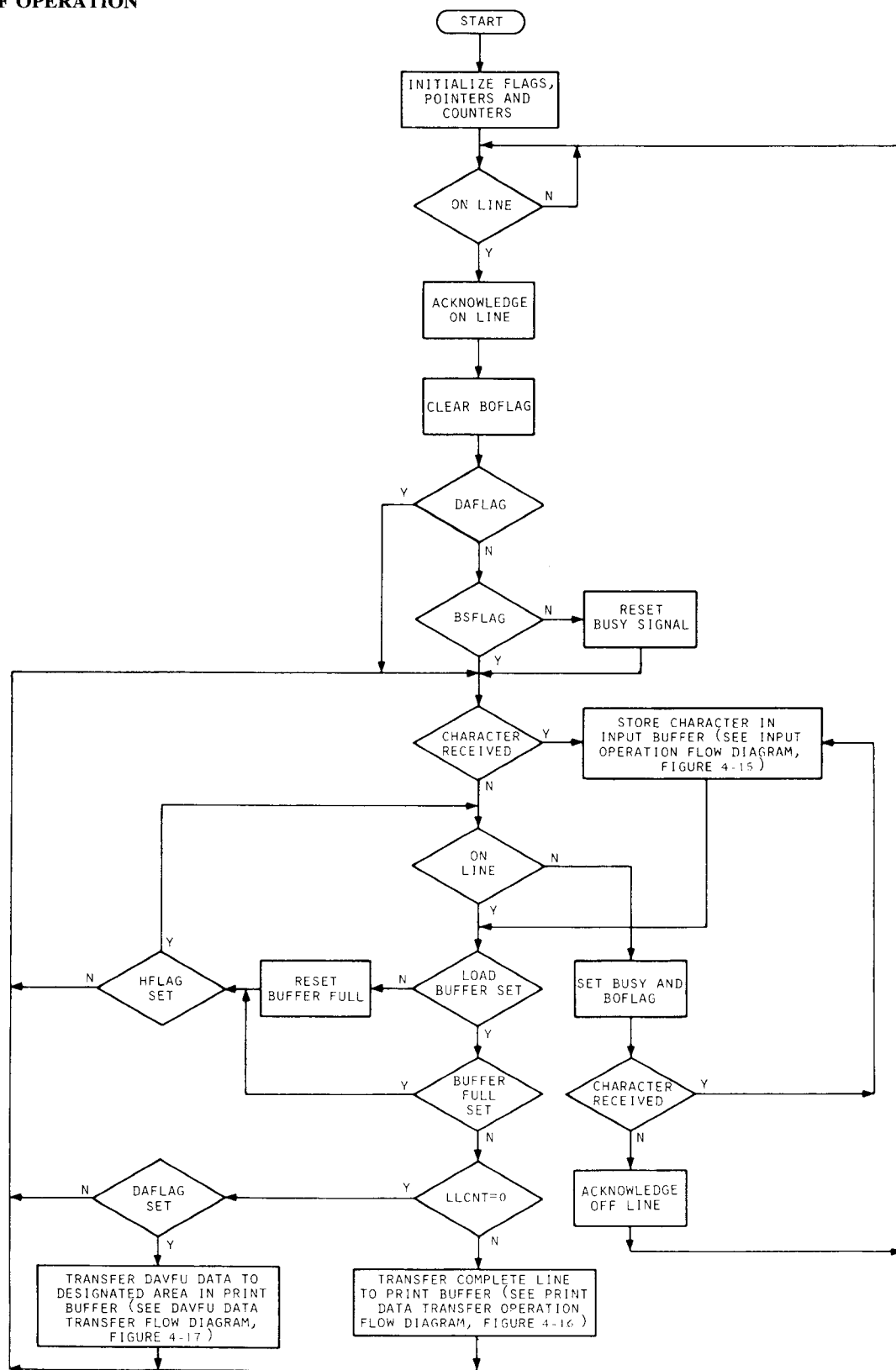


Figure 4-14. Serial Interface Overall Operation Flow Diagram

- (2) When the input buffer is 3/4 full, and will stay BUSY until enough data has been transferred to the print buffer.
- (3) When a DAVFU start code has been received. The serial interface will stay BUSY long enough to allow transfer of all print data from the input buffer.

Next, the USART chip is examined for the presence of an assembled character. If a character is found to be present, it is stored in the input buffer as detailed in paragraph (2) below. Otherwise, the ON LINE signal is monitored to verify that the print processor is still on line. Assuming that the ON LINE signal is still high, and that the print processor has set the LOAD BUFFER signal, the contents of the line loaded counter LLCNT is examined. If LLCNT does not equal zero, one line of data is transferred from the input buffer to the print buffer as detailed in paragraph (3) below.

If the ON LINE signal is low, the BUSY signal to the user is activated, and BOFLAG (BUSY due to off line) is set. The BUSY signal informs the user to complete loading the current line, and then wait until the BUSY condition has been lifted. Next, the USART chip is tested for the presence of an assembled character. If a character is present, it is loaded in the input buffer as detailed in paragraph (2) below. This operation is repeated several times until the user has completed transmitting the current line. At that time, the off-line signal is acknowledged, and the sequence returns to the on line signal monitoring loop.

Unlike print data, DAVFU data is transferred directly from the USART chip to the VFU portion of the print buffer. However, before DAVFU data can be serviced, the input buffer must be empty. To accomplish this, the contents of the input buffer are transferred, character by character, line after line, and printed. During this time, the BUSY signal is active and no characters are accepted from the user system. Each time a line is transferred from the input buffer to the print buffer, LLCNT is decremented by one. Eventually LLCNT will equal zero and the last line will be printed, allowing the serial interface to enter the DAVFU data transfer operation.

If, as a result of an input operation, HLFLAG is found to be in the set state, no input operation can take place. Instead, the transfer operation is entered as many times as necessary until enough data has been transferred to allow HLFLAG to be reset.

(2) Input Operation (Figure 4-15) - During each input operation, one character is transferred from the USART to the input buffer. Each character is tested for load errors, control codes, and DAVFU start codes. No character loading can take place if the input buffer is already filled to capacity.

THEORY OF OPERATION

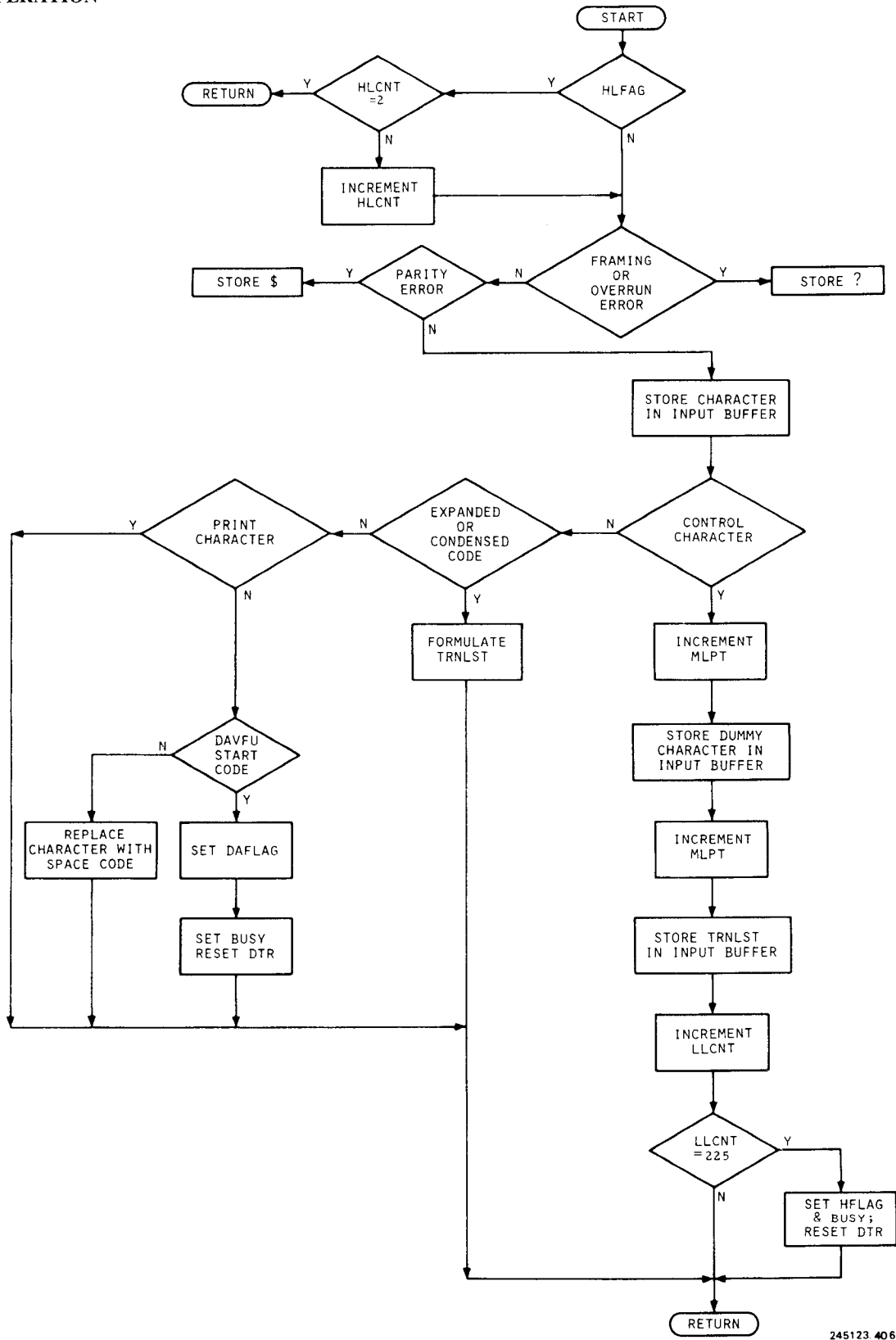


Figure 4-15. Input Operation

At the start of the input operation, the state of HALT Flag HLFLAG is examined. If set, HLCNT is tested. If HLCNT equals 2, the input operation is exited and returned to the overall operation. Otherwise, HLCNT is incremented by one. If HLFLAG is not set, HLCNT is neither examined nor incremented.

NOTE

HLFLAG is set when all but two locations of the input buffer are full.

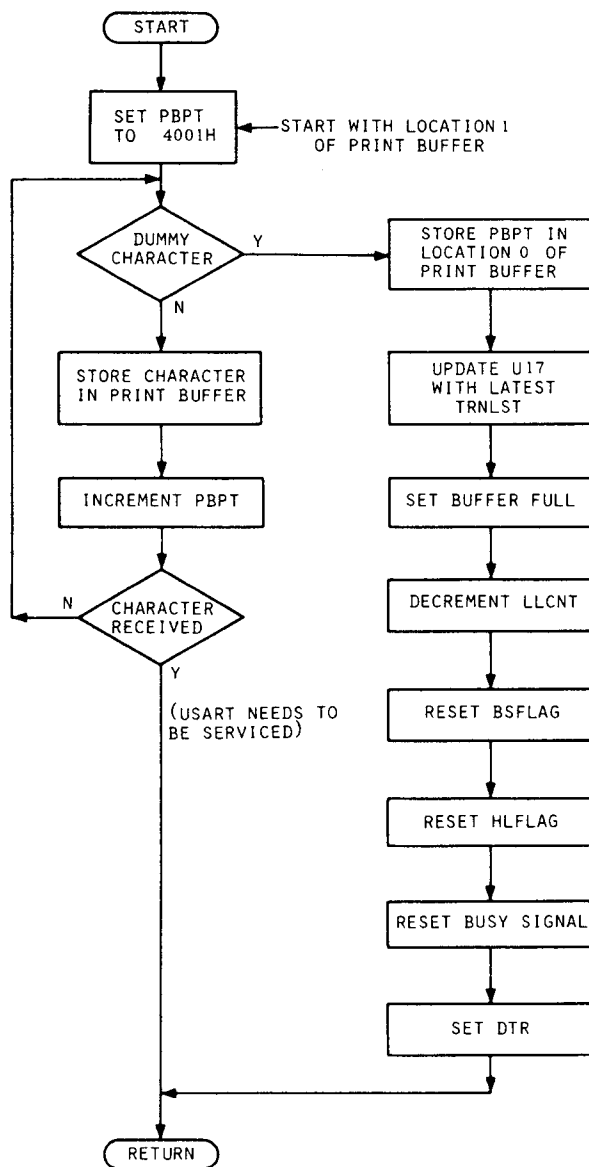
Next, the character supplied by the USART is tested for framing, overrun, and parity errors. If a framing or overrun is detected, a question mark (?) is stored. If a parity error is detected, a dollar sign (\$) is stored. Otherwise the character is stored unaltered in the input buffer and tested for the following:

- (aa) Print character.
- (bb) DAVFU start code. If present, DAFLAG and BUSY are set and DTR is reset.
- (cc) Control code. If present, the dummy character is stored above the control character, followed by TRNLST. After TRNLST has been stored, LLCNT is incremented and tested. If less than 255, the input operation returns to the overall operation. If LLCNT equals 255, indicating that the input buffer is now filled to capacity, HFLAG and BUSY are set, and DTR is reset before the input operation sequence is exited.
- (dd) Condensed or expanded code. If present, TRNLST is formulated accordingly.
- (ee) If none of the above is present, the character currently stored in the input buffer is replaced by a space code.

(3) Print Data Transfer Operation (Figure 4-16) -

This operation transfers complete lines of print data, character by character, to the print buffer. Starting with location 1, characters are transferred one at a time in a continuous loop until one of two conditions are encountered:

- (aa) The USART needs to be serviced. Under this condition, the print data transfer operation is exited, and eventually the input operation is entered. During the input operation, the USART character is loaded in the input buffer, and then the print data transfer operation is reentered.



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Figure 4-16. Print Data Transfer Operation Flow Diagram

- (bb) A dummy character is detected indicating the end of the current line. Under this condition, the location address of the previous character (control character) is stored in location zero of the print buffer.

Next, interface information latch U17 is updated with the latest TRNLST status (condensed, expanded), and LLCNT is decremented. Finally, BUSY and HLTFLLAG are reset, and DTR is set.

(4) DAVFU Data Transfer Operation (Figure 4-17) -

During this operation, DAVFU data is transferred directly from the USART to the VFU area of the print buffer. Loading will proceed sequentially until one of the following occurs:

- (aa) Receipt of another DAVFU start code.
- (bb) DAVFU fault.
- (cc) Receipt of a DAVFU stop code.

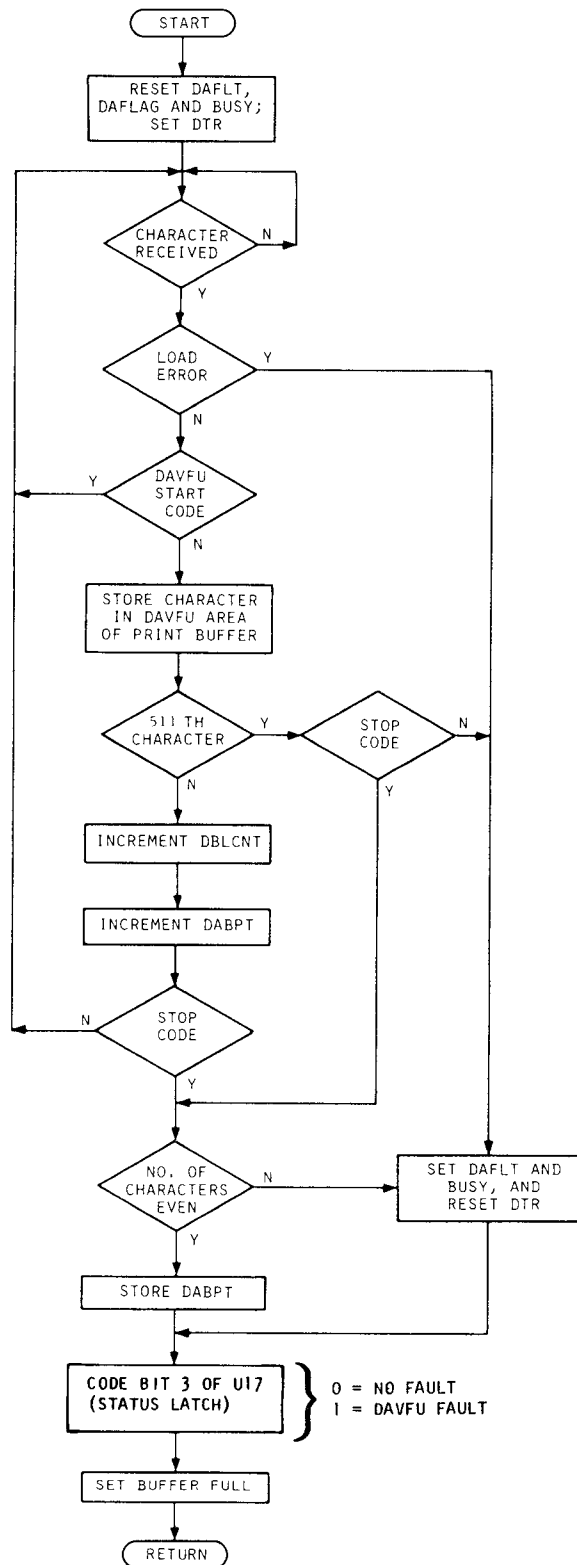
As shown in figure 4-17, the DAVFU fault flag, DAVFU Flag and BUSY signal are cleared, and DTR is set. Next, the operation enters a loop until the USART indicates that it has a character available for transfer. At that time, the character is tested for load error and DAVFU start code. Assuming that neither condition exists, the character is stored in the DAVFU area of the print buffer, in a location specified by the DAVFU buffer pointer DABPT. Next, the DAVFU character count is monitored for 511. Assuming that the count is less than 511, DAVFU character length counter DBLCNT and buffer pointer DABPT are incremented, and the character is tested for a DAVFU stop code. If the character is not a stop code, the operation returns to the USART monitoring loop until another character becomes available.

Eventually, after receipt of several characters, the user will transmit a DAVFU stop code. If the number of DAVFU characters is even, DABPT is stored in location 0 of the print buffer; DAVFU fault bit D3 is coded in U17, (since no fault has occurred, D3 is set to 0); and BUFFER FULL is set in bit D1 of U17.

DAVFU fault can occur under the following conditions:

- (aa) Character load error
- (bb) Number of characters equals 511, and no stop code was received.
- (cc) The total number of characters received, including the start and stop codes, is odd.

When a DAVFU fault occurs, DAFLT and BUSY are set, and DTR is reset. Then a DAVFU fault condition is reported to the print processor by setting bit D3 of U17 to one.



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Figure 4-17. DAVFU Data Transfer Flow Diagram

(e) Definition of Flags, Pointers and Counters - Table 4-8 is an alphabetical list of flags, pointers, and counters used by the interface processor to transfer data from the USART to the print processor.

TABLE 4-8. DEFINITION OF FLAGS, POINTERS AND COUNTERS

Item	Definition
BLCNT	Buffer Length Counter This counter records the number of characters loaded from the user to the Input Buffer for each line of data.
BOFLAG	Busy Off Line Flag This flag is set to distinguish between a 3/4 full busy condition and a busy off-line condition. It is set whenever the printer is put off-line. Once set, the BUSY signal will not get reset unless the printer is again placed on line.
BSFLAG	Busy Flag This flag is set when the Input Buffer is 3/4 full.
BUFTOP (LSB), BUFTPA (MSB)	Input Buffer Top + 1 This is the address of the top location of the Input Buffer + 1.
BUSYPT (LSB), BUSYA (MSB)	Busy Pointer This address pointer is 3/4 up the Input Buffer (with reference to the bottom of the next line to be transferred). It is used to set the Busy Flag when the Input Buffer is 3/4 full.
CMNDST	USART Command Word Status This records the last command word written to the USART.
DABPT (LSB), DABPTA (MSB)	DAVFU Buffer Pointer This address pointer points to the DAVFU portion of the Print Buffer.
DAFLAG	DAVFU Flag This flag is set when a DAVFU start code is received from the user.

TABLE 4-8. DEFINITION OF FLAGS, POINTERS AND COUNTERS
(Contd)

Item	Definition
DAFLT	<p>DAVFU Fault Flag</p> <p>This flag is set if:</p> <ol style="list-style-type: none"> 1. A DAVFU load error was detected. 2. DAVFU Buffer is overfilled. 3. An odd number of DAVFU characters has been loaded.
DBLCNT (LSB), DBLCTA (MSB)	<p>DAVFU Buffer Length Counter</p> <p>This counter indicates the number of characters input during the DAVFU Transfer Operation.</p>
HALTPT (LSB), HALTA (MSB)	<p>Halt Pointer</p> <p>This address pointer is two locations below the top of the Input Buffer. It is used to check when the Input Buffer is nearly full.</p>
HLCNT	<p>Halt Counter</p> <p>This counter indicates the number of characters (to a maximum of 2) that will be input to the Input Buffer after the HALTPT is reached.</p>
HLFLAG	<p>Halt Flag</p> <p>This flag is set when the Input Buffer is within two locations of being completely full.</p>
LLCNT	<p>Lines Loaded Counter</p> <p>This counter records the number of complete lines in the Input Buffer to be transferred to the Print Buffer.</p>
LTFLAG	<p>Line Transfer Flag</p> <p>This flag is set if a line transfer from the Input Buffer to the Print Buffer is in progress.</p>
MLPT	<p>Main Loop Pointer</p> <p>Used to point to the next empty location in the Input Buffer. It is incremented each time a legal character is loaded from the user.</p>

TABLE 4-8. DEFINITION OF FLAGS, POINTERS, AND COUNTERS
(Contd)

Item	Definition
OPTST	Output Port Status This records the last byte written to OPT (Output Port).
PBPT	Print Buffer Pointer Points to the location of the Print Buffer where the next character is to be loaded. It is incremented with each character transferred from the Input Buffer.
PBTAS (LSB), PBTASA (MSB)	Print Buffer Pointer Temp. Store The PBPT is stored here before the USART is interrogated.
PTBST)	Port B Status This records the last byte written to Port B.
RBFLAG	Reset Busy Flag Flag used as a reminder to reset the BUSY Signal and the BSFLAG. It is set when the buffer is no longer 3/4 full.
STPT	Start Transfer Pointer Points to the first character of the next line in the Input Buffer to be transferred to the Print Buffer. It is incremented as each character is transferred.
TRLNST	Transfer Line Status Word This byte contains those bits of Port B which are set uniquely for each input data line. Where: <div style="margin-left: 40px;"> Bit 7 = Expanded Code 6 = Condensed Code 4 = DAVFU/PRINT* 3 = DAVFU Fault 1 = Buffer Full </div>

4.4.3 DPC Centronics-Compatible Interface CCA (Option)

The DPC Centronics-Compatible Interface CCA presents the user system with an interface that is compatible with Centronics printers. As such, it accepts data in bit-parallel, character-serial form, using the DATA STROBE/ACKNOWLEDGE communications scheme. The following paragraphs describe the interface signals, interface timing, hardware, and sequential operation of the DPC Centronics-Compatible Interface.

a. Interface Signals

Table 4-9 lists and defines the signals connected between the user system and the DPC Centronics-Compatible Interface.

TABLE 4-9. DPC CENTRONICS-COMPATIBLE INTERFACE SIGNALS

Signal	Definition	Pin Number	
		P1	50-Pin Interface Connector
SLCT (SELECT)	A printer-generated signal which indicates that the printer has been selected. When the SLCT signal is active: (a) The ALARM light is off. (b) The printer operator has pressed the ON LINE switch, or an octal (021) has been received via the data bus. (c) The printer is ready to receive data.	19	21
SLCT RTN		20	5
ACKNLG*	A printer-generated signal which acknowledges that the printer has received a data word. If the data word produces a busy condition, the acknowledge signal will not be generated until the busy condition is reset.	15	23
ACKNLG RTN*		16	7
DATA STROBE*	A user-generated signal which defines when information on the data lines is stable and may be stored in the printer buffer.	37	38
DATA STROBE RTN*		38	37

TABLE 4-9. DPC CENTRONICS-COMPATIBLE INTERFACE SIGNALS
(Contd)

Signal	Definition	Pin Number	
		P1	50-Pin Interface Connector
BUSY	A printer-generated signal that the printer is unable to receive print or format data. A select code can be transmitted during a busy condition.	17	22
BUSY RTN		18	6
INPUT PRIME*	A user-generated signal that clears the printer buffer and initializes the interface logic. The input prime signal is asynchronous to the interface logic. This signal does not affect print or paper motion cycles.	43	31
INPUT PRIME RTN*		44	15
FAULT*	A printer-generated signal indicating that one of the following faults has occurred:	9	26
	(a) Printer is Out of Paper. (b) Shuttle is not moving. (c) Printer is not selected		
FAULT RTN*		10	10
OSCXT	A printer-generated signal that transmits a 100 kHz square wave to the user.	13	24
OSCXT RTN		14	8
PE	A printer-generated signal that indicates printer is Out of Paper.	11	25
PE RTN		12	9
PAPER INSTRUCTION (Optional)	This user-generated signal informs the printer that information on the data lines is to be treated as format data. This signal can only be used when the TCVFU or DAVFU option is installed; however, a data line can be terminated using the standard ASCII format codes (PAPER INSTRUCTION signal inactive) even though the TCVFU or DAVFU option is installed.	41	30

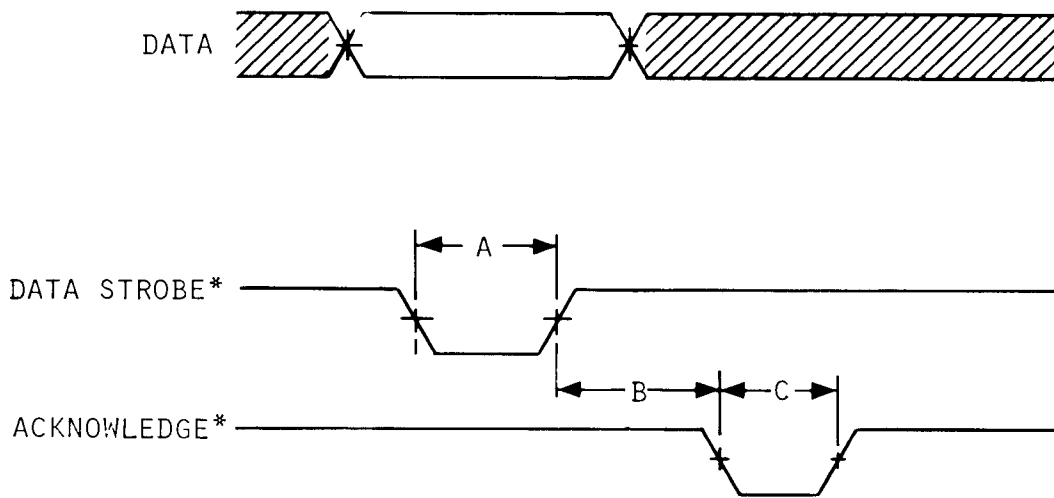
TABLE 4-9. DPC CENTRONICS-COMPATIBLE INTERFACE SIGNALS
(Contd)

Signal	Definition	Pin Number	
		P1	50-Pin Interface Connector
PAPER INSTRUCTION RTN		42	14
DATA 1	User Data	21	19
DATA 1 RTN		22	3
DATA 2	User Data	23	20
DATA 2 RTN		24	4
DATA 3	User Data	25	1
DATA 3 RTN		26	2
DATA 4	User Data	27	41
DATA 4 RTN		28	40
DATA 5	User Data	29	34
DATA 5 RTN		30	18
DATA 6	User Data	31	43
DATA 6 RTN		32	42
DATA 7	User Data	33	36
DATA 7 RTN		34	35
DATA 8	User Data	35	28
DATA 8 RTN		36	44

b. Interface Timing

Interface communication signals operate in the pulsed, rather than the handshaking mode. Once the DPC Centronics-Compatible Interface has been selected (see paragraph 4.4.3d) and no BUSY condition exists, it will communicate with the user as follows (see figure 4-18):

1. The user places data on the data lines and transmits a DATA STROBE* signal.
2. Sensing the DATA STROBE* signal, the DPC Centronics-Compatible Interface stores the data in the line buffer and sets a delay timer.
3. At the expiration of the delay time, the DPC Centronics-Compatible Interface returns an ACKNOWLEDGE* signal.
4. Sensing the ACKNOWLEDGE* signal, the user system can transmit another DATA STROBE signal.



TIME B IS THE ACKNOWLEDGE DELAY

STARRED SIGNAL NAMES SIGNIFY
ACTIVE LOW SIGNAL

$$A = 1.0 \mu\text{SEC. MAX.}$$

$$= 0.5 \mu\text{SEC. MIN.}$$

$$B = 7 \pm 1.0 \mu\text{SEC.}$$

$$C = 4 \pm 1.0 \mu\text{SEC.}$$

 = UNDEFINED AREA

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Figure 4-18. Data Transfer Timing Without Busy

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If the user transmits a character that causes the Interface CCA to enter the BUSY state (CR, DESELECT, or termination code), the interface communication sequence will be as follows (see figure 4-19):

1. The user system places a character on the data lines.
2. The user system transmits a DATA STROBE* signal.
3. Sensing the leading edge of the DATA STROBE* signal, the DPC Centronics-Compatible Interface decodes the character coded on the data lines.
4. After the character has been decoded, on the trailing edge of DATA STROBE*, the DPC Centronics-Compatible Interface enters the BUSY state.

NOTE

If the character received is CR, BUSY is entered on the leading edge of DATA STROBE*.

5. After a time delay, as determined by the type of character received, the DPC Centronics-Compatible Interface terminates the BUSY state and transmits an ACKNOWLEDGE* signal to the user.

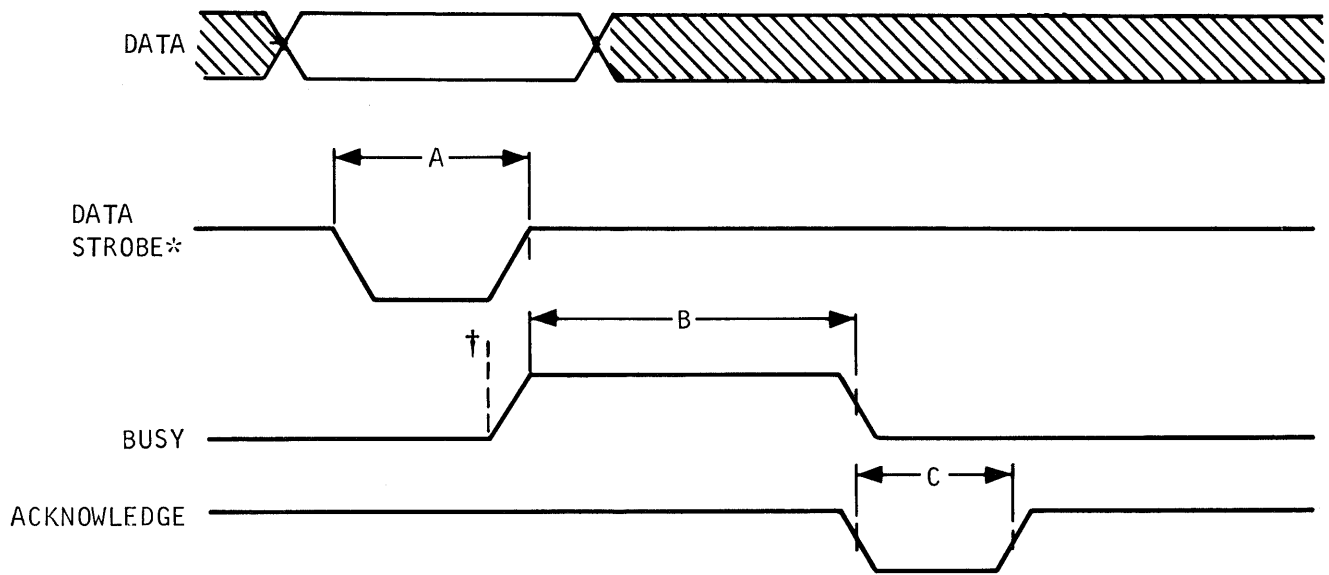
c. Interface Hardware Description (Figure 4-20)

Figure 4-20 is a simplified block diagram of the circuits that comprise the DPC Centronics-Compatible Interface. The following paragraphs describe the functions of the circuits and devices depicted.

1. Chip Select Decoder U50 - This device samples the five most significant bits of the Processor CCA address bus, and generates seven mutually exclusive chip select signals -- CS1 - CS4 and CS6 - CS8. The chip select signals are used to enable individual devices within the DPC Centronics-Compatible Interface. Refer to table 4-3 for the function of each chip select signal.

2. Interface Control Latch U54 - This device is connected to data bus DBUF1 - DBUF8, and forms the input half of the two-way communications path between the Processor CCA and the DPC Centronics-Compatible Interface. To latch information into U54, the Processor CCA turns on CS4, along with memory write signal MEMW. Bit designations are as follows:

LSB	DBUF1	= Load Buffer
	DBUF2	= Ready
	DBUF3	= On Line
	DBUF4	- -
	DBUF5	- -
	DBUF6	= LD (Error)
	DBUF7	= Condensed
MSB	DBUF8	= PE (Paper Empty)



A = 1.0 μ sec max, 0.5 μ sec min

B = Duration of BUSY as defined

C = 4.0 μ sec \pm 1 μ sec

RECEIVED DATA

1. CR w/o Auto Line
2. CR w/ Auto Line
3. Deselect Code
4. All Other Terminations

DURATION OF BUSY

- 7.0 μ sec \pm 1.0 μ sec
- Print & Paper Motion Cycles
- Until Printer is Selected
- Print & Paper Motion Cycles

STARRED SIGNAL NAMES SIGNIFY ACTIVE LOW SIGNALS

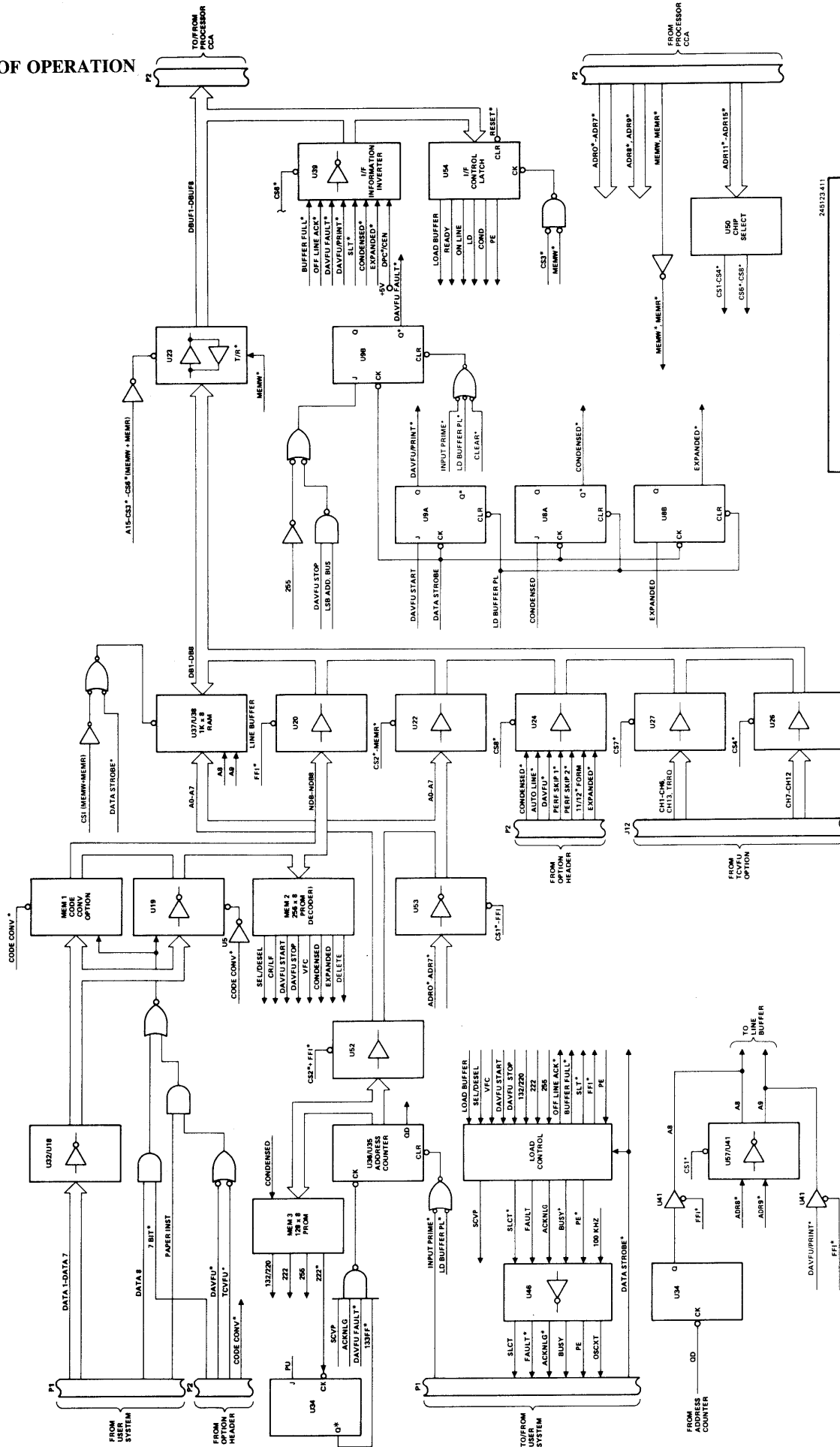
† START OF BUSY OCCURS ON TRAILING EDGE OF DATA STROBE* IN ALL CASES EXCEPT CR.
WHEN RECEIVED DATA IS CR, START OF BUSY OCCURS ON LEADING EDGE OF DATA STROBE*.

 = UNDEFINED AREA

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Figure 4-19. Data Transfer Timing With BUSY

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Figure 4-20. DPC Centronics-Compatible Interface CCA Block Diagram

3. Interface Information Inverter U39 - This device is connected to data bus DBUF1 - DBUF8, and forms the output half of the two-way communications path between the Processor CCA and the DPC Centronics-Compatible Interface. Since U39 has no storage capability, information is collected from different flip-flops within the DPC Centronics-Compatible Interface. To read the contents of U39, the Processor CCA turns on chip select signal CS3 along with memory read signal MEMR. Bit designations are as follows:

LSB	DBUF1	=	BUFFER FULL
	DBUF2	=	ON/OFF LINE Acknowledge
	DBUF3	=	DAVFU FAULT
	DBUF4	=	DAVFU/PRINT*
	DBUF5	=	SELECT
	DBUF6	=	CONDENSED
	DBUF7	=	EXPANDED
	DBUF8	=	DPC/CEN* (Always low in the DPC Centronics-Compatible Interface)

4. Bi-Directional Driver U23 - Connected between data buses DBUF1 - DBUF8 and DB1 - DB8, this device serves as the bi-directional data port between the Processor CCA and the DPC Centronics-Compatible Interface. The expression:

$$A15 \cdot CS3* \cdot CS6* \quad (MEMW + MEMR)$$

implies that U23 is enabled any time the Processor CCA performs a memory write or read to or from the DPC Centronics-Compatible Interface, provided that both CS3 and CS6 are inactive. As a result, U23 time-shares data bus DBUF1 - DBUF8 with U39 and U54.

5. Lower and Upper Tape Channel Control Drivers U27 and U26 - Together, these two devices route tape channel information from the optional TCVFU through U23 to the Processor CCA. Two memory read operations are required to transfer the full complement of TCVFU bits over the 8-bit DBUF1 - DBUF8 bus -- first, the lower half, using chip select signal CS7, followed by the upper half, using chip select signal CS4.

NOTE

The operations described in this paragraph involve the transfer of tape channel information from the TCVFU to the Processor CCA, and occur when the operator presses the tape reader switch on the TCVFU unit. Ultimately, this information is transferred from the Processor CCA to the DPC Centronics-Compatible Interface and is stored in line buffer U37-U38. Refer to paragraph 4.4.1h for TCVFU loading details.

6. Option Header Driver U24 - This device transfers information from the two option headers that plug into the mother board and connect through P2 to the DPC Centronics-Compatible Interface. To read the contents of

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the option header, the Processor CCA performs a memory read operation with the address bits configured for CS8. With CS8 active, the path is open between P2 and DBUF1 - DBUF8 through U24 and U23.

7. Last Address Driver U22 - This device channels the contents of the address counter U35-U36-U34 to the Processor CCA. At the end of a data load operation, the address counter always points to the line buffer location where the last character is stored. During buffer interrogate, the Processor CCA examines each location of the line buffer, starting with the location pointed to by the address counter. To accomplish this, the Processor CCA performs a memory read operation, with the address bits configured for CS2. With CS2 active, U22 along with U52 and U23, are enabled, opening the path between the address counter and data bus DBUF1-DBUF8.

8. Buffer Driver U20 - This driver channels user data to the line buffer U37-U28. During data load operations, signal FF1 is active, opening the path from data bus NDB1-NDB8 through U20 to data bus DB1 - DB8. Data on NDB1 - NDB8 is always in ASCII form.

9. Line Buffer U37-U28 - The line buffer is a 1K x 8 RAM, used for storing print and VFU data. It is accessible, on a time-shared basis, to the circuits internal to the DPC Centronics-Compatible Interface as well as to the Processor CCA. When ASCII-coded user data is under internal control, as specified by FF1, it is channelled through U20 and written into a location in the line buffer specified by address bits A0 - A9 and clocked by DATA STROBE*. In this case, the address bits are obtained in part from the address counter (U52 enabled), and in part from flip flop U9B (DAVFU/PRINT*), through U41. Address bit A9 is low when the data is a print or control character selecting the lower half of buffer locations. Address bit A8 is obtained from the most significant address counter flip flop U34.

When under control of the Processor CCA, as specified by CS1, data is either written into or out of the line buffer. Direction of data flow is controlled by mutually exclusive signals MEMW and MEMR, and the data is channelled between buses DB1-DB8 and DBUF1 - DBUF8 through U23. With CS1 active, chip U52 is disabled and chips U53 and U57-U41 are enabled. Accordingly, buffer location address is determined by the configuration of buffer address bits ADR0-ADR9. The Processor CCA writes into the line buffer during buffer interrogate or when storing TCVFU data. Typically, data is read out of the line buffer when printing.

10. Address Counter Driver U52 - This device channels eight of the address counter bits A0-A7 to either the line buffer or to the Processor CCA. When loading user data, FF1 is active and CS2 is inactive, and the line buffer location address is channelled from the address counter through U52 to the line buffer. During buffer interrogate, FF1 is inactive and CS2 is active, and the address counter points to the last buffer location where the control character is stored. Accordingly, this information is channelled through U52, U22, and U23 to data bus DBUF1 - DBUF8, and then to the Processor CCA.

11. ASCII Inverter U19 - This device is active when the printer operates without code conversion. It inverts ASCII-coded user data to bus NDB1 - NDB8, which is destined for the line buffer.

12. Code Converter MEM1 (Optional) - This device is active when the printer operates with code conversion. It converts user data of a specified code into ASCII format to bus NDB1 - NDB8, which is destined for the line buffer.

13. User Data Inverter U32-U18 - This device is active during data load, and is used to invert and condition user data of any code destined for either U19 or MEM1, as applicable.

14. Data Decoder MEM2 - This 256 x 8 PROM monitors user data at the NDB1 - NDB8 level for the presence of a special character. By definition, a special character is anything other than a print character, and includes the following:

- (a) SEL/DESEL - The user has selected or deselected the printer.
- (b) CR/LF - The user has transmitted a carriage return or a line feed code.
- (c) DAVFU START
- (d) DAVFU STOP
- (e) VFC - The user has transmitted a vertical format code accompanied by a paper instruction signal. Valid only when either TCVFU or DAVFU option is incorporated in the printer.
- (f) CONDENSED - User-programmed horizontal pitch.
- (g) EXPANDED - User-programmed horizontal pitch.
- (h) DELETE - User-programmed BUFFER CLEAR signal.

15. Count Decoder MEM3 - This 128 x 8 PROM monitors the output of the address counter for critical counts, as follows:

- (a) 132/220 = Top Count, respectively for normal or condensed horizontal pitch.
- (b) 222 = Maximum buffer load.
- (c) 255 = Maximum DAVFU count (equivalent to 510).
- (d) 222* = Clock derived from 222 and used to set flip flop U34.

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16. Address Counter U35-U36 - Together with U34, U35-U36 forms a 9-bit binary counter with a capacity of 512. Clocked by signal ACKLG in a binary sequence, it is used during data load to form the line buffer address bits A0-A8. Bit A9 is controlled by flip flop U9A. Counter U35-U36 is turned off when signal SCVP is inactive, when signal DAVFU FAULT* is active, or when signal 133FF* is active. Signal SCVP is inactive when either a condensed or expanded code is received, or when a CR code is received and auto line feed is not in effect. Signal DAVFU FAULT* is obtained from flip-flop U9B. Signal 133FF* is active when the total number of print characters exceeds 222.

Counter U35-U36 is initialized at the start of the data load cycle by signal LD BUFFER PL*, or when the user activates signal INPUT PRIME*. When initialized, counter U35-U36 is preset to a count of 1, so that user data is never loaded in location 0 of the line buffer.

17. DAVFU/PRINT* Flip Flop U9A - Flip-flop U9A defines during the data load cycle, the nature of the data supplied by the user. When reset, it indicates that the current user data consists of print information. Reset initially by signal LD BUFFER PL*, flip-flop U9A will stay reset unless a DAVFU START code is detected by MEM2. On detection of a DAVFU START code, U9A sets and remains set for the duration of that data load cycle. Signal DAVFU/PRINT* is used during the data load cycle to form the most significant line buffer address bit A9. It is also used as a status bit channelled through U39 to the Processor CCA.

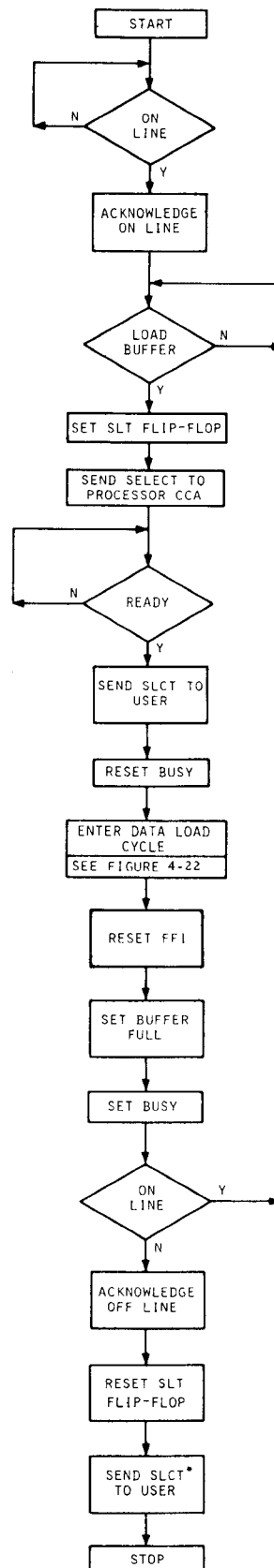
18. DAVFU FAULT* Flip Flop U9B - This flip-flop is set when a DAVFU fault condition is detected, and is used as one of the status bits channelled through U39 to the Processor CCA. DAVFU fault condition occurs when the number of DAVFU characters supplied by the user is odd, or when the number of DAVFU characters exceeds 510 (255 x 2).

19. Condensed, Expanded Flip Flops U8A and U8B - These flip flops store horizontal pitch information specified by the user in the form of horizontal pitch commands. The user may transmit either of the two horizontal pitch commands at any time during the data load cycle. From the flip-flops, the information is channelled through U39 to the Processor CCA. Then, during the subsequent print cycle, the entire line is printed with a horizontal pitch as specified. At the start of the next data load cycle, flip-flops U9A and U9B are cleared by LD BUFFER PL*.

20. Load Control - The load control is a group of circuits that controls sequential operation of the DPC Centronics-Compatible Interface. Its main function is to ensure that user-supplied print and DAVFU data is loaded in appropriate locations within the line buffer. Details of the load control are provided in paragraph d, Sequential Operation.

d. Sequential Operation (Figure 4-21)

The following paragraphs describe the sequence of major events involved in the operation of the DPC Centronics-Compatible Interface. Sequential operations are, for the most part, under control of the load control circuit



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Figure 4-21. DPC Centronics-Compatible Interface CCA General Flow Diagram

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group, shown in the block diagram in figure 4-20. The following topics are included, each keyed to a flow diagram:

1. General Operation
2. Data Load Cycle
3. User-controlled Select/Deselect

1. General Operation (Figure 4-21) - Following initialization, the DPC Centronics-Compatible Interface is in a inactive state, monitoring the condition of the ON LINE signal. When the Processor CCA activates the ON LINE signal, an ON LINE ACKNOWLEDGE signal is returned to the Processor CCA. No further action occurs until the Processor CCA activates the LOAD BUFFER signal. Upon receipt of signal LOAD BUFFER, flip-flops FF1 and SLT are set, and BUSY reset. Then, on the trailing edge of LOAD BUFFER, flip-flop BUFFER FULL is also reset. The condition FF1 BUFFER FULL* implies that the DPC Centronics-compatible Interface is now in the data load cycle, and the line buffer cannot be accessed by the Processor CCA. The condition SLT BUSY* informs the user that data can now be accepted.

During the data load cycle, user data is loaded, one character at a time, in the line buffer. The data load cycle ends upon receipt of a termination code (CLF, CR, FF, or VFC), or when maximum count is reached and auto print is enabled. Auto print is a switch-selected feature that automatically terminates the data load cycle upon receipt of 132 characters (normal print) or 220 characters (condensed print).

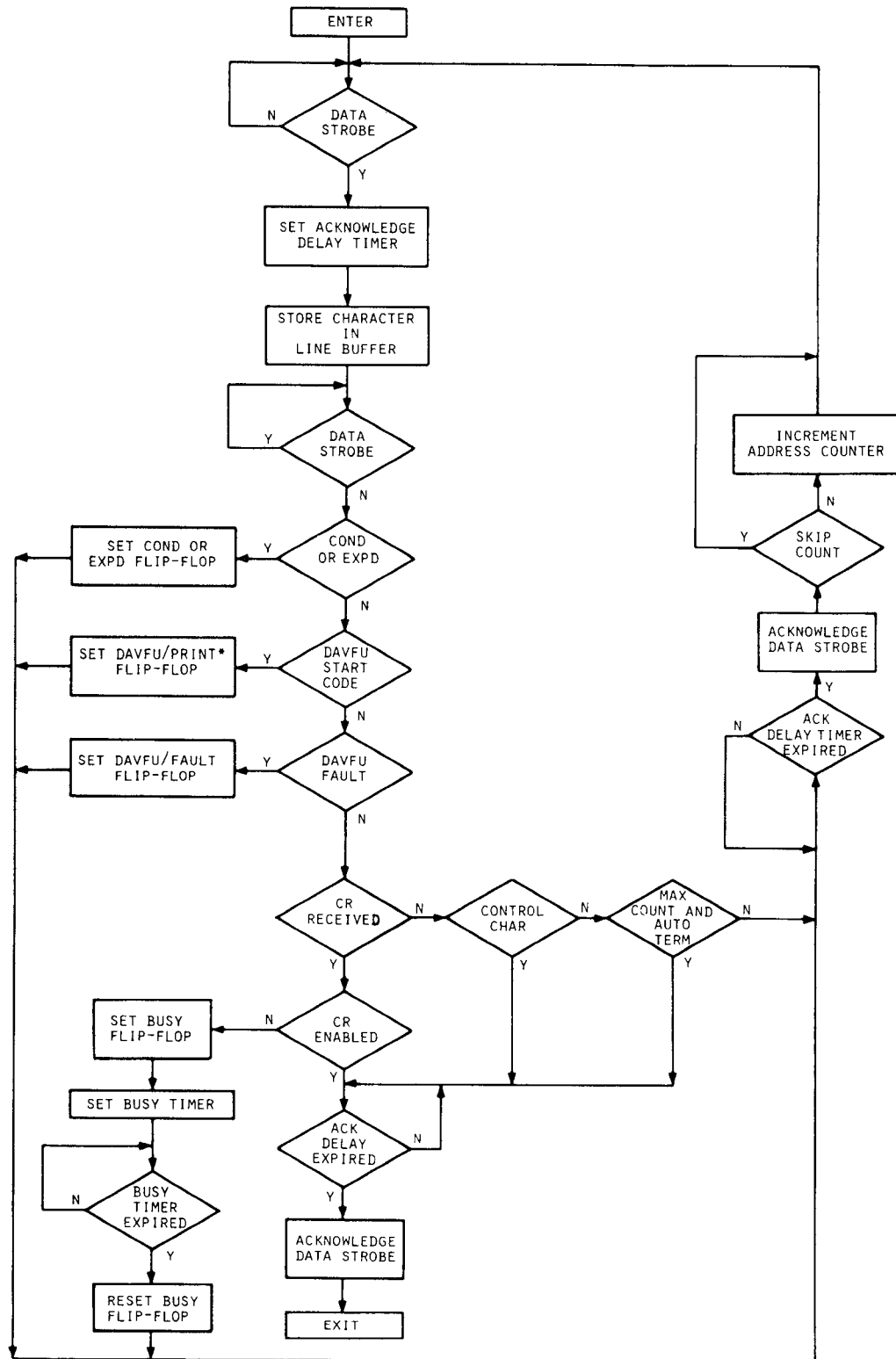
NOTE

Should the Processor CCA go off line while the DPC Centronics-Compatible Interface is in the midst of loading data, the off line signal will not be acknowledged until after the completion of the data load cycle.

Following completion of the data load cycle, flip-flops BUSY and BUFFER FULL are set, and FF1 is reset. The condition BUFFER FULL informs the Processor CCA that user data is now present in the line buffer and available for printing. Signal BUSY informs the user that further data will not be accepted until the BUSY condition has been lifted.

The on line signal is next monitored for a possible off line condition. If ON LINE is still high, the sequence loops back to the LOAD BUFFER decision block. If ON LINE is low, it is acknowledged immediately. Flip-flop SLT is then reset, informing the user that the printer is deselected.

2. Data Load Cycle (Figure 4-22) - The cycle begins when the user raises DATA STROBE, indicating that a character is available on the data lines. On the rising edge of DATA STROBE, an acknowledge delay timer is started, and the character is stored in location 1 of the line buffer. In addition, the character just stored in the line buffer is examined for the presence of special codes, such as a condensed or expanded code or a DAVFU start code. If



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Figure 4-22. DPC Centronics-Compatible Interface Data Load Cycle

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applicable, a test is also made to determine if a DAVFU fault exists. If any of these conditions is encountered, the applicable flip-flop is then set on the trailing edge of DATA STROBE. Otherwise, the character is tested for CR. If CR is received but not enabled, the BUSY flip-flop is set and the BUSY timer is started. When the BUSY timer expires, the BUSY flip-flop is reset. If CR is received and enabled, if any other control character (FF, LF, or VFC) is detected, or if a maximum count is reached and AUTO TERM is enabled, the acknowledge delay timer is tested. When the acknowledge delay timer expires, the DATA STROBE is acknowledged, and the data load sequence exits and returns to the general sequence.

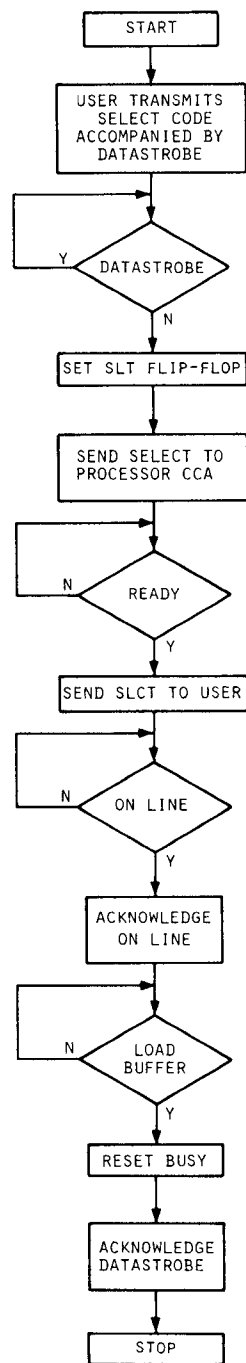
Under any other circumstances, such as no control character and no maximum count, the sequences do not exit but loop back toward the DATA STROBE decision box. First, the acknowledge delay timer is monitored, and when expired, the DATA STROBE is acknowledged. If no skip count condition exists, the address counter is incremented. Skip count condition exists if any of the following has been detected:

- (a) Condensed or expanded code
- (b) DAVFU error
- (c) Carriage return code (CR) was raised, but the CR function is disabled.

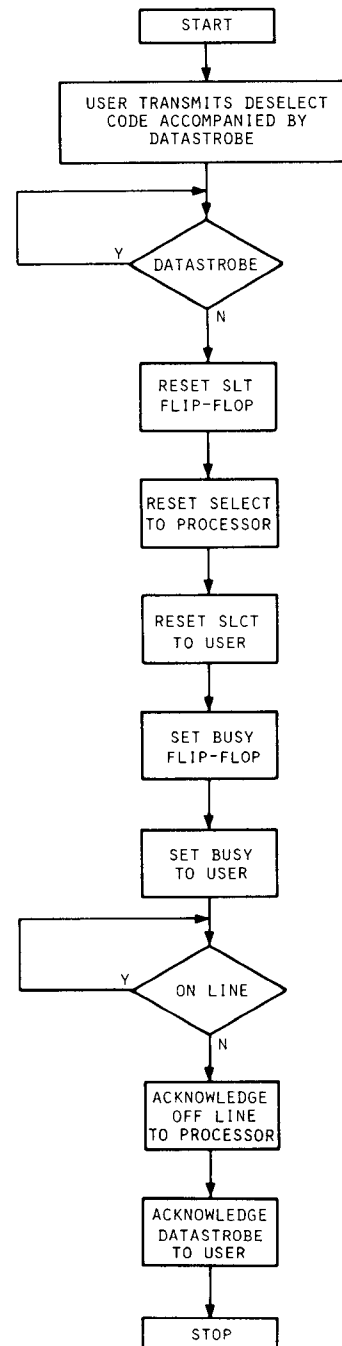
3. Select/Deselect (Figure 4-23) - Before the DPC Centronics-Compatible Interface can receive data from the user, it must be selected. The DPC Centronics-Compatible Interface can be selected either by the operator pressing the ON LINE switch or by the user transmitting a select code (octal 021). Once selected, the DPC Centronics-Compatible Interface can be deselected either by the operator pressing the ON LINE switch or by the user transmission of a deselect code (octal 023). The general flow diagram shown in figure 4-21 assumes that the select/deselect function was effected by the operator pressing the ON LINE switch. The sequence shown in figure 4-23 depicts user-transmitted select/deselect codes and is described in the following paragraphs:

(a) Select (Figure 4-23) - The sequence begins when the user transmits a select code accompanied by DATA STROBE. On the trailing edge of DATA STROBE, flip flop SLT is set, and a SELECT signal is transmitted to the Processor CCA. Assuming that READY is active (no further action will take place if READY is inactive), signal SLCT is transmitted to the user, indicating that the DPC Centronics-Compatible Interface is selected. However, at this point, the BUSY flip-flop is still set, and data cannot be accepted from the user.

At a later point in the sequence, the Processor CCA will respond to the SELECT signal transmitted earlier by raising signal ON LINE. With ON LINE high, an acknowledge signal is returned to the Processor CCA. In response, the Processor CCA transmits a LOAD BUFFER signal. With LOAD BUFFER high, the BUSY flip-flop is reset, and the DATA STROBE signal is acknowledged, indicating that the DPC Centronics-Compatible Interface is now ready to receive data from the user.



A. SELECT FLOW



B. DESELECT FLOW

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Figure 4-23. Select and Deselect Data

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(b) Deselect - (Figure 4-23) - Action starts when the user transmits a deselected code accompanied by DATA STROBE. On the trailing edge of DATA STROBE, flip-flop is reset. With SLT reset, signal SELECT is reset to the user. At the same time, flip-flop BUSY is set, and signal BUSY is transmitted to the user.

Later in the sequence, the Processor CCA responds by dropping the ON LINE signal. With ON LINE low, an OFF LINE ACKNOWLEDGE SIGNAL is returned to the Processor CCA.

NOTE

Should the user transmit a DESELECT code during a data load cycle, no OFF LINE ACKNOWLEDGE signal will be transmitted to the Processor CCA at this point.

Following acknowledgement of the OFF LINE signal, DATA STROBE is acknowledged, completing the DESELECT sequence.

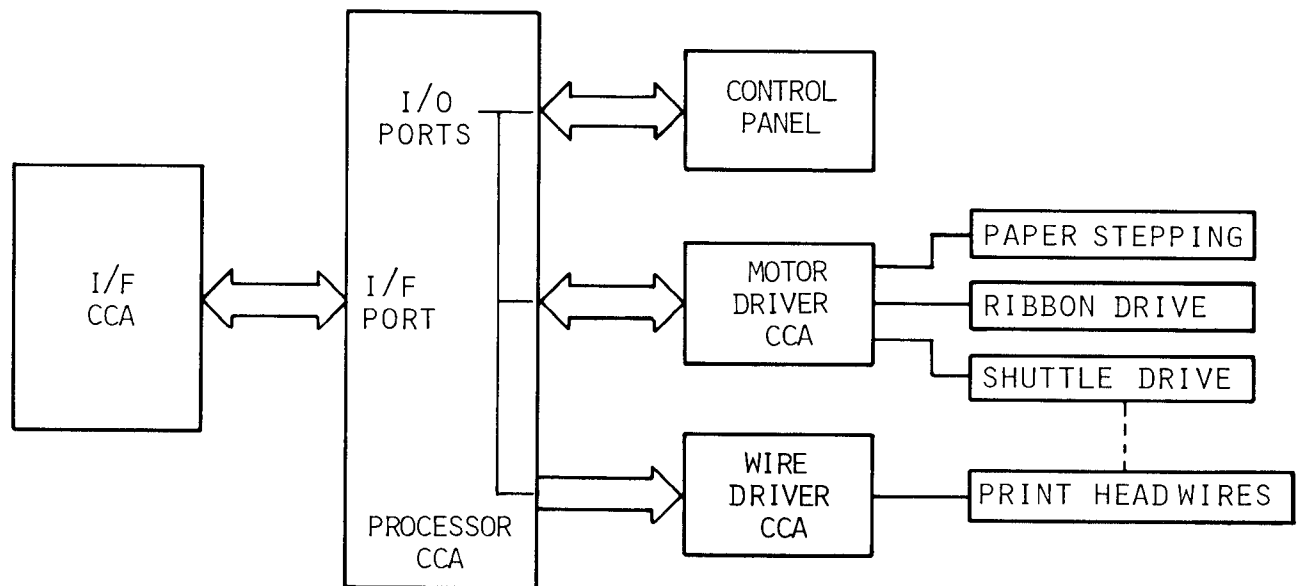
4.5 PROCESSOR CCA (Figure 4-24)

The following paragraphs are detailed functional descriptions of the Processor CCA. The Processor CCA is a microprocessor-based pre-programmed computer that functions as the printer's controller. As shown in the simplified block diagram in figure 4-24, the Processor CCA is interfaced with the other circuit card assemblies via the interface (I/F) port and input/output (I/O) port. The following discussion of the Processor CCA's control over the I/F and I/O port communications assumes that the circuit card assemblies are integrated as a system. Detailed logic diagrams are provided in volume II of this manual.

4.5.1 Functional Organization (Figure 4-25)

The Processor CCA is organized as shown in figure 4-25 and is comprised of the following functional elements:

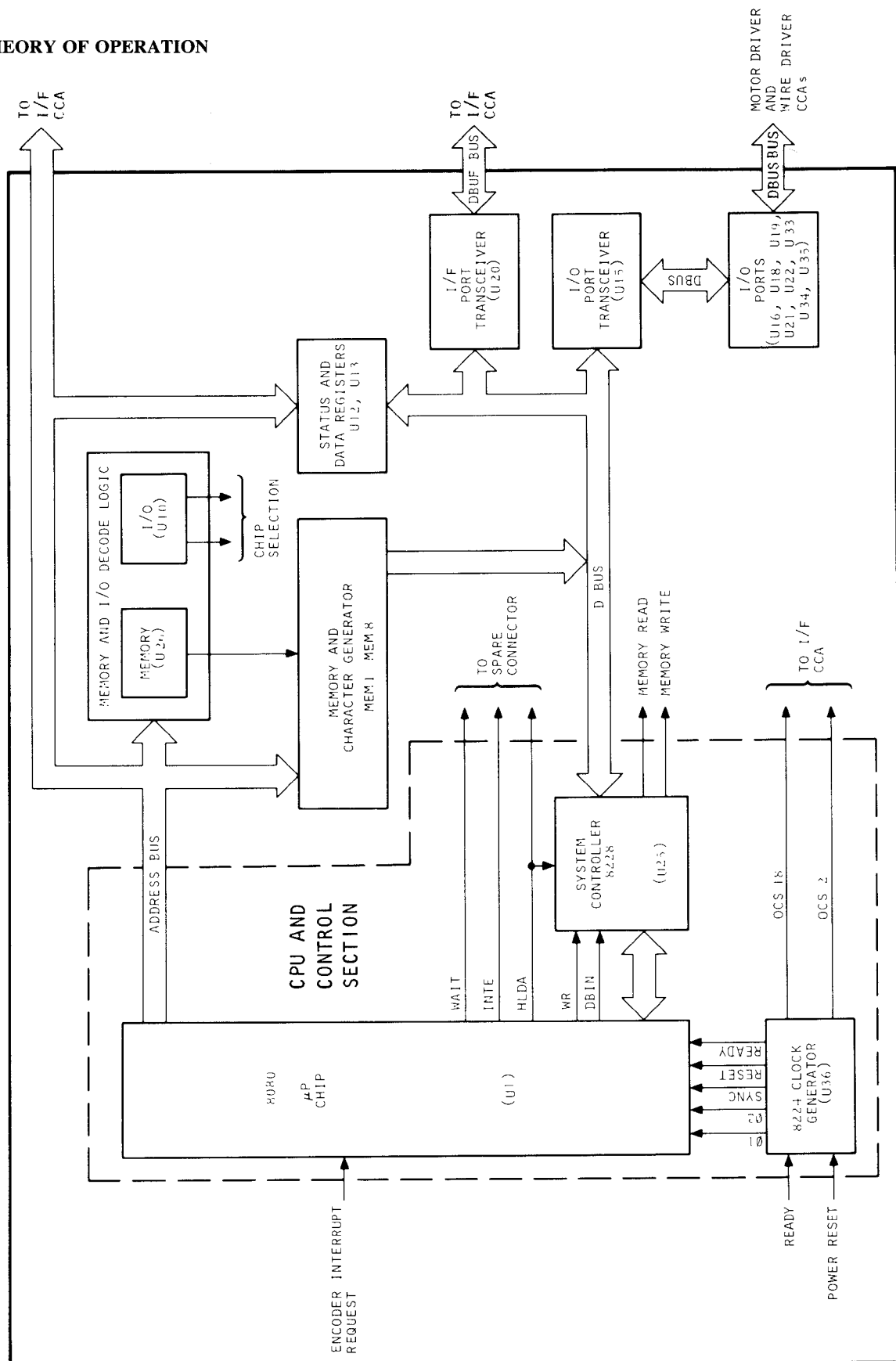
- a. CPU and Control Section
- b. Program Memory
- c. Character Generators
- d. I/F Port Transceiver
- e. I/O Port Transceiver
- f. Memory and I/O Decoding Logic
- g. Status and Data Registers
- h. Address and Communications Bus Structure



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Figure 4-24. Simplified Block Diagram of Processor CCA Interface and Communication Ports

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Figure 4-25. Processor CCA Functional Organization Block Diagram

a. CPU and Control Section

The CPU and Control Section is comprised of the 8224 Clock Generator, the 8228 system controller, and the 8080 Control Processing Unit (CPU). These three devices synchronize and control all printer operation. Operating instructions read from program memory are carried to the 8080 microprocessor chip, via the system controller, over the internal data bus (D bus). The 8-bit data bus is connected to both I/F and I/O port transceivers, thereby establishing a communication link between the 8080 microprocessor chip and any addressable device.

The two basic operations performed by the CPU and Control Section are the read and write instructions. Information is read into the 8080 microprocessor chip, is processed, and is then written out to one of the devices on the Processor CCA I/F or I/O port. The signals MEMORY READ and MEMORY WRITE enable the appropriate devices.

Since the data bus is shared by most of these devices, each device must have tri-state outputs and must remain in the off state until enabled. Each device is assigned a 16-bit code address, which is connected to the address bus. When the 8080 microprocessor chip outputs the address of a device, that device becomes enabled, and information may be read from or written into it.

1. Control Signal Definitions - Table 4-10 contains a list of signals and their definitions used by the CPU and Control Section.

TABLE 4-10. CPU AND CONTROL SECTION SIGNALS

Signal	Definition
INT	Interrupt - counts the encoder marks.
INTE	Interrupt Enable - The 8080 microprocessor chip will acknowledge interrupts.
INTA	Interrupt Acknowledged - causes the program to jump to the proper point upon receipt of the encoder marks.
WAIT	A response that the 8080 microprocessor chip is in an idle mode.
Ø1	The 2 mHz clock, 110 ns on, and 385 ns off (0-12V).
Ø2	The 2 mHz clock, 275 ns on, and 220 ns off (0-12V).
RESET	A clear signal to the 8080 microprocessor chip resulting from the power up delay signal POWER RESET* to the 8224 clock generator.
SYNC	Output by the 8080 microprocessor chip to mark the start of the instruction cycle.

TABLE 4-10. CPU AND CONTROL SECTION SIGNALS (Contd)

Signal	Definition
Ø2TTL	0-5 volt Phase 2 output.
OSC	The 18 mHz output.
WR*	A write instruction is being performed.
DBIN	Data Bus In, a read instruction is being performed.
BUSEN*	The chip enable for the system controller.
MEMW*	Write contents of the Data Bus into a device.
MEMR*	Read contents of a device onto the Data Bus.
STATUS STROBE*	A low true construct of SYNC or POWER RESET* which allows the system controller to latch status bits and to reset automatically on power up.

2. Operating States - This paragraph describes the following 8080 microprocessor chip operating states: Write Operation, Read Operation, Interrupt Operation, Ready Condition, Reset Condition, Sync Operation, and Bus Enable.

(a) Write Operation - Signal WR* will go low whenever a write instruction is performed, allowing information from the microprocessor chip to pass through the system controller and onto the data bus.

(b) Read Operation - Signal DBIN (Data Bus In) goes high when information on the data bus is to be received by the 8080 microprocessor chip.

(c) Interrupt Operation - When enabled, the 8080 microprocessor chip can be interrupted by signal INT, which is used to count the encoder marks as the shuttle is moving. After the interrupt has been serviced, the 8080 microprocessor chip will resume normal operation at the point in the program where it was interrupted.

(d) Ready Condition - Signal RYDIN to the clock generator is synchronized and passed onto the 8080 microprocessor chip when a ready condition exists. Without the READY signal, the microprocessor chip will be in a WAIT or IDLE mode.

(e) Reset Condition - Signal POWER RESET* (Reset into the Clock Generator) is synchronized and sent to the 8080 microprocessor chip as RESET, thereby clearing the microprocessor chip set and starting program execution at address zero.

(f) Sync Operation - Before each instruction is performed, the 8080 microprocessor chip conditions the control bus by outputting signal

SYNC to the Clock Generator, where it is synchronized and sent as signal STATUS STROBE to the System Controller. This information is latched into a register that outputs the contents of the control bus.

(g) Bus Enable - Signal BUSEN* (Bus Enable) will enable the System Controller when low.

3. CPU and Control Section Timing - All operations performed by the 8080 microprocessor chip must be synchronized. The Clock Generator establishes the timing and synchronization for the following signals.

(a) Clock, Ø1-Ø2 - The Clock Generator is crystal controlled and outputs a two-phase clock to the 8080 microprocessor chip to establish the Phase 1 and Phase 2 timing.

(b) Oscillator - The oscillator output (OSC) from the Clock Generator is the frequency of the crystal, which is nine times faster than the system's rate of operation.

(c) TTL Ø2 - Signal TTL is the logic level Phase 2 clock.

4. 8224 Clock Generator - At the start of the print cycle, the 8080 microprocessor chip issues status information on its data bus on the type of action to take place during that cycle. By bringing the SYNC signal from the CPU and Control Section and gating it with an internal Phase 1A timing signal, a low strobe is derived. This occurs at the start of each print cycle, as soon as the status information is stable on the bus. Signal STSTB* (Status Strobe) connects directly to the 8228 System Controller.

Power up reset signal POWER RESET* also generates STSTB* which automatically resets the System Controller.

The generation of the automatic system reset and start up upon initial power up is accomplished by the 8224 Clock Generator. An external RC network is connected to the RESIN* input. The slow transition of the power supply rise is sensed by an internal Schmitt trigger. This circuit converts the slow transition into a clean, fast edge when its input reaches a predetermined value. The output of the Schmitt trigger is connected to a D-type flip flop which is clocked by the Phase 2D internal timing signal. The flip flop is synchronously set, and the RESET signal is withdrawn from the 8080 microprocessor chip. The RYDIN* (Ready In) signal is connected to a D-type flip flop and is also clocked by Phase 2D. Its output, READY, is sent to the 8080 microprocessor chip. The 8224 single chip Clock Generator/Driver contains the following:

(a) Crystal-Controlled Oscillator - Two inputs are provided for the crystal connections XTAL1 and XTAL2. The selection of the external crystal frequency depends mainly on the speed at which the 8080 microprocessor chip is to be run. Basically, the oscillator operates at nine times the desired microprocessor chip speed. The crystal selected for the printer is 18 MHz.

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(b) Clock Generator - The Clock Generator consists of a synchronous divide-by-nine counter and the associated decode gating needed to create the waveforms of the two 8080 microprocessor chip clocks and auxiliary timing signals. The waveform generated by the decode gating is a 2-5-2 digital pattern.

The Phase 1 and Phase 2 clocks generated can be thought of as consisting of units based on the oscillator's frequency. Assume that one unit equals the period of the oscillator frequency. By multiplying the number of units contained in a pulsewidth or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be obtained.

(c) High Level Drivers - The outputs of the Clock Generator are connected to two high level drivers for direct interface to the 8080 microprocessor chip. TTL level Phase 2 is also generated for external timing purposes.

(d) Auxiliary Logic Functions - Several other signals are generated internally so that timing of the auxiliary flip flops (READY, RESET, and STATUS STROBE) can be achieved.

5. 8228 System Controller - The 8228 is a single chip system controller and databus for the microprocessor. It generates all control signals required to interface directly with RAM, ROM, and devices on both I/F and I/O ports. The bi-directional bus driver is controlled by signals from the gating array so that proper bus flow is maintained, and its outputs can be forced into their high impedance state (tri-state) for direct memory accessing activities.

At the start of each print cycle, the 8080 microprocessor chip issues on its data bus status information that indicates the type of activity that will occur during the cycle. The system controller stores this information in a status latch when the STSTB* (status strobe) information goes low. The output of the status latch is connected to the gating array and is part of the control signal generation.

(a) Gating Array - The gating array of the 8228 system controller generates control signals MEMR*, MEMW*, I/O R*, I/O W*, and INTA* by gating the outputs of the status latch with signals DBIN*, WR*, and HLDA* from the 8080 microprocessor chip.

(b) Read Operation - The read control signals MEMR*, I/O R*, and INTA* are derived from the logical combination of the appropriate status bits and the DBIN input from the 8080 microprocessor chip.

(c) Write Operation - The write control signals MEMW* and I/O W* are derived from the logical combination of the appropriate status bits and the WR* input from the 8080 microprocessor chip.

(d) Interrupt - The ENC INT REQ* interrupt signal is automatically gated onto a bus internal to the 8080 microprocessor chip. Each interrupt will cause a jump to a specified location in the program memory. The

system controller is set up so that when DBIN input is active, the instruction is gated onto the internal data bus (D Bus) when ENC INT REQ* is acknowledged.

(e) Bus Enable - The BUSEN* (bus enable) input will enable the system controller when low. Since a single system controller is used on the printer, this signal is tied to ground.

b. Program Memory

The program memory and character generator consists of Programmed Read Only Memory chips (PROMs) MEM1 through MEM8. A map of this memory structure is shown in figure 4-26. Enabling any of the various memory devices is a function of the memory and I/O decode logic in table 4-12.

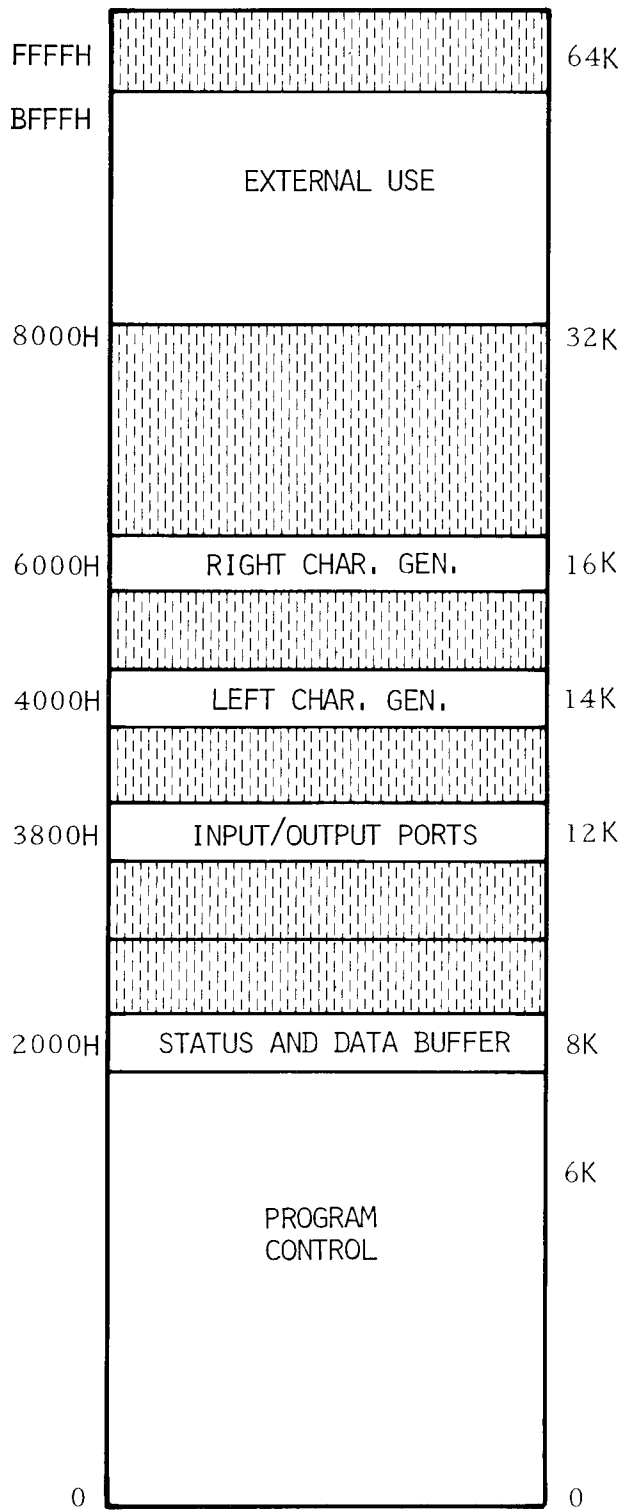
As shown in figure 4-26, the program memory is partitioned into dedicated segments comprising the program control section, input/output ports, status and data buffer registers, and right and left character generation segments.

1. Program Control Section - The program control section is the main portion of the memory, coordinating the sequence of operation for correct printer operation. The program control section performs the following tasks:

- (a) Monitors all printer switches
- (b) Controls two-way status and data exchange with the Interface CCA.
- (c) Controls the shuttle servo motor for speed and direction.
- (d) Moves paper as required by controlling the paper feed stepping motor.
- (e) Prints data by controlling the firing of the print wires.

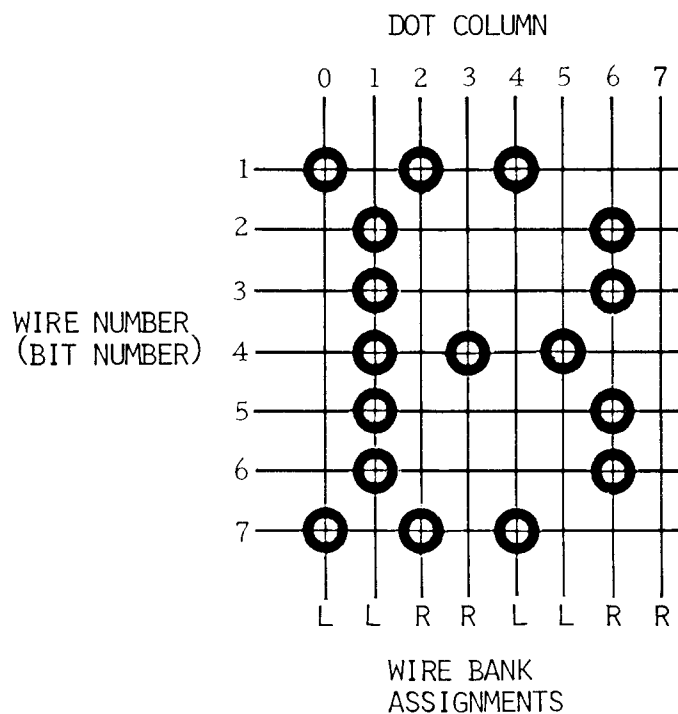
c. Character Generators - This section of the memory contains the tables which specify the print wire(s) to be fired for each printable character. Figure 4-27 shows an example of character generation. The vertical columns (dot columns) represent seven of ten equally spaced segments of a character column. Columns eight to ten are used by the control program for character spacing. The dot column data corresponds to the encoder-generated interrupts input into the 8080 microprocessor chip. Each horizontal column represents one of seven print wires in the print head which is to be fired when printing a character.

Each dot column represents one byte (8 bits) of data which determines if a dot is to be printed. Since there are only seven wires per wire bank, bit 8 is always a zero. As shown in figure 4-27, dot column zero has a dot in positions 1 and 7, which corresponds to a hex 41. In dot column 6, positions 2, 3, 5, and 6 have dots which correspond to a hex 36.



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Figure 4-26. Program Memory Map



	L	R
0	41 _H	00
1	3E _H	0 _H
2	0 _H	41 _H
3	0 _H	08 _H
4	41 _H	00 _H
5	08 _H	0 _H
6	0 _H	36 _H

A DOT = 1
NO DOT = 0

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Figure 4-27. Example Of Character Generator Structure

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The data is stored in consecutive bytes within the character generator. These are addressed by a combination of the binary equivalent of the dot column number plus the binary equivalent of the seven-bit ASCII code for the character being printed. The most significant bit of the address is a zero for the left bank data and a one for the right bank. Table 4-11 provides an example of the ASCII code dot column number addressing.

TABLE 4-11. ASCII CODE/DOT COLUMN NUMBER ADDRESSING

ASCII Code	Dot Column Number	Address (Hex)	
		Left	Right
1 0 0 0 0 1 0	0 0 0	210	610
1 0 0 0 0 1 0	0 0 1	211	611
1 0 0 0 0 1 0	0 1 0	212	612
1 0 0 0 0 1 0	0 1 1	213	613
1 0 0 0 0 1 0	1 0 0	214	614
1 0 0 0 0 1 0	1 0 1	215	615
1 0 0 0 0 1 0	1 1 0	216	616
1 0 0 0 0 1 0	1 1 1	217	617
Note: For international characters 80 _H - 9F _H , bit 8 is dropped, and addressing starts at 0 _H .			

The address bus to the character generator has been arranged so that a 16-bit address will access the data for each dot column. The lower byte of the address is the same as the ASCII code for the character being printed. The lower 3 bits of the upper byte is the dot column being printed at that particular moment. The upper byte is either a 4_H or a 6_H, depending on whether the data is for the left or right bank of wires.

For dots printed by the same wire, there are a minimum of three dot columns between the dots. This spacing allows for the cycle time needed for the wires. Cycle time is the total amount of time required for a wire to go from a rest position to a full extension and then back to a rest position.

d. I/F Port Transceiver

The Processor CCA communicates with the various interface configurations described in paragraph 4.3 via the I/O port transceiver U20, using address bit A15. Control and status information and data exchanged between the Processor CCA and the Interface CCA are transferred over the 8-bit DBUF bus. The information exchanged between the two CCAs and the input/output devices which interface the I/F port transceiver is described in paragraph 4.5.3 and illustrated in figure 4-29. Another function of the I/F port transceiver is to supply status information to the optional status display using chip select signal CS16*. The interface port transceiver operation is shown in the following truth table.

MEMR*	A15*	CS16*	Function
1	0	1	Write Data to I/O Port
1	1	0	Write Data to Display
0	0	1	Read Data from I/F Port
* = Active in the low state X = Don't care condition			

e. I/O Port Transceiver (U15)

The Processor CCA communicates with the print, paper advance, ribbon advance, and shuttle movement control electronics via the I/O bus transceiver U15. A detailed description of the I/O port functions is provided in paragraph 4.5.4 and illustrated in figures 4-30 and 4-31. The I/O port transceiver is shown in the following truth table.

CS6*	MEMR*	Function
0	0	Read from I/O Port
0	1	Write to I/O Port
* = Active in the low state X = Don't care condition		

f. Memory and I/O Decoding Logic

A unique device within the program memory and character generator section is enabled by memory decoder U26. The memory decoder uses a 5-bit address scheme (bits 11-15) to select one of eight memory devices. I/O decoding is performed by U10, which uses a 9-bit address scheme (bits 0-3 and 11-15). Table 4-12 below lists the memory device enable signals and their functions. Refer to table 4-15 for the device enable selection signals and their functions.

TABLE 4-12. MEMORY DEVICE ENABLE SIGNALS

Address Bit Configuration 15 14 13 12 11	Chip Select Signal	Function
0 0 0 0 0	CS1*	With A10, enables MEM1 or MEM2
0 0 0 0 1	CS2*	With A10, enables MEM3 or MEM6
0 0 0 1 0	CS3*	With A10, enables MEM7 or MEM8
0 0 0 1 1	CS4*	Enables MEM4
0 0 1 0 0	CS5*	With MEMW* used to enable the status and data register group
0 0 1 1 0	CS6*	With MEMR* used to enable the I/O port transceiver. Also used to enable I/O port devices
0 1 X X X	--	Enables MEM5 (character generator)

g. Status and Data Registers

The Status and Data Registers are random access memory chips U12 and U13. These elements are linked to form 8-bit-wide registers, which are used to store the status of each device that controls the printer operation and to provide temporary storage for print or VFU data. Table 4-13 lists the locations addressed by the CPU and Control Section and the function of each location.

TABLE 4-13. STATUS AND DATA REGISTER ADDRESS AND USAGE

Address (Hex)	Usage
2000-2085	Processor CCA RAM used to store the self test pattern.
208F	Counts the number of times the shuttle servo motor has moved with a line feed only.
2090	Dot column counter. Its value is incremented (or decremented) by each encoder mark, depending on the direction the Motor Driver CCA is moving.
2091	Character column counter. Its value is incremented (or decremented) each time a new character is accessed.
2092	True condition bit used to determine if a switch change is real or caused by noise.
2093	Interface CCA RAM status register. Is set if Interface CCA is installed.
2094	Register containing the line termination code received from the Interface CCA.
2095	Shuttle speed compressed print bit. Low True 20 _H = 34 inches per sec. (10 CPI) 00 _H = 20.4 inches per sec. (16 CPI)
2096	Out of Paper Status Register.
2097	Non-underline printable character bit which is set each time a printable character is decoded.
2098	Printable character bit which is set whenever a line of data contains printable characters.
2099	No paper motion status register. Set to 01 _H each time paper has been moved, which inhibits paper motion.

TABLE 4-13. STATUS AND DATA REGISTER ADDRESS AND USAGE
(Contd)

Address (Hex)	Usage
209A	Expanded print bit which is set when a line of data contains an expanded code.
209B	Multiple line feed bit which is set whenever a form feed or VFU command is received.
20AC	Contains print data for the right bank of wires.
20AD	Contains control information for the Interface CCA (on line, load buffer, etc.).
20AE	Contains print data for the left bank of wires.
20AF	Contains the ASCII code for the right bank of wires.
20B0	Contains the ASCII code for left bank of wires.
20B1	Register that contains information to determine which way to move the shuttle in order to print the next line.
20B3	Contains forms length select switch setting. Used to initialize register 20A4 _H and update any FLS changes.
20B5	Horizontal velocity bit used to detect a change in shuttle speed.
20B6	Temporary storage register for print data. Used for expanded print.
20B9	Register that contains information calculated for seeking horizontal position of the shuttle. Used to determine the fastest way to move the shuttle to print the next line.
20BB	Contains the start of line character column count value.
20BC	Contains the end of line character column count value.
20BD	Contains information for output port 3008 _H .
20BE	Contains information for output port 3007 _H .
20C0	Counter used to detect the absence of encoder marks.
20C1	Counter used for 240 line shutoff for self test.
209C	Underline bit which is set whenever an underline code is received.

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TABLE 4-13. STATUS AND DATA REGISTER ADDRESS AND USAGE
(Contd)

Address (Hex)	Usage
209D	Partial paper feed bits one and two. Set for underlining.
209F	Self test bit which is set when the printer is in the self test mode.
20A0	Character column counter right. Counts multiples of 10 encoder marks for the right bank of wires.
20A1	Character column left. Counts multiples of 10 encoder marks for the left bank of wires.
20A2	Contains the character column counter value of the first character in the line.
20A3	Contains the character column counter value of the last character in the line.
20A4	Contains the number of printable lines remaining in the form. It is decremented each time paper is moved.
20A5	Contains the number of printable lines in a form. Based on vertical pitch, forms length select switch setting, and variable format information.
20A6	Overprint counter, set to 12 initially. Decrementd whenever an overprint occurs.
20A7	Contains either a carriage return, line feed, or form feed code.
20A8	Contains the number of lines for perforation skip.
20A9	Contains the upper 8 bits of print buffer address.
20C2	Register used as a timer for various printer operations.
20C3	Register used as a timer for various printer operations.
20C4	Counter used to allow only five successive reads of a vertical format tape.
20C5	Vertical format-loaded status register. Set whenever vertical format data has been loaded, or any vertical format faults have been cleared.

TABLE 4-13. STATUS AND DATA REGISTER ADDRESS AND USAGE
(Contd)

Address (Hex)	Usage
20C6	Contains lower byte of vertical format memory address.
20C7	Contains upper byte of vertical format unit memory address.
20C8	Lower byte of direct access vertical format counter.
20CA	Forms length count value for the bottom of form position.
20CB	Forms length count value for the top of form position.
20CC	Bottom of form for perforation skip.
20CD	Go to top of form for perforation skip.
20CE	On line flip flop status register. Used to check for changes in the state of the on line flip flop.
20CF	Bit set when a carriage return code terminates a line of data containing an underline code. Inhibits paper motion.
20D0	Print head shuttle position seeking bit, set whenever the shuttle is moving the print head.
20D1	Top count code used with the DPC Centronics-Compatible Interface CCA. Used with auto print feature.
20D2	Jog timer bit which is set after a jog. When set, will cause a time delay to allow the shuttle speed to settle before further movement occurs.
20D3	Double termination code bit which is set when a line of data contains a termination code only (LF, CR, or FF).
20D4	Carriage return only bit which is set when a carriage return code terminates a line of data.

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h. Address and Communications Bus Structure

The Processor CCA uses a four-bus system to address and communicate with its various internal elements, the Interface CCA, the Wire Driver and Motor Driver CCAs, and the operator control panel. The following buses comprise the address and communications bus structure: D Bus, DBUS Bus, DBUF Bus, and Address Bus.

1. D Bus - The D bus is an 8-bit bus which interfaces the CPU and Control Section with the I/O port transceiver (U15), I/F port transceiver U20, the program memory and character generator, and the status and data registers U12 and U13.

2. DBUS Bus - The DBUS Bus is an 8-bit bus which interfaces the I/O port transceiver U15 with the various I/O port devices.

3. DBUF Bus - The DBUF Bus is an 8-bit bus which interfaces the Processor CCA with the Interface CCA and the optional status display on the control panel.

4. Address Bus - The address bus is a 16-bit high true bus used for memory addressing and chip selection. The high true state is used for addressing the interior elements of the Processor CCA (bit 15 is always low). The address bus is routed through inverters and transferred to the Interface CCA in the true state. (Bit 15 must be in the high state when an internal element of the Interface CCA is to be addressed).

4.5.2 Initialization for Interface and Input/Output Port Communication

Before the I/F and I/O ports can be enabled for data transfer, wire firing, ribbon advance, and paper advance operations, the printer must be powered up and the initialization and operating status verification sequences must be performed.

a. Power Up PWR RESET*

When PWR RESET* goes active, the CPU and Control Section will perform the following functions:

1. Disable Interface Control Latch 9000_H by writing a 00_H. Status is written into Status and Data Register 20AD_H.

2. Read Option Header data from interface port B800_H.

3. Write a B3_H to I/O port 3008_H to drive the Paper Feed Stepping Motor to Phase One, and then a BE to lock the motor in Phase One. Phase of this operation is stored in Status and Data Register 3006_H.

4. Read Perforation skip data from the Interface options configuration header latch B800_H, compute the value, and store in Status and Data Register 20A8_H.

5. If the FLSS option is installed, the value is read from I/O port 300B and stored in Status and Data Register 20B3_H. The value is converted into the number of printable lines and stored in Status and Data Registers 20A4_H and 20A5_H.

6. If the printer is of a standard configuration, the value is read from Interface Option Header B800_H, is computed, and stored in Status and Data Registers 20A2_H and 20A5_H.

7. DBUF 4 is set to Interface Control Latch 9000_H, and the status is stored in Status and Data Register 20AD_H.

8. Outputs from I/O Port 3007_H are set to the high state. Signal RESET* in the high state clears the internal logic and logic on the Interface CCA.

9. The following Status and Data Registers are set as indicated: 2005_H = 00, 20CC_H = 00, 20CD_H = 00, and 2096_H = 01.

b. Initialization

The Initialization sequence is entered as a result of completing the power-up sequence, or as a result of an alarm clear condition. The sequence is as follows:

1. DBUF1 - DBUF3 are set low to Interface Control Latch 9000_H, resetting signals ON LINE, READY, and LOAD BUFFER. The status of this operation is stored in Status and Data Register 20AD_H.

2. DBUS is set to a 32_H and transferred to output port 3007_H. This operation resets flip flops U28 and U30 on the Processor CCA and resets logic on the Interface CCA.

3. Signal CLRFF (bit 5) of input port 3009_H is tested for its logic state. If low, then all outputs of port 3008_H are set high to disable all motor operations. If high, then the following Status and Data Registers are set as indicated below:

<u>Register</u>	<u>Value</u>
2099	01
209B	00
209C	00
209D	00
209F	00
20A6	12
20CB	00
20CF	00
20D0	00

4. Signal 10/16*PITCH (bit 6) of input port 300B_H is tested for its logic state. If low (16 pitch) then 20_H is written into Status and Data Register 2095_H and 20B5_H. If high (10 pitch), then 00_H is written into the registers.

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5. Signal BAIL OPEN (bit 4) of input port 300A_H is tested for its logic state. If low, then the state of signal CLEAR FLOP output from U28 is tested at Input port 3009_H. BAIL OPEN in the high state will cause the CPU and Control Section to recycle through the initialization sequence until BAIL OPEN is reset. BAIL OPEN in the high state will cause ALARM IND* of output port 3007_H to be enabled, and READY to be reset to Interface Control Latch 9000_H. The new interface status word is written into Status and Data Register 20AD_H. This cycle will continue until CLRFF of input port 3009_H switches to the high state. BAIL OPEN in the low state will cause GO/STOP of output port 3008 to be enabled, which will initiate shuttle movement to the shuttle park position.

6. DBUF Bus is set to zero and output to the VFU/Print data line buffer 8000_H on the Interface CCA. The CPU and Control Section will then perform a read operation to detect any change in the status of DBUF Bus. If a change is detected, indicating the absence of any Interface CCA, Status and Data Register 2093_H is cleared, and output port 3008_H is disabled to halt any motor operation. If the DBUF Bus remains low, indicating the presence of an Interface CCA, then 01_H is written into Status and Data Register 2093_H, and DBUF bit 2 (READY) is set high to Interface Control Latch 9000_H.

c. Operating Status Verification (Figure 4-28)

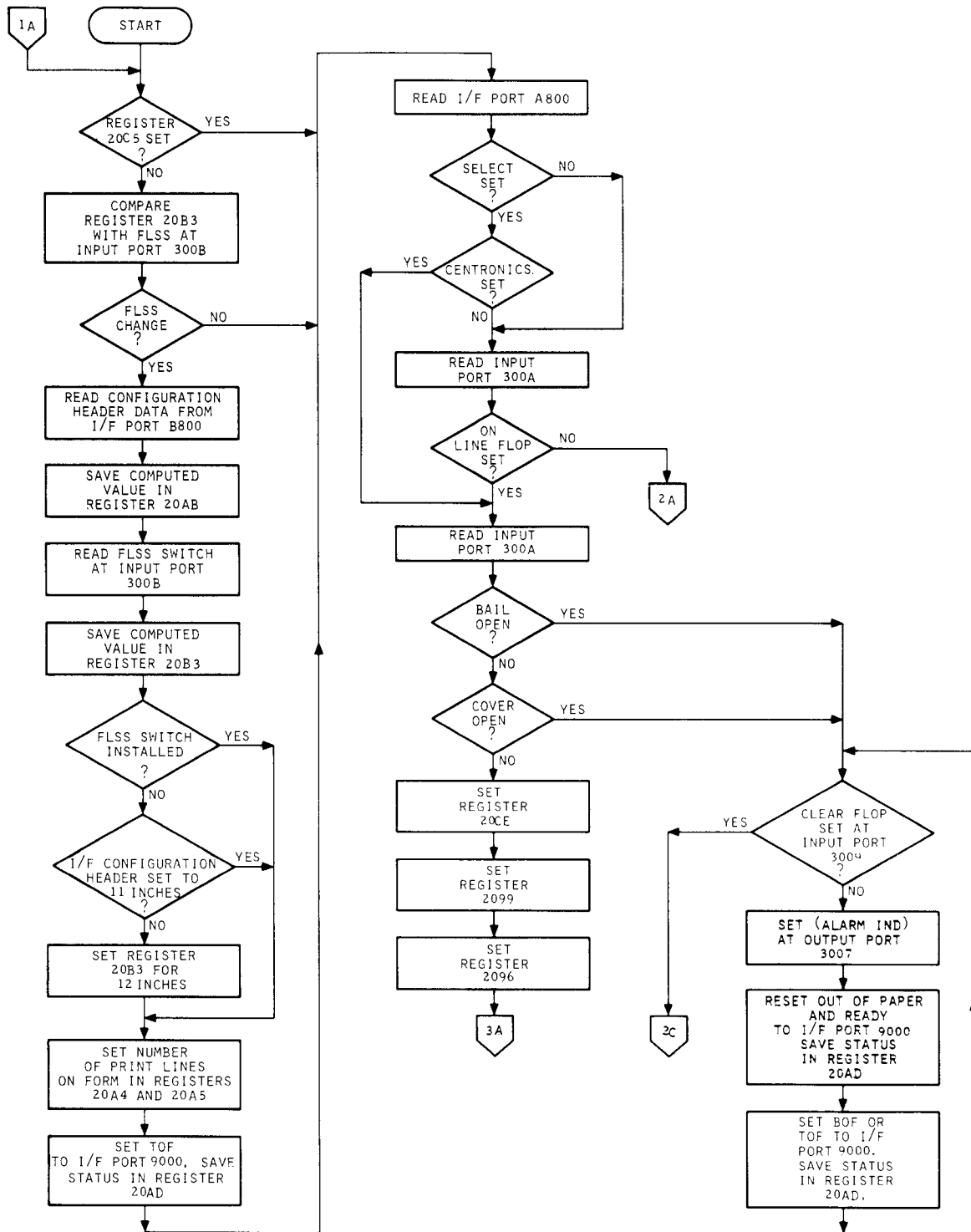
After completing the Power-up and Initialization sequences, the CPU and Control Section enters into the operating status verification sequence. This sequence is re-entered each time the shuttle is parked because of a slow interface data transmission rate, a paper advance command which requires multiple line feed operations, a command which requires a change in the shuttle travel velocity, the absence of a character generator, or because of the completion of a self test operation. Completion of this sequence allows the CPU and Control Section to enable the ports for either on line or off line operation.

During this sequence, the Status and Data Registers are updated to reflect the current operating status of the I/F and I/O ports. Upon completion of this sequence, the ON LINE, READY, and LOAD BUFFER CONTROL outputs are enabled to I/F Port 9000_H.

4.5.3 Interface Port Communication and Control (Figure 4-29)

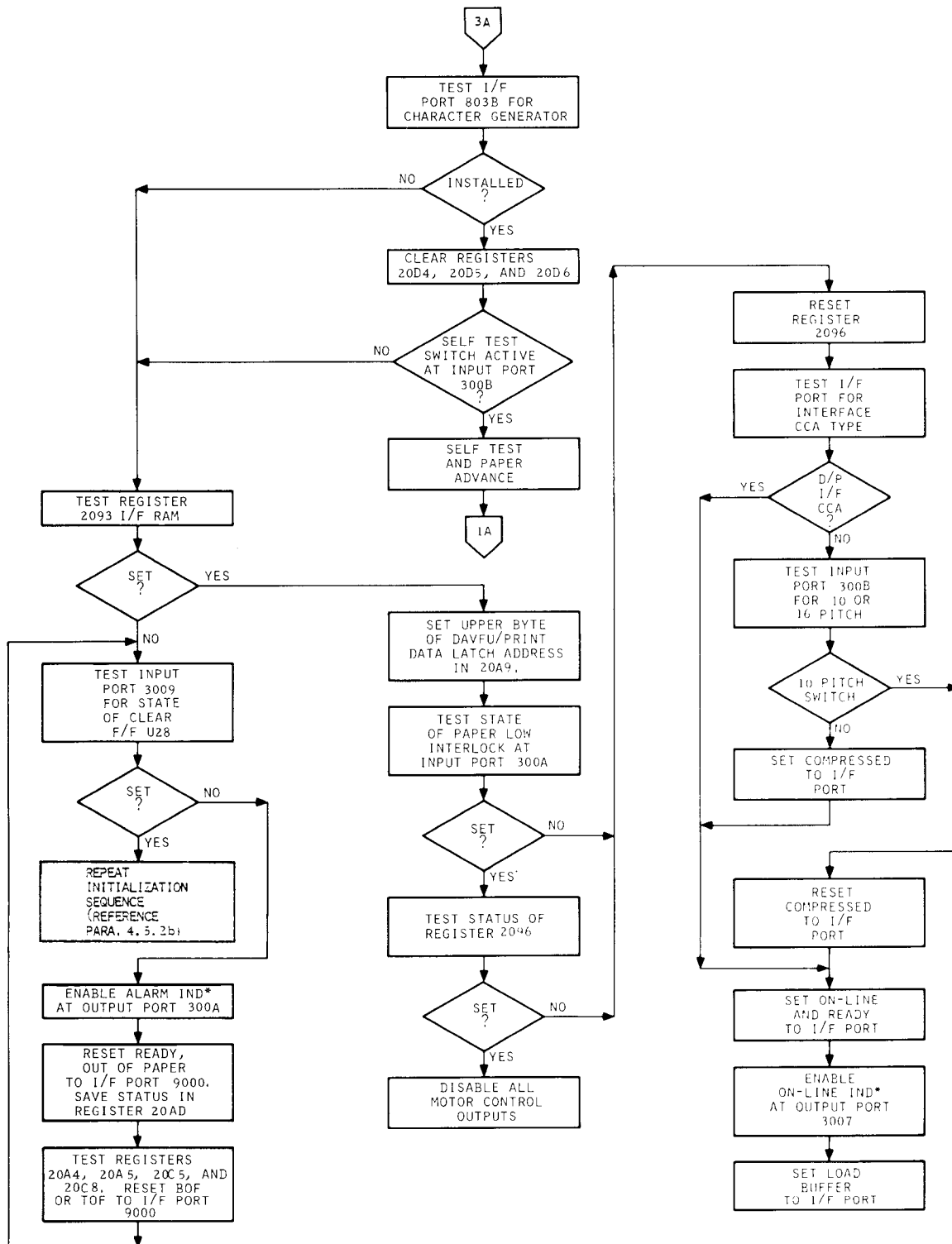
Communication between the Processor CCA and the Interface CCA takes place over the DBUF bus. Each of the interface types described in paragraph 4.4 contains devices which are addressable by the CPU and Control Section.

As shown in figure 4-29, a given device is enabled for input or output by the CPU and Control Section of the Processor CCA issuing a 15-bit (bit 10 is not used) address over the address bus. Each Interface CCA converts address bits A11-A13 into a unique chip select pulse (CS1* - CS9*) as listed in table 4-14. Address bit A15 (bit 14 is 0) must be true when any interface port device chip select pulse is generated.



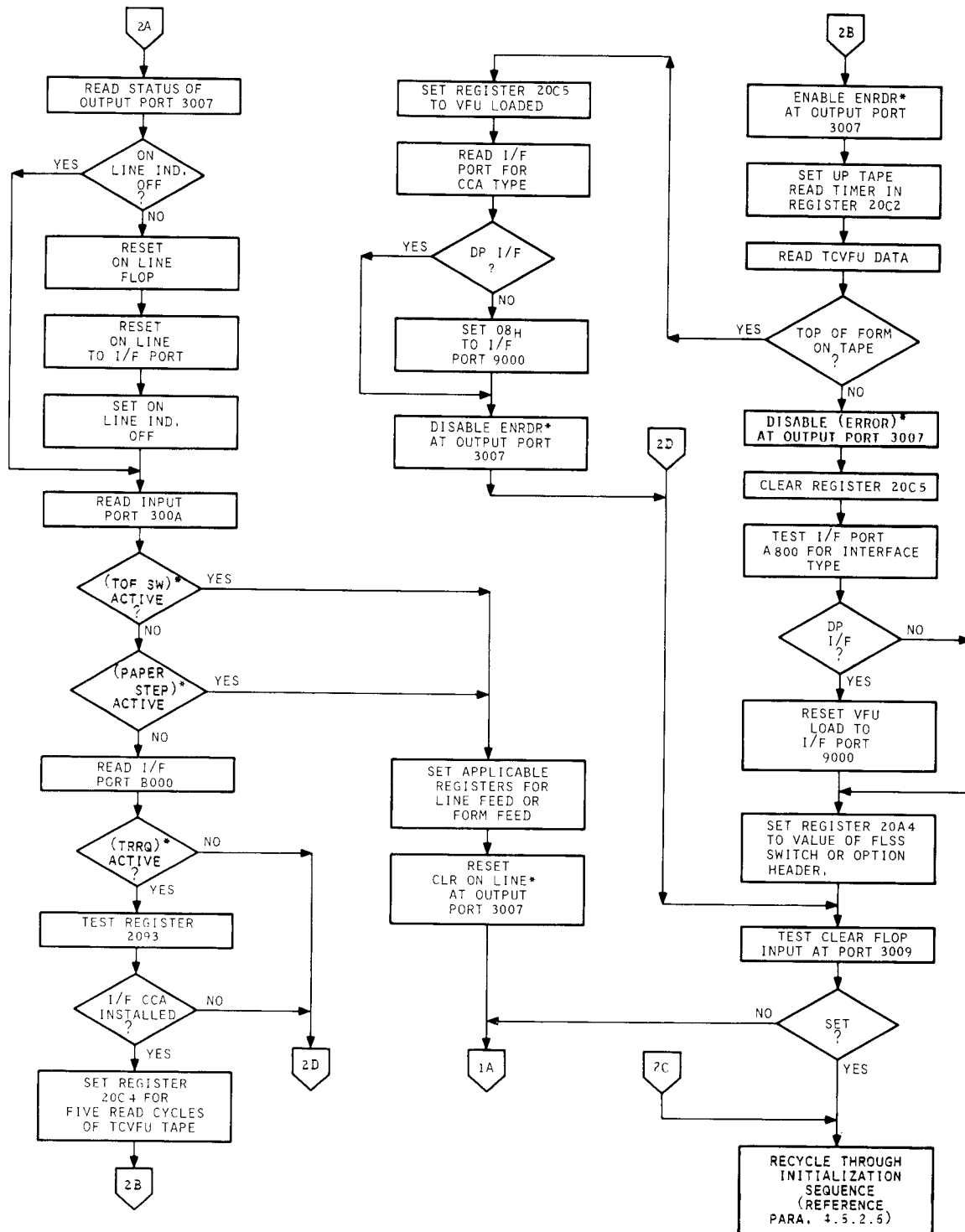
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Figure 4-28A. Operating Status Verification Flow Diagram



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Figure 4-28B. Operating Status Verification Flow Diagram



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Figure 4-28C. Operating Status Verification Flow Diagram

TABLE 4-14. INTERFACE PORT DEVICE SELECTION

Address Bus Bit Configuration																Chip Select Signal	Enable Function
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
1	0	0	0	0		0	0	0	0	0	0	0	0	0	0	CS1*	Read and Write to VFU/Print
1	0	0	0	1		0	0	0	0	0	0	0	0	0	0	CS2*	Read last address counter value
1	0	0	1	0		0	0	0	0	0	0	0	0	0	0	CS3*	Interface Status Latch
1	0	0	1	1		0	0	0	0	0	0	0	0	0	0	CS4*	TCVFU Driver (upper byte)
1	0	1	0	0		0	0	0	0	0	0	0	0	0	0	CS5*	Not Used
1	0	1	0	1		0	0	0	0	0	0	0	0	0	0	CS6*	Interface Status Latch
1	0	1	1	0		0	0	0	0	0	0	0	0	0	0	CS7*	TCVFU Driver (lower byte)
1	0	1	1	1		0	0	0	0	0	0	0	0	0	0	CS8*	Option Header Driver
1 = Logic High State 0 = Logic Low State * = Active in Logic Low State A Read or Write command must be active																	

Address bit A15 is inverted on the Processor CCA to generate active low pulse A15*, which is used to enable interface port transceiver U20. With U20 enabled, the CPU and Control Section controls the transfer of information between the internal D bus and the external DBUF bus.

Descriptions of the interaction of the various devices with the DBUF bus are provided in the applicable Interface CCA description.

a. Interface Port Address and DBUF Bit Assignments

The hexadecimal addresses of the various interface devices are sequentially listed below. Included are definitions for the bit assignment of each device.

1. Address 8800H - VFU/Print Data Address Counter - An input latch which indicates the location in the I/F CCA VFU/Print Data Line Buffer where data is stored.

2. Address 9000H - Interface Control Latch - The DBUF bit numbers, signal names, and functions are listed as follows:



Figure 4-29. Processor CCA Interface Port Communications Functional Block Diagram

THEORY OF OPERATION

DBUF Bit No.	Signal	Function
1	LOAD BUFFER	Informs the Interface CCA to start loading the print buffer.
2	READY	Informs the Interface CCA that the Processor CCA is ready to go on line or off line.
3	ON LINE	Informs the Interface CCA whether the Processor CCA is in the on line or off line mode.
4	TOP OF FORM (TOF)	Informs the Interface CCA that the Top of Form position has been detected.
5	BOTTOM OF FORM (BOF)	Informs the Interface CCA that the Bottom of Form position has been detected.
6	PAPER MOVING	Informs the Interface CCA that paper is moving.
7	CONDENSED	Informs the Interface CCA that the condensed 16 pitch switch is active.
8	PAPER EMPTY (PE)	Informs the Interface CCA that the Paper Low Interlock is active.

4. Address A800H - Interface Status - The DBUF bit numbers, signal names, and functions are listed as follows:

DBUF Bit No.	Signal	Function
1	BUFFER FULL	Informs the Processor CCA that the Interface CCA has completed a load cycle.
2	ON LINE ACK	Acknowledges the ON LINE/OFF LINE status generated by the Processor CCA.
3	DAVFU FAULT	Informs the Processor CCA that the DAVFU load cycle has a fault, or that a parity error exists.
4	DAVFU/PRINT*	Informs the Processor CCA whether the loaded information is DAVFU or print data.

DBUF Bit No.	Signal	Function
5	SAT*	Informs the Processor CCA that the Interface CCA is selected (DPC Centronics-Compatible Interface Only).
6	CONDENSED	Informs the Processor CCA that the line loaded was transmitted with a CONDENSED code.
7	EXPANDED	Informs the Processor CCA that the line loaded was transmitted with an EXPANDED code.
8	DPC/CENT*	Informs the Processor CCA whether the Dataproducts or DPC Centronics-Compatible Interface is present in the printer.

5. Address B000_H - TCVFU Status - The DBUF bit numbers, signal names, and functions are listed as follows:

DBUF Bit No.	Signal	Function
1	CH1	Channel 1 of the TCVFU Reader
2	CH2	Channel 2 of the TCVFU Reader
3	CH3	Channel 3 of the TCVFU Reader
4	CH4	Channel 4 of the TCVFU Reader
5	CH5	Channel 5 of the TCVFU Reader
6	CH6	Channel 6 of the TCVFU Reader
7	TRRQ*	Informs the Processor CCA of the status of the TCVFU Reader switch.
8	CH13	TCVFU Reader strobe pulse.

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6. Address B800H - Header Status - The DBUF bit numbers, signal names, and functions are listed as follows:

DBUF Bit No.	Signal	Function															
1	(CONDENSED EN)*	Informs Processor CCA that condensed print option is enabled.															
2	(AUTO LINE EN)*	Informs the Processor CCA that automatic line feed option is enabled.															
3	(DAVFU EN)*	Informs the Processor CCA that the DAVFU option is enabled.															
4	(PERF SKIP #1)* (PERF SKIP #2)*	These two bits are coded to indicate to the Processor CCA the amount of perforation skipover required. <table border="1"> <thead> <tr> <th>Perf. Skip #1</th><th>Perf. Skip #2</th><th>Lines of Skipover</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>3</td></tr> <tr> <td>0</td><td>1</td><td>4</td></tr> <tr> <td>1</td><td>0</td><td>6</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	Perf. Skip #1	Perf. Skip #2	Lines of Skipover	0	0	3	0	1	4	1	0	6	1	1	0
Perf. Skip #1	Perf. Skip #2	Lines of Skipover															
0	0	3															
0	1	4															
1	0	6															
1	1	0															
6	11/12*FORM EN	Conditions the Processor CCA to compute number of print lines on form based on either 11 (high) or 12 (low) inches.															
7	PLOT EN	Not Used.															
8	(EXPANDED DIS)*	Informs Processor CCA that expanded print option is disabled.															

b. Data Transfer

On completion of the Operating Status Verification sequence, LOAD BUFFER is set to Interface Port 9000H, and Registers 20C2 and 20C3 are set to 350 milliseconds. If BUFFER FULL* does not become active within the 350 millisecond load window, the I/O ports will be enabled to perform a shuttle park operation (see subparagraph C1).

When BUFFER FULL* becomes active, the value of Interface port 8800 is read to determine the location in the Interface VFU/PRINT data line buffer where the termination code is stored.

NOTE

For printers configured with a Serial Interface CCA, Location 00 of the VFU/PRINT data line buffer is read to determine the location of the termination code.

During the time that data is read from Interface Port 8000_H, LOAD BUFFER is disabled at Interface Port 9000_H.

4.5.4 I/O Port Communication and Control (Figures 4-30 and 4-31)

The Processor CCA uses nine I/O port devices to communicate with the control panel and the Wire Driver and Motor Driver CCAs. As shown in the functional flow block diagram, figures 4-30 and 4-31, each port device is assigned a hexadecimal address which corresponds to an eight-bit register location in the Status and Data Register (see paragraph 4.5.2).

a. I/O Port Enable Codes

The CPU and Control Section communicates with each I/O port device by issuing a unique 16-bit address code which is decoded into an enabling chip select signal as listed in table 4-12. The communication path between the CPU and Control Section and the individual I/O port device is completed by U15, which operates in either the transmit or receive code.

Table 4-15 lists the chip select signals, their address bus bit configurations, and enable functions.

TABLE 4-15. I/O DEVICE ENABLE SIGNALS

Address Bit Configuration 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																Chip Select Signal	Enable Function
0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	CS5*	Status & Data Register U11, U12
0	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	CS6*	I/O Port Transceiver U15
0	0	1	1	0	X	X	X	X	X	X	0	0	0	0	0	CS7*	Output Port U32
0	0	1	1	0	X	X	X	X	X	X	0	0	0	1	0	CS8*	Output Port U33
0	0	1	1	0	X	X	X	X	X	X	0	0	1	0	0	CS9*	Output Port U35
0	0	1	1	0	X	X	X	X	X	X	0	0	1	1	0	CS10*	Output Port U34
0	0	1	1	0	X	X	X	X	X	X	0	1	0	0	0	CS11*	Input Port U22
0	0	1	1	0	X	X	X	X	X	X	0	1	0	1	0	CS12*	Input Port U21
0	0	1	1	0	X	X	X	X	X	X	0	1	1	0	0	CS13*	Input Port U19
0	0	1	1	0	X	X	X	X	X	X	0	1	1	1	0	CS14*	Output Port U16
0	0	1	1	0	X	X	X	X	X	X	1	0	0	0	0	CS15*	Output Port U18
0	0	1	1	0	X	X	X	X	X	X	1	0	1	0	0	CS16*	Interface Port Transceiver U20
1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	-	Interface CCA Enable
1 = Logic High State																X = Don't Care	
0 = Logic Low State																* = Active when in the Low State	

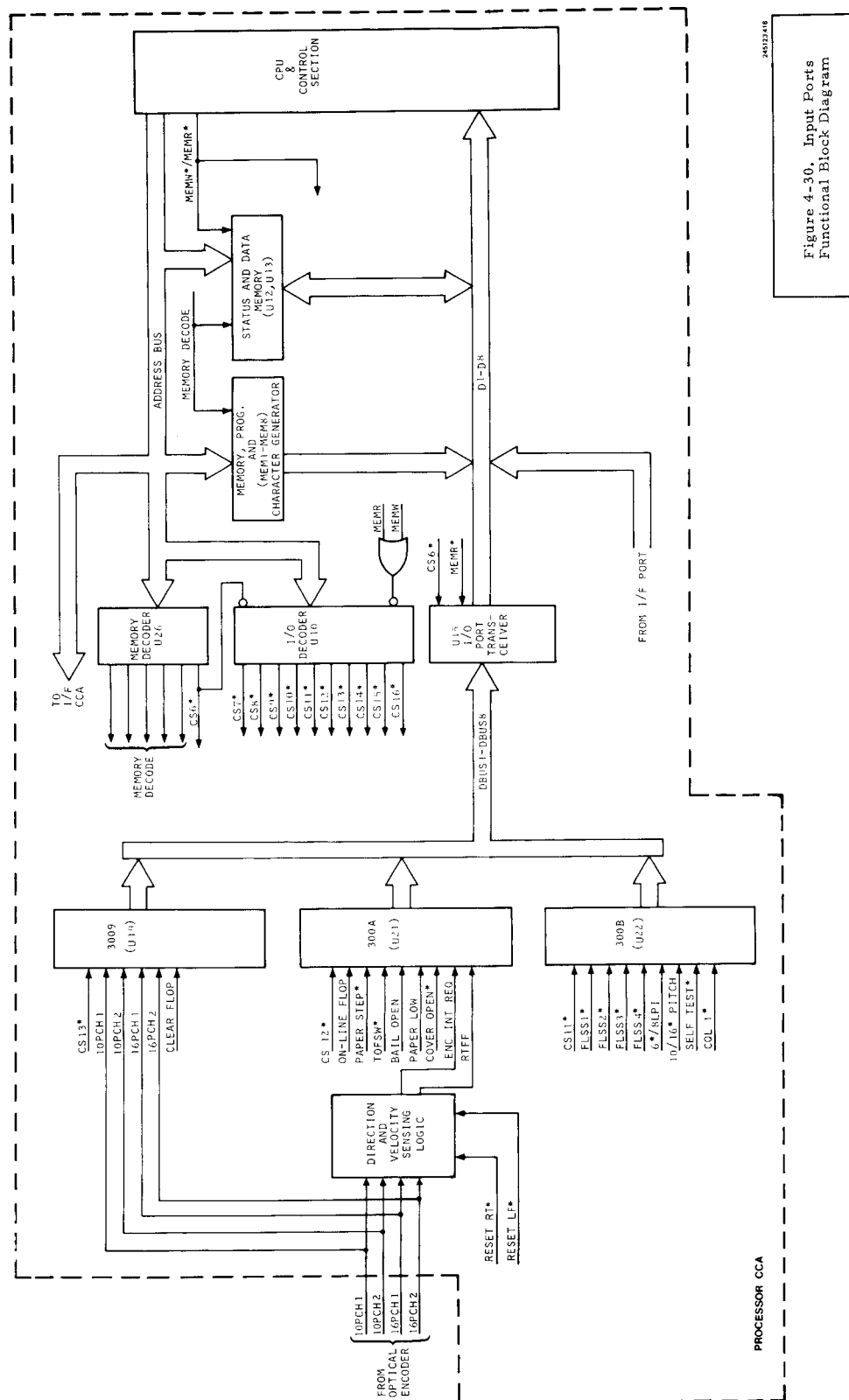
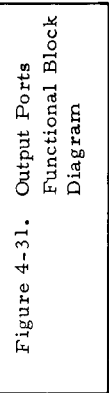


Figure 4-30. Input Ports Functional Block Diagram



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I/O port transceiver U15 is enabled when CS6*, the output from memory decoder U26, is in the logic low state. The transmit/receive mode is controlled by the logic state of the signal MEMR* output from the CPU and Control Section. As shown in figure 4-30, the CS6* pulse is used to enable the I/O port address decoder. The I/O port address decoder U10 receives the decoded four least significant bits of the address bus and outputs a unique decoded I/O device enable chip select signal pulse (CS7* - CS15*). The CS16* output from the I/O decoder is ORed with address bit A15*, which enables the interface port transceiver U20 when interface port communication is performed.

To control paper advance, ribbon advance, shuttle movement, and print wire firing, the CPU and Control Section will issue a unique address for the applicable I/O port device. The address decoder, enabled by either a read MEMR* or a write MEMW* command, will decode the address into a specific chip select pulse. When the various I/O port devices are enabled, the CPU and Control Section can manipulate the outputs and read the input when controlling any of the above mentioned functions.

b. I/O Port Signal Definitions

The hexadecimal addresses of the various I/O port devices are sequentially listed below. Included are definitions for the assignment of each bit interconnected with the DBUS.

1. Address 3007_H

DBUS Bit	Signal	Definition
8	RESET*	Used to reset the Interface CCA.
7	RCLRFF*	Used to clear the right clear flip flop.
6	ALARM IND*	Used to turn the ALARM/CLEAR switch indicator lamp on or off
5	ON LINE IND*	Used to turn the ON/OFF LINE indicator on or off
4	RESET LF*	Used to clear the left sensing flip flop
3	RESET RF*	Used to clear the right sensing flip flop
2	ENRDR*	Used to enable the TCVFU reader
1	CLR ON LINE*	Used to clear the on line flip flop

2. Address 3008_H

DBUS Bit	Signal	Definition
8	RMTR*	Used to enable the ribbon advance motor
7	10/16 SHTL*	Used to select shuttle travel velocity which corresponds to print density (pitch)
6	RIGHT/LEFT*	Indicates the direction in which the shuttle will move.
5	GO/STOP*	Indicates whether the shuttle will stop or go.

2. Address 3008_H

DBUS Bit	Signal	Definition			
4	STEP	Used to apply power to the paper stepper motor.			
3	01* - 03*	Paper step phase signals used to move paper as follows:			
		ϕ_3	ϕ_2	ϕ_1	Paper Moved
		0	1	1	One Step
		1	1	0	One Step
		1	0	1	One Step
		0	1	1	One Step

3. Address 3009_H

DBUS Bit	Signal	Definition
5	CLRFF	Indicates the state of the clear flip flop.
4	16PCH2	Indicates the data output from the optical encoder.
3	16PCH1	Indicates the data output from the optical encoder.
2	10PCH2	Indicates the data output from the optical encoder.
1	10PCH1	Indicates the data output from the optical encoder.

4. Address 300A_H

DBUS Bit	Signal	Definition
8	RTFF	Right flip flop used to indicate when the shuttle is moving in the right (active high) or left (active low) direction.
7	ENCS	Used to indicate an encoder mark (the logical ORed outputs of the right and left flip flops).
6	COVER OPEN*	Indicates when the cover is open.
5	PAPER LOW	Indicates when the printer is out of paper.
4	BAIL OPEN	Indicates when the bail is open.
3	TOFSW*	Indicates the position of the TOP OF FORM switch.
2	PAPER STEP*	Indicates the position of the PAPER STEP switch.
1	ON LINE FLOP	Indicates the status of the on line flip-flop.

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5. Address 300B_H

DBUS Bit	Signal	Definition				
8	COL 1*	Column 1 sensor - used to indicate that the shuttle position is right of column 1. Indicates the position of the TEST switch. Indicates the position of the horizontal pitch switch. Indicates the position of the vertical pitch switch. Indicates the position of the forms length switch as follows:				
7	SELF TEST*					
6	10/16 PITCH*					
5	6/8 LPI*					
4-1	FLSS4* to FLSS1*					
		FLSS4	FLSS3	FLSS2	FLSS1	LPI
		0	0	0	0	11
		0	0	0	1	3
		0	0	1	0	3½
		0	0	1	1	4
		0	1	0	0	5½
		0	1	0	1	6
		0	1	1	0	7
		0	1	1	1	8
		1	0	0	0	8½
		1	0	0	1	11
		1	0	1	0	12
		1	0	1	1	14
		1	1	0	0	11
		1	1	1	0	11
		1	1	1	1	11

6. Address 300C_H

DBUS Bit	Signal	Definition
8-1	7L* to 1L*	Individual print wire control signals used to drive the left column print wires.

7. Address 300D_H

DBUS Bit	Signal	Definition
8-1	7L* to 1L*	Individual print wire control signals used to drive the left column print wires.

8. Address 300E_H

DBUS Bit	Signal	Definition
8-1	7R* to 1R*	Individual print wire control signals used to drive the right column print wires.

9. Address 300F_H

DBUS Bit	Signal	Definition
8-1	7R* - 1R*	Individual print wire control signals used to drive the right column print wires.

c. Print Head Shuttle Control (Figures 4-30, 4-31, and 4-32)

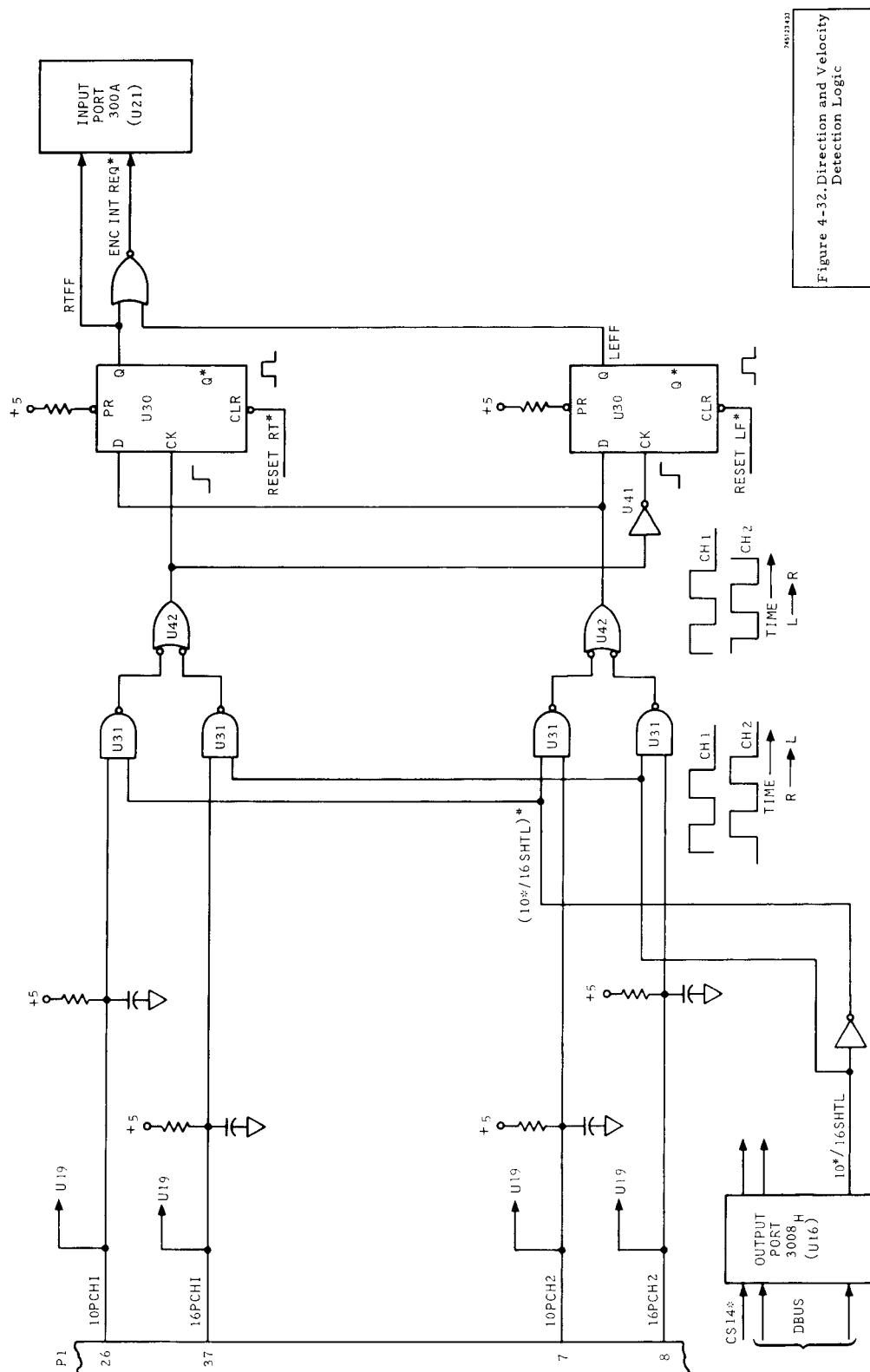
The print head is transported across the print station by a belt-driven shuttle mechanism assembly. The shuttle mechanism drive belt is coupled to the shaft of a velocity controlled DC motor. The Processor CCA uses output ports 3008_H (see figure 4-31) to control the motor rotation rate and direction. Output port 3007_H is used to initialize the internal logic, which detects shuttle rate. Input ports 3009_H, 300A_H, and 300B_H (see figure 4-30) are used to input shuttle-to-platen data, velocity rate, print wire firing of synchronous pulses, and direction of shuttle travel.

To initiate shuttle motion for a given direction and to control the travel velocity, the Processor CCA uses RIGHT*/LEFT and 10*/16 at output port 3008_H (see figure 4-31) to communicate with the Motor Driver CCA. Signal 10*/16 is also input at port 300B_H and is used by the Processor CCA to compute end zone reference points for reversing shuttle motion. Signals RESET RT* and RESET LF* at output port 3007_H (see figure 4-31) are used to clear the velocity and direction sensing logic internal to the Processor CCA.

When shuttle motion is in progress, the optical encoder assembly transfers a pulse train to the Processor CCA that indicates shuttle velocity. The pulse train (10PCH1, 10PCH2, or 16PCH1, 16PCH2) is input onto the Processor CCA at port 3009_H (see figure 4-30) and to the Direction and Velocity logic network (see figure 4-32). Encoder inputs at 3009_H are used to detect direction of travel when shuttle parking is to be performed (refer to subparagraph 1).

The encoder inputs to the Direction and Velocity Sensing Network (see figure 4-32) are used to develop the CPU and Control Section interrupt signals ENC INT REQ* and right/left status pulse RTFF. These signals are transferred to input port 300A_H and are used to synchronize shuttle velocity, and direction with print wire firing.

The 10/16*PITCH and COL 1* signals at input port 300B (see figure 4-32) are used to determine the switch setting for shuttle velocity and to detect when the shuttle is at the column one position near the left end frame.



To control shuttle movement, the Processor CCA will first park the shuttle at a referenced home position and initialize internal control logic. Next, an active signal BUFFER FULL* from the interface port will cause the CPU and Control Section to seek the current shuttle position and move the shuttle to the nearest print position.

1. Parking the Shuttle at the Home Position
(Figures 4-30 and 4-31) - Refer to figure 9-15 in volume II of this manual. Parking the shuttle at the home position is performed under any of the following conditions:

- (a) When the POWER switch is reset.
- (b) When the shuttle velocity and pitch setting do not agree.
- (c) When a DAVFU fault is detected at the Interface CCA.
- (d) When a DAVFU Code is received and the DAVFU option is not enabled.
- (e) When a change in the state of the ON LINE switch occurs.
- (f) When a STOP command is generated because of a malfunction.

When shuttle parking is to be performed, the CPU and Control Section will first initialize a no-shuttle motion timer (Status and Data Registers 20C2_H and 20C3_H). Next, the interrupt input signal ENC INT REQ* is disabled. The status of output port 3008_H is then tested to determine the logic state of GO*/STOP. If GO*/STOP is in the low state, input port 300B_H is then enabled to read the status of COL 1*. If the COL 1* input is at the high state, output port 3008_H is enabled. RIGHT*/LEFT is forced to the high state, and the no-motion timer is decremented until COL 1* switches to the low state. If the timer should time out before COL 1* switches low, all the control signals interfacing the motor driver power circuits will be disabled. When COL 1* switches to the low state, input port 3009_H is enabled and the 10 PCH2 input is monitored until a low-to-high transition occurs. The low-to-high transition will cause the CPU and Control Section to force the RIGHT*/LEFT output of port 3008_H low.

When the status of GO*/STOP indicates a high state, the state of COL 1* is input. If COL 1* is in the high state, the RIGHT*/LEFT output of port 3008_H is forced high, the status is stored in the Status and Data Register, and the motion timer is decremented until COL 1* switches low. If the timer should time out before COL 1* switches low power to all drive motors will be disabled.

A low transition of COL 1* will cause the RIGHT*/LEFT output of port 300B_H (see figure 4-31) to switch low. The low state of RIGHT*/LEFT will cause the 10PCH2 input to port 300B_H to be monitored for a low-to-high transition. When 10PCH2 switches high, implying that the shuttle is now moving to the right from the left end frame, the state of 10/16* at input port 300B is tested to determine travel velocity. The state of this signal will cause a set or reset state of 10*/16 SHTL at output port 3008_H (see figure 4-31). The status of 10*/16, indicating shuttle velocity, is stored in the applicable Status

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A low transition of COL 1* will cause the RIGHT*/LEFT output of port 300B_H (see figure 4-31) to switch low. The low state of RIGHT*/LEFT will cause the 10PCH2 input to port 300B_H to be monitored for a low-to-high transition. When 10PCH2 switches high, implying that the shuttle is now moving to the right from the left end frame, the state of 10/16* at input port 300B_H is tested to determine travel velocity. The state of this signal will cause a set or reset state of 10*/16 SHTL at output port 3008_H (see figure 4-31). The status of 10*/16, indicating shuttle velocity, is stored in the applicable Status and Data Register. This velocity will remain fixed and used as the reference speed for print wire firing unless the print format option is changed (see paragraph 4.5.4, subparagraph c2).

The COL 1* input is then tested for a low-to-high transition (shuttle leaving the column one position). If the shuttle motion timer (Status and Data Registers 20C2 and 20C3) should zero out before COL 1* changes state, power to all motors is disabled. When COL 1* switches high, the RESET LF* and RESET RT* outputs from port 3007_H (see figure 4-31) are clocked into flip-flop U30 (see figure 4-32) to clear the LEFF and RTFF outputs from Status and Data Register 2090 each time an interrupt is generated. LEFF is ORed with RTFF to generate interrupt signal ENC INT REQ* for each dot column the shuttle traverses.

After clearing the LEFF and RTFF flip-flops, the dot column counter is cleared to zero (Status and Data Register 2090), and simultaneously, a 17D is loaded into the character column counter (Status and Data Register 2091). At the same time, signal ENC INT REQ* is enabled for counting dot columns, and as the shuttle is moving, every tenth RTFF will increment or decrement the character column counter. With the shuttle moving to the right from the left end frame, the character column counter will be incremented. When a count of 36D is reached, the RIGHT*/LEFT output of port 3008_H (see figure 4-31) will switch to the high state, causing the shuttle to reverse direction toward the left. The 10PCH2 input at port 3009_H is then monitored for a low-to-high transition. When the transition is detected, the CPU and Control Section will enable output port 3008_H (see figure 4-30) and set GO*/STOP to the high state. When in the high state, GO*/STOP will disable power to the shuttle motor drive circuit on the Motor Driver CCA. The shuttle is then parked at the home position, and the shuttle control logic is initialized.

After initializing the shuttle at the home position, the CPU and Control Section will wait for a buffer full condition at the interface port. A buffer full condition will cause the CPU and Control Section to enable the shuttle motor drive circuitry and move the shuttle to the nearest print position.

2. Velocity Direction Control (Figure 4-32) - The standard printer has a velocity of 34 inches per second (IPS), which is the reference velocity for printing at ten characters per inch (CPI). Printers configured with the optional 10/16 PITCH switch have a velocity of 20.4 IPS for the 16 pitch setting (16 CPI). When the Condensed Print option is enabled, shuttle velocity is 20.4 IPS, and is 34 IPS when the Expanded Print option is enabled. Either velocity is maintained for each print line unless the 10/16 PITCH switch setting is changed or unless a change is detected in the logic states of the CONDENSED and EXPANDED bits at interface status latch A800_H (see figure 4-29).

Referring to figure 4-32, the logic state of 10*/16 SHTL output from port 3008_H is set during shuttle parking and initialization (see paragraph 1 above). The 10*/16 SHTL signal is Nanded with encoder output signals 10PCH1 and 10PCH2, or 16PCH1 and 16PCH2. The logic state of 10*/16 SHTL determines which encoder output will be analyzed for shuttle direction.

The frequency of either 10 pitch or 16 pitch pulse train will specify the shuttle travel velocity. A pulse is generated for each instance the encoder assembly, attached to the shuttle, intersects an imaginary dot column position on the platen. When shuttle motion is in progress, to perform a print operation, the encoder outputs over channel 1 are used to clock the channel 2 pulse train through flip-flop U30. The right sensing output (RTFF) and left sensing output (LEFF) are ORed to generate the CPU and Control Section interrupt signal ENC INT REQ*.

Signal ENC INT REQ* is generated every 294 microseconds, which the CPU and Control Section uses as an index for synchronizing print wire firing. Signal RTFF is the dot column count, and depending on shuttle travel direction, will increment or decrement Status and Data Register 2090_H (dot column counter). Every tenth increment or decrement of the dot column count will cause an increment or decrement of the character column count in Status and Data Register 2091_H (character column counter). The CPU and Control Section reads the content of these registers to determine shuttle horizontal position.

To compute the shuttle's travel direction, the leading edge of pulse 10PCH1 or 16PCH1 is used as a reference to analyze the pulse transitions received on channel 2. If the pulse on channel 2 is high when the leading edge of channel 1 is switched from low to high, the LEFF output is cleared and RTFF output from U30 will be set. This condition indicates that the shuttle is traveling in the direction of left end frame. This condition will cause the RTFF output to be cleared and the LEFF to be set.

The direction in which the shuttle travels to perform a print operation depends upon the location of the print characters stored at I/F port 8800_H (see figure 4-30). When the status of I/F port A800_H indicates that the buffer is full and contains print data, I/F port 8800_H is interrogated for the presence of first and last print characters. The CPU and Control Section translates this data into start of line (SOL) and end of line (EOL) and stores the computed values in the allocated Status and Data Registers. The CPU and Control Section compares the contents of the character column count register with the SOL and EOL registers to determine shuttle position with respect to character print position. The computed value logic state of RIGHT*/LEFT controls the operation of the reversing amplifier located on the Wire Driver CCA. The reversing amplifier will cause the shuttle mechanism drive motor to rotate in the correct direction. When in motion, the encoder will output pulse train 10PCH or 16PCH, which is analyzed for direction and velocity.

When the shuttle mechanism is computed to be at the last dot column of the last character column to be printed, the CPU and Control Section will set or reset the RIGHT*/LEFT output of Output Port 3008_H, reversing the direction of motion of the shuttle drive motor. During the time period when the shuttle mechanism is turning around (60 milliseconds maximum, if

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velocity is 20.4 inches per second, or 100 milliseconds if the velocity is 34 inches per second) the CPU and Control Section enables Interface Port Transceiver U20 and sets LOAD BUFFER to interface control latch 9000_H (see figure 4-30). If, during the turn-around time Interface Port A800_H responds with a buffer full condition (BUFFER FULL* active when low) Interface Port 8000_H (see figure 4-30) is again interrogated for start of line and end of line data. (During shuttle turn-around time, output port 3008_H is used to step paper).

d. Print Wire Firing

The print function controls the information output to the print head. Printing is performed by accessing the ASCII-coded character from Interface Port 8800 and converting the data into an address to access the character. This 8-bit address is used to fire a wire column. Four internal counters are used to keep track of the position of the left and right wires. These counters are CCCL, DCCL and CCCR, DCCR respectively, and are used with the ASCII character code to access the character generator. Updating of the internal counters with each encoder mark keeps track of the print head position.

The character generator is divided into two parts. One part is addressed for the right wires, and the other for the left wires. The address which accesses the character generator is made up of the dot column counter (DCCR for the right wire section; DCCL for the left wire section) and the ASCII character code. The address selects one of eight bytes of data for a particular character. The selected byte will then be used to turn on any wire of the vertical wire column (where the uppermost wire is the least significant bit of the addressed byte from the character generator). The three low order bits of the dot column counter will access any of the eight bytes of data for a particular character. The sixth bit will be used to access either side of the character generator. The ASCII seven-bit code will be used to access any of the 128 characters in the character generator.

When printing at 10 or 16 characters per inch, the left and right wire banks are updated with information every 294 microseconds, the period of one encoder mark. However, once a wire is fired, it must stay on for $355 + 5$ microseconds. For this reason, output ports 300D_H and 300C_H are used for left wire data. Output ports 300F_H and 300E_H are used for right wire data. Each pair of output ports are updated every 294 microseconds, with each individual output port of the left/right output port set being updated every 588 microseconds.

When printing at five characters per inch (expanded mode), the shuttle servo motor travels at the 10-characters-per-inch rate. However, every other encoder mark is skipped, and the same dot column information is printed twice. This effectively expands the width of the character to 20 encoder marks. Of these, 14 are allotted for dot information and six for inter-character spacing. Also, since updating is only required on every other encoder mark, only one latched port in each pair is used: LB and RB.

e. Ribbon Advance

Ribbon motion is initiated by the Processor CCA at the start of the shuttle or paper motion cycle through the ribbon drive system of the Motor Driver CCA.

f. Paper Advance Control (Figures 4-30 and 4-31)

Each time the printer is powered up, the CPU and Control Section will first initialize the paper advance controls. The CPU and Control Section first locks the paper feed stepper motor into phase one. This is accomplished by enabling U15 and setting the DBUS to a B3_H. The B3_H output from U15 is placed on the DBUS, the CPU and Control Section enables Output Port 3008_H, and the content of the DBUS is output to the Motor Driver CCA. The low state of STEP* and Ø3* will energize the motor and start motor movement. After 4 milliseconds, the Ø3* signal is reset to high (inactive) and the Ø1* signal is set low (active), causing motor rotation to Phase 1. The STEP* signal is then reset high, de-energizing the motor in Phase 1. Upon completion of initialization of the stepper motor control circuitry, the CPU and Control Section loads Status and Data Register 20BD_H with the status of Output Port 3008_H.

Next, the CPU and Control Section computes the Top of Form position from the total number of printable lines on the form and from the perforation skip code. To do this, the CPU and Control Section reads the applicable bits of the option header via the option header driver B800_H and I/F Port Transceiver (see figure 4-30). The CPU and Control Section detects the logic state of DBUF4 and DBUF5 to compute the number of lines to be skipped when performing perforation skipover and stores the computed value into Status and Data Register 20A8_H. If the printer is configured with the optional 6/8 CPI and Form Length Select switches (FLSS), the CPU and Control Section enables I/O Port Transceiver U15 and reads the content of Input Port 300B_H (U22). The logic state of DBUS5 establishes the line density (6 or 8 lines per inch), and is used to compute the total number of lines remaining on the form as specified by the logic state of DBUS1 through DBUS4.

The value of the FLSS setting is saved in Status and Data Register 20A5_H and loaded in Status and Data Register 20A4_H, which is used as a counter for the number of print lines on the form.

In the standard printer, the CPU and Control Section enables both Interface Port Transceiver U20 and the Interface Bus Transceiver, and reads the logic state of DB6 output of the Option Header Driver B800_H. The logic high or low status of DB6 is input to the Processor CCA, indicating that the printer is configured to handle 11- or 12-inch forms, and is saved in Status and Data Register 2045_H. The 11- or 12-inch value is also loaded into Status and Data Register 20A4_H, which is used as a counter for the number of print lines on the form. When Top of Form is reached, the CPU and Control Section will then set the DBUF4 line high true to the Interface Control Latch 9000_H (figure 4-30) and will store the status in Status and Data Register 20AD_H.

After initializing the paper stepping motor control circuitry, and computing the perforation skip and/or forms length, the CPU and Control

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Section will then read the state of the applicable Status and Data Registers. These registers are re-initialized each time the CPU and Control Section is reset or a paper motion-related control panel switch setting is changed.

4.6 MOTOR DRIVER CCA (Figure 9-16, Volume II)

The Motor Driver CCA contains the drive circuitry for the print head shuttle servo motor, the paper feed stepping motor, and the ribbon drive motor. The column 1 sensing amplifier U11 and motion suppress circuits are also included. Output of U11 is used as an input to the Processor CCA for print head shuttle reset positioning and as a marker for determining print head turn-around at the left end zone and start of print line at the left margin. The motion suppress circuit U11 detects the power on condition and prohibits accidental printing, shuttle motion, and paper incrementing during power on or off.

4.6.1 I/O Signal Definitions

Table 4-16 lists the I/O signals and their functions.

TABLE 4-16. MOTOR DRIVER CCA SIGNAL DEFINITIONS

Name	Function
STEP*	Low True. When true, this input enables full power to be applied to the stepping motor for duration of stepping.
Ø1*	Low True. When true, this input turns on Phase 1 coil of stepping motor.
Ø2*	Low true. When true, this input turns on Phase 2 coil of stepping motor.
Ø3*	Low True. When true, this input turns on Phase 3 coil of stepping motor.
RM*	Low True. When true, this input turns on the ribbon motor.
10 PCH1	This input represents the 10 pitch encoder track, channel 1.
16 PCH1	This input represents the 16 pitch encoder track, channel 1.
10*/16 SHTL	This input selects the correct encoder track for the shuttle servo motor. If low, 10 PCH1 is selected; if high, 16 PCH1 is selected.
R*/L	This input directs the motion of the shuttle. Low commands right motion, high commands left motion. This signal should change only when shuttle speed has settled or is at zero.

TABLE 4-16. MOTOR DRIVER CCA SIGNAL DEFINITIONS (Contd)

Name	Function
DET POS	<p>This line represents the output of the "column one" sensor. (This is not a TTL signal).</p> <p>(1) The asterisk implies function is alive in the low state.</p> <p>(2) Unless otherwise specified, all signals are TTL levels.</p>

4.6.2 Circuit Operation

This paragraph describes the shuttle servo motor, paper feed stepping motor, and ribbon drive motor operation.

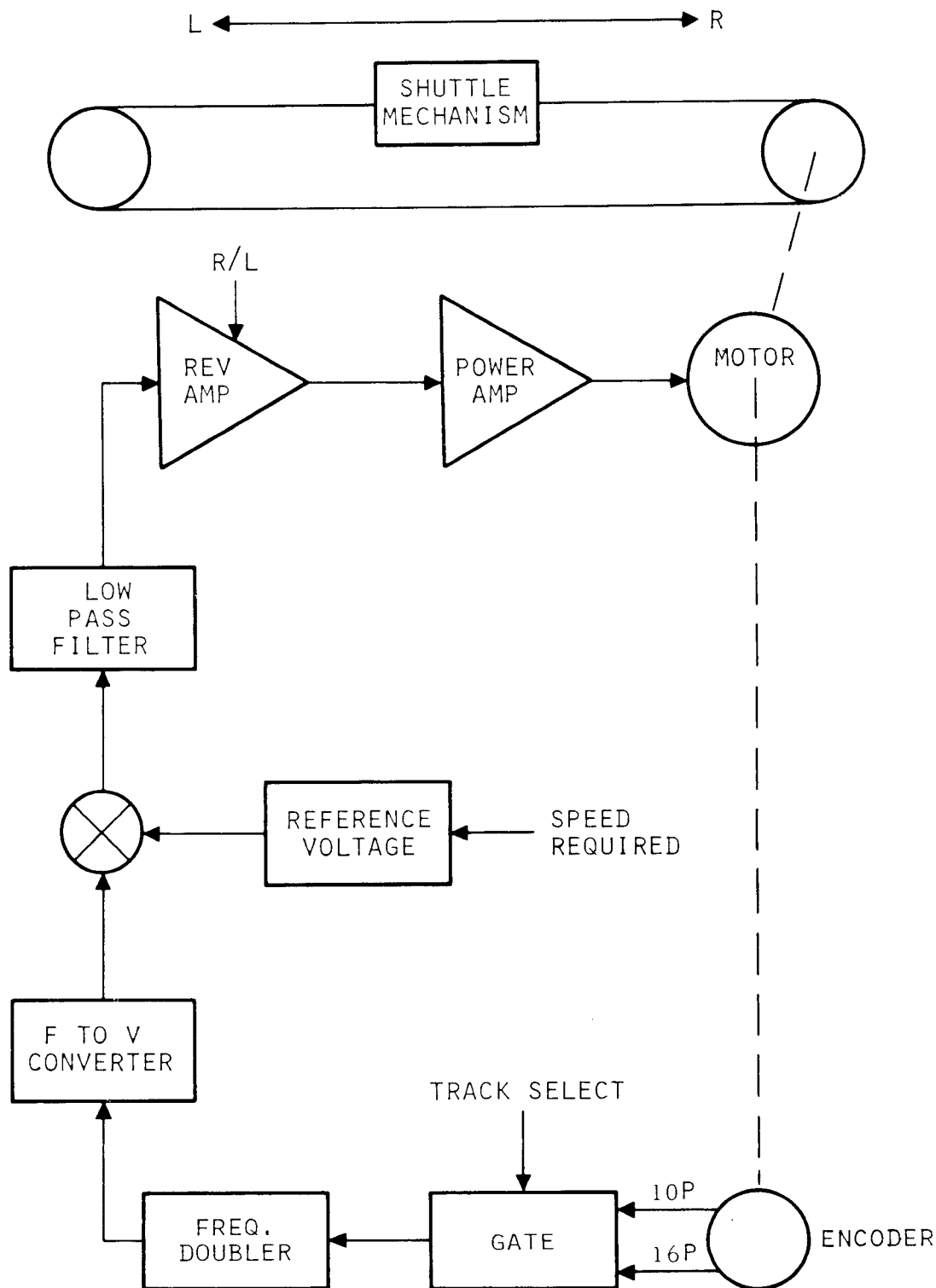
a. Shuttle Servo Motor Control (Figure 9-16, Volume II)

A velocity-controlled DC motor, via a pulley and belt, drives the shuttle mechanism across the print station. The Processor CCA commands the servo motor with respect to GO/STOP, RIGHT/LEFT, and 16 PITCH (HI) I0 PITCH (LO) speed. An optical incremental encoder, mounted on the motor shaft, provides information for firing the print solenoids, and the same encoder signals are used to derive velocity information for the servo motor. A block diagram of the shuttle servo motor is shown in figure 4-33.

Referring to figure 9-16, SH 2, the correct track from the encoder is selected at gates U14-3, U13-3, and U13-11, and is fed to an edge detector circuit U4-8, U4-6, effectively doubling the encoder input frequency. The pulses at U4-6 trigger U4-5, a one-shot whose average positive DC output at U4-11 is compared with a negative DC reference voltage at R5. The error is amplified and carrier-filtered by low-pass filters U1 and U2. U3 is a "reversing" amplifier whose gain is -1 or +1, depending on the L/R signal. The output of U3, limited by CR4 and CR5, is next fed to a current drive switching power amplifier. This self-oscillating amplifier, consisting of U7, Q7, Q13, Q4, and Q15, drives the motor from the +21V and -21V supplies. Current feedback is obtained from R26, which is in series with the motor. The switching amplifier operates between 20 and 25 kHz, to provide high power efficiency. Transistors Q3 and Q10 limit the current in the motor to avoid motor de-magnetization and excessive transistor current.

A re-triggerable one-shot at U10 is used to detect very slow movement or lack of shuttle motion if the GO command has been given. The one shot then times out, locks out further triggering, and causes U6-13 to go low, grounding the bases of Q7 and Q13, thus shutting off the motor drive. U10 is reset only when the GO signal changes to STOP.

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Figure 4-33. Shuttle Servo Motor Block Diagram

b. Paper Feed Stepping Motor Control

A three-phase motor is used to drive the tractor assembly. For six lines per inch, the motor moves four steps to get one line of paper movement (see timing diagram, figure 4-34), and moves three steps per line for eight lines per inch. Normally, one phase winding is kept energized to produce a holding torque. For slewing, stepping is carried out continuously. See the timing diagram shown in figure 4-35.

Assume that Phase 3 is energized. In this phase, Q3* is low, turning on Q2, which then turns on Q1. Current flows through CR21, the Phase 3 winding, Q1, and into the -21V supply. In this manner, the holding torque is produced. To step the motor, STEP* goes low, turning on Q12, and resulting in turning on Q11, thus applying +21V to the motor common winding and back-biasing CR21. At the same time, Phase 3 is turned off and Phase 1 is turned on with the full supply voltage across it. Keeping signal STEP* low, the motor is stepped in sequence to Phase 1, Phase 2, Phase 3, etc. To terminate the stepping sequence, STEP* goes high, turning off Q11. One phase is still left on, via CR21 and the -21V supply. Line AC, when high, inhibits any input signals to the stepping drive, suppressing any inadvertent movement during power on or power off.

c. Ribbon Motor Drive Control

When signal RM* goes low, Q14 is turned on, applying a +21 volts to the ribbon drive motor, which drives the ribbon in the ribbon cassette via a gear-head. The ribbon motor is actuated only during printing.

1. Column One Sense Amplifier - U11-2 is a comparator which translates the analog detection of the photo-sense signal at pin 4 to a TTL signal at pin 2. This signal is used by the Processor CCA.

2. Motion Suppress Circuit - Two comparators, U11-1 and U11-14, are used to detect power on and power off, respectively. Their outputs are collector ORed to give inhibit signals via U11-13 to the print head drivers and the paper feed drivers, and via CR19, to the shuttle servo motor drive. This prevents accidental printing, shuttle motion, or paper incrementing during power on and power off.

4.7 WIRE DRIVER CCA (Figure 9-17, Volume II)

The Wire Driver CCA contains 14 solenoid drive circuits which interface the Processor CCA with the print head. Each solenoid drive circuit controls an associated print wire solenoid housed in the print head assembly.

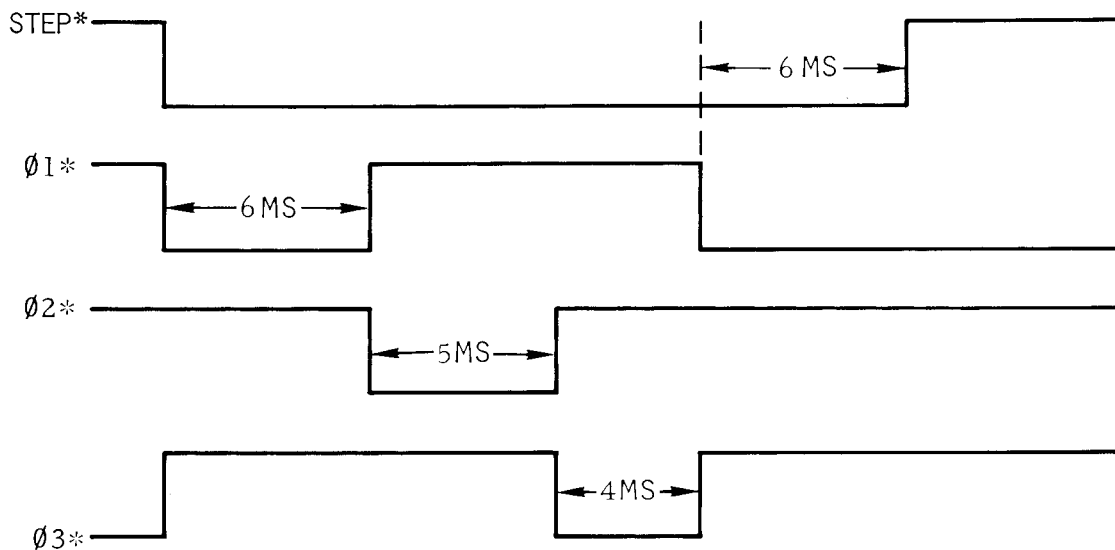
4.7.1 I/O Signal Definitions

Table 4-17 lists the I/O signals and defines their functions.

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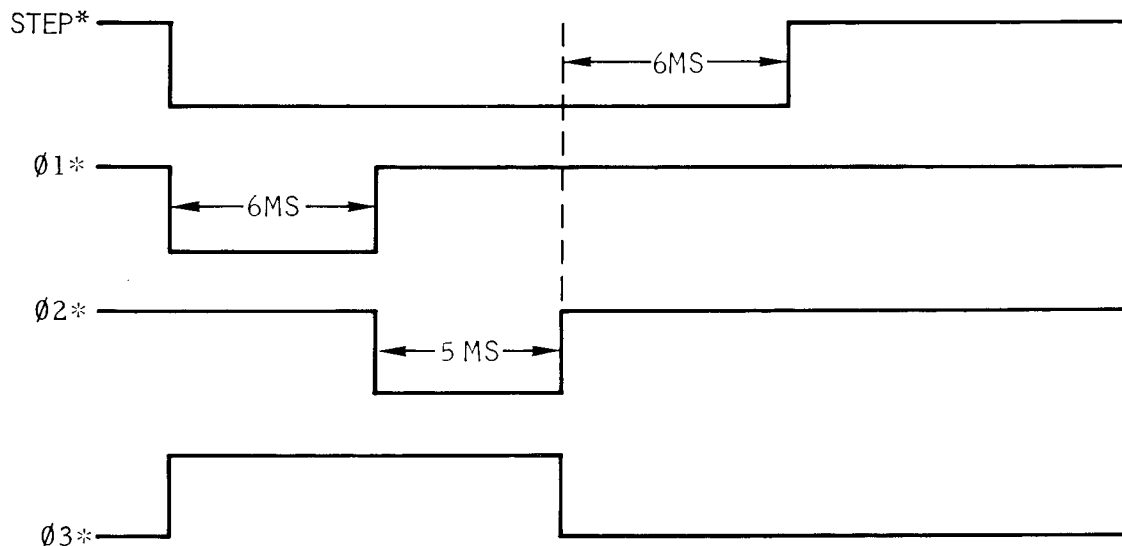
(A) FOR 6 LINES/INCH

TOLERANCE: $\pm 100 \mu\text{S}$



SEQUENCE: Ø3-Ø1-Ø2-Ø3-Ø1, Ø1-Ø2-Ø3-Ø1-Ø2, ETC.

(B) FOR 8 LINES/INCH

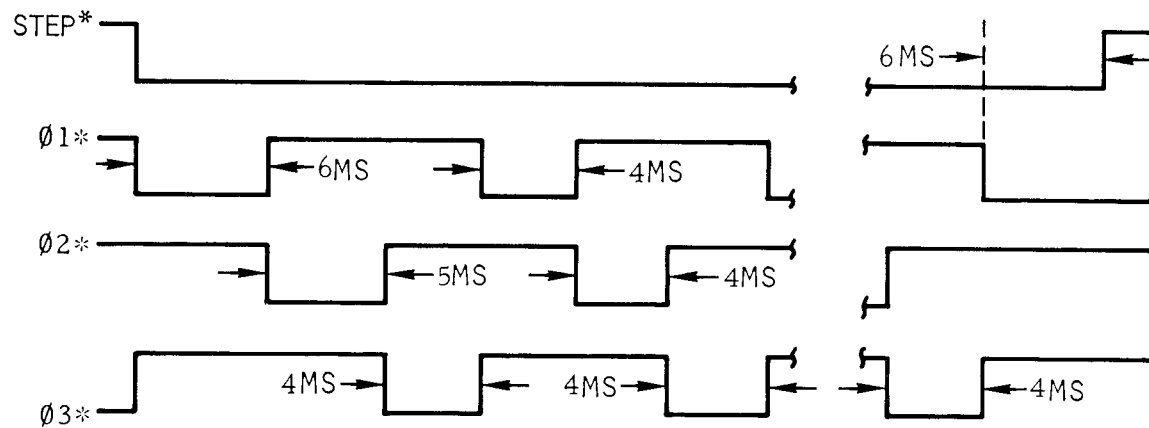


SEQUENCE: Ø3-Ø1-Ø2-Ø3-, Ø3-Ø1-Ø2-Ø3, ETC.

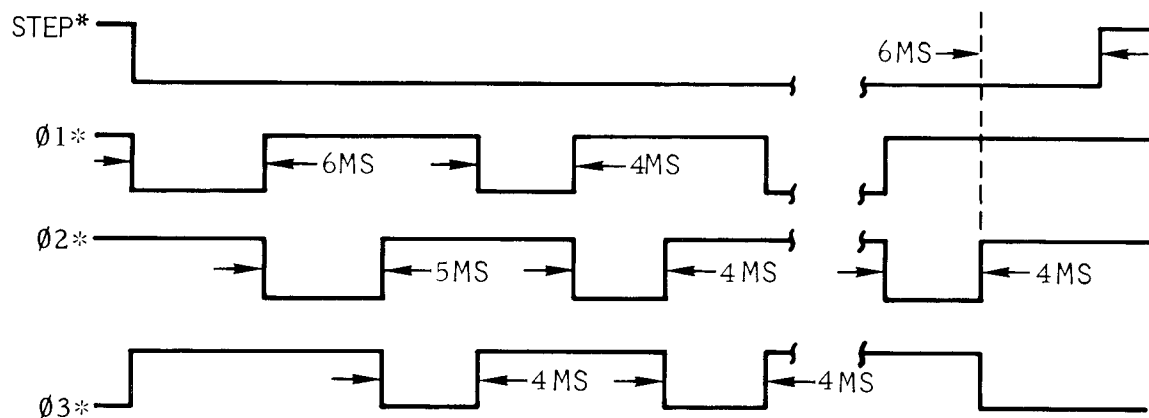
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Figure 4-34. Stepping Motor Input Waveforms (Line Step Mode)

(A) FOR 6 LINES/INCH

TOLERANCE $\pm 100 \mu\text{S}$ 

(B) FOR 8 LINES/INCH



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Figure 4-35. Stepping Motor Input Waveforms (Slew Mode)

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TABLE 4-17. WIRE DRIVER CCA I/O SIGNAL DEFINITIONS

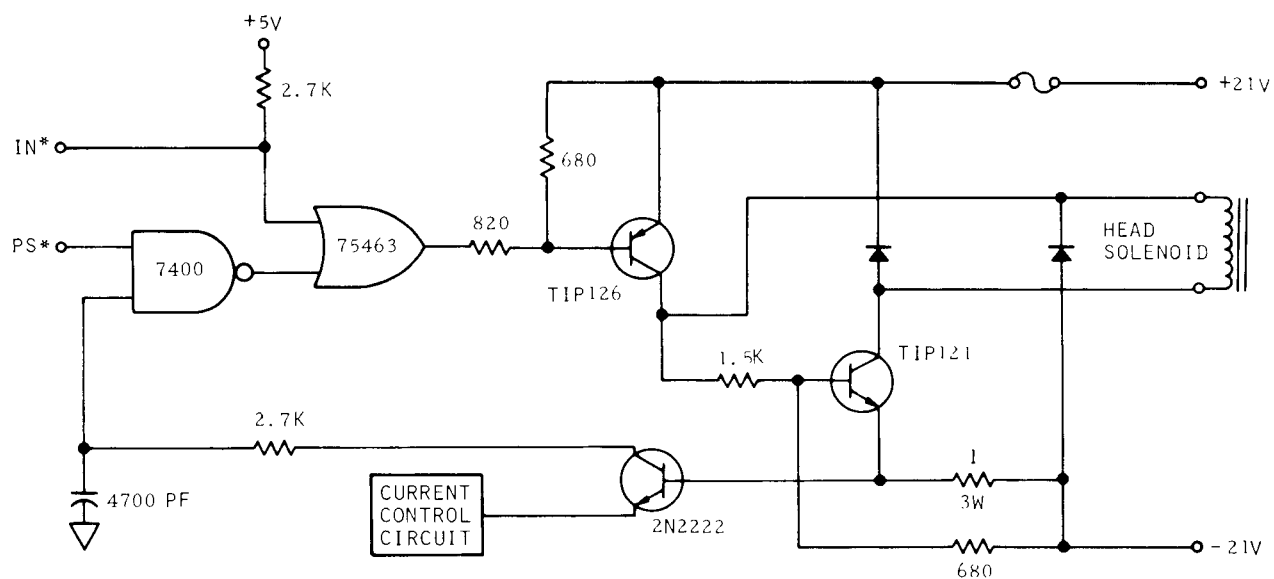
Signal	Function
PS	(Print Suppress) - A TTL high true signal from the Motor Driver CCA that inhibits any spurious signal to the input of the wire drivers from inadvertently firing the print wires during printer power up or power down.
1R* - 7R* 1L* - 7L*	Driver Input (Right/Left) - TTL low true signal from the Processor CCA that turns on the driver circuit. This signal should be low for not longer than 350 ± 10 microseconds.
1R1, 1R0, 2R1, 2R0 7R1, 7R0, 7L1, 2L1, 2L0, 1L1, 1L0	Wire driver outputs are connected to the coils in the print head -- one on the inside (1) wire of each coil winding, and one on the outside (0) wire of each coil winding. At room temperature, the coil forms a load of approximately 1.45 ohms, 3.5 mHz. Nominally, the signals relative to each other; i.e., (1L1-1L0), remain at 0V when the driver is off. The waveform across the driver outputs is similar to that shown in figure 4-36 when the coil is activated.

4.7.2 Circuit Operation (Figure 4-36 and 4-37)

Figure 4-36 shows a typical wire driver circuit. When the input signal is low, the output of OR gate (U13, U14, U17, U18, U21, U22, U24) goes low, turning on PNP transistor Q15-29. This causes current to flow through the transistor, which turns on NPN transistors Q30-Q43. The NPN transistor allows current to flow through the coil in the print head. As the current in the coil approaches a preset value, the voltage across the 1-ohm sense resistor turns on the 2N2222 transistor. The voltage at the emitter of 2N2222 (current bias) determines the peak value of the current through the head coil. As the 2N2222 transistor is turned on, it discharges the 4700 pF capacitor at the input of NAND gate 7400.

At the point that the 7400 output changes state, the output of OR gate 75463 goes high and turns off power transistors TIP126 and TIP 121. The 2N2222 transistor is immediately turned off, since no more current is flowing through the 1-ohm resistors; and then the 4700 pF capacitor begins to charge through the internal pull up resistor of NAND gate 7400. When the output of 7400 changes to the low state, the power circuit is again reactivated and begins to build up current in the coil. This "chopping" action continues as long as the input signal is low.

To inhibit the complete circuit from firing, the PS* signal on the the input of NAND gate 7400 must go low.

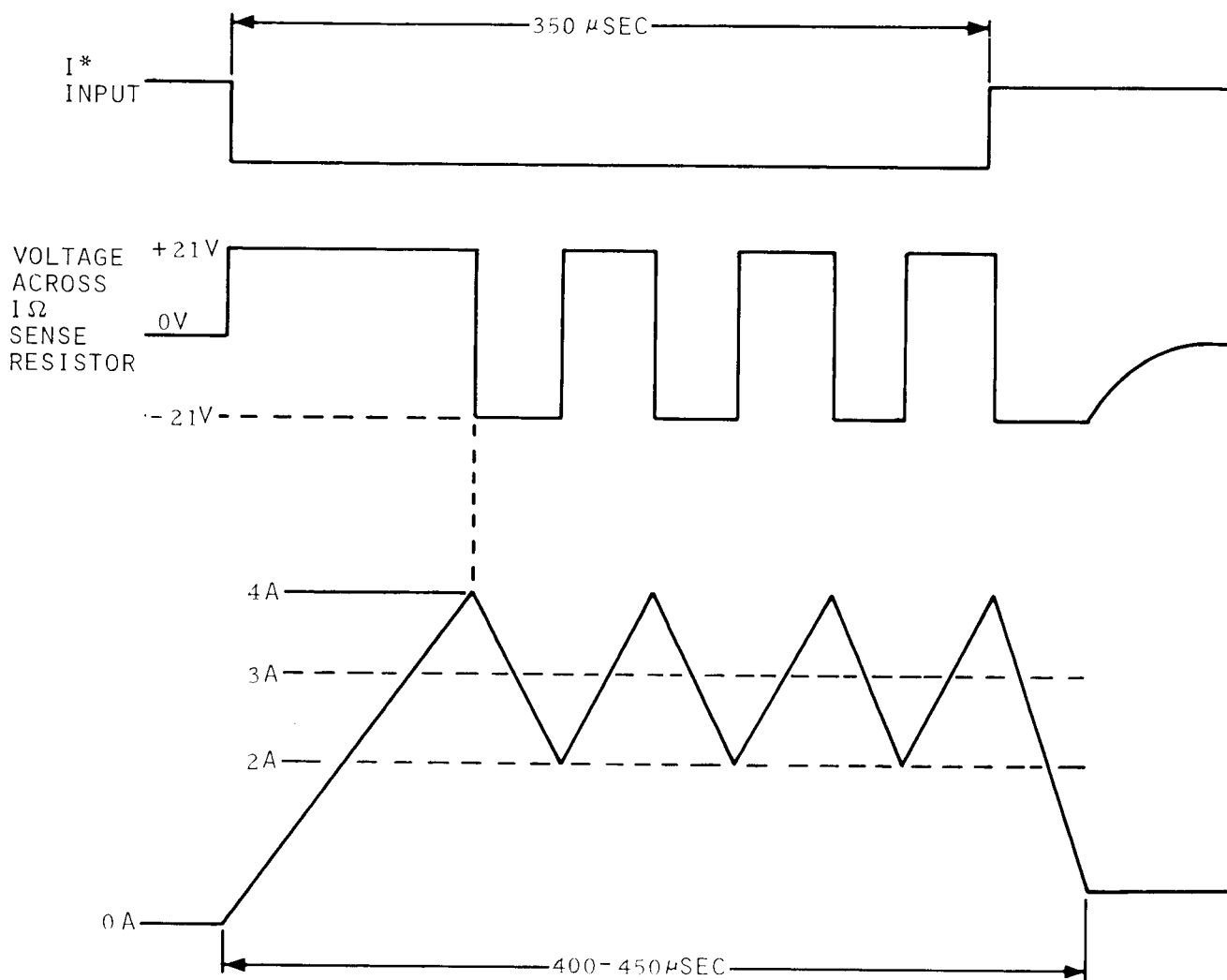


ALL RESISTOR VALUES IN OHMS

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Figure 4-36. Typical Wire Driver Circuit

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Figure 4-37. Wire Driver Current Waveform

The current control circuit (figure 4-38) controls the reference point on the emitter of every 2N2222 transistor. The 500-ohm potentiometer is used in a voltage divider circuit, dividing the 5.6V reference voltage caused by the 680-ohm resistor and the 1N5232B zener diode. The potentiometer controls the transistor base voltage, which controls the current reference voltage across the TIP126 transistor. The 10 microfarad capacitor is used to filter out any transients.

4.8 POWER SUPPLY SYSTEM

The power supply system is composed of two sections: the AC-to-filtered DC converter, and the voltage regulator. The AC-to-filtered DC converter is available in the standard and optional universal versions. The voltage regulator is common to both versions.

The power supply system is protected against high frequency line noise and switching transients by a line filter which is installed to include suppression of switching transients generated by the POWER ON switch. In the event of excess internal temperatures, a thermosensor will interrupt the AC input power until the temperature drops to its normal operating value. The thermosensor is mounted on the rectifier heat sink assembly located above the transformer.

4.8.1 Universal AC-to-Filtered DC Converter

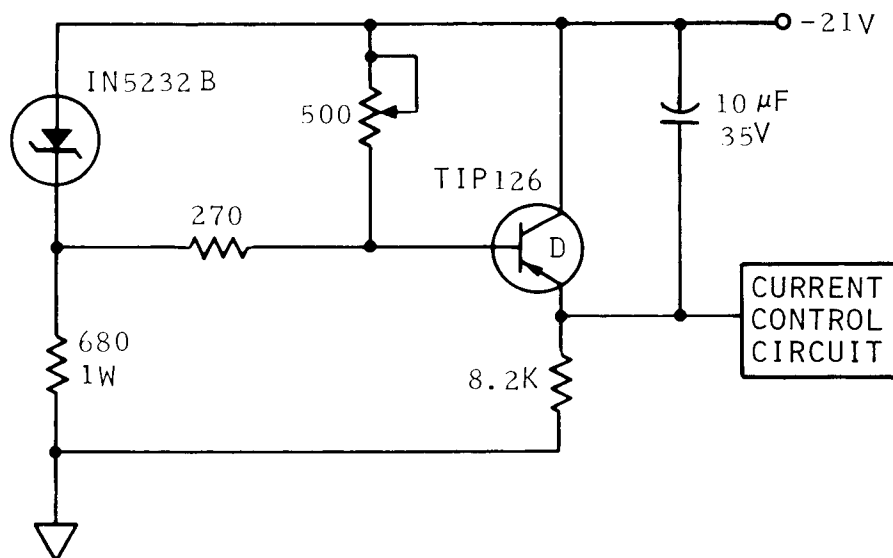
Table 4-18 lists the available input voltages and frequencies which can be programmed into the power supply by simply rearranging the wiring of the program connector TB2 (see figure 4-39). No tools are required to perform the wiring changes.

TABLE 4-18. UNIVERSAL SUPPLY INPUT VOLTAGES
AND FREQUENCIES

Nominal Input Voltage	Low Input Voltage	High Input Voltage	Input Freq. Range
115 VAC	90 VAC	127 VAC	59 to 60.6 HERTZ
250 VAC	204 VAC	264 VAC	59 to 60.6 HERTZ
115 VAC	90 VAC	140 VAC	49 to 50.5 HERTZ
250 VAC	187 VAC	264 VAC	49 to 50.5 HERTZ

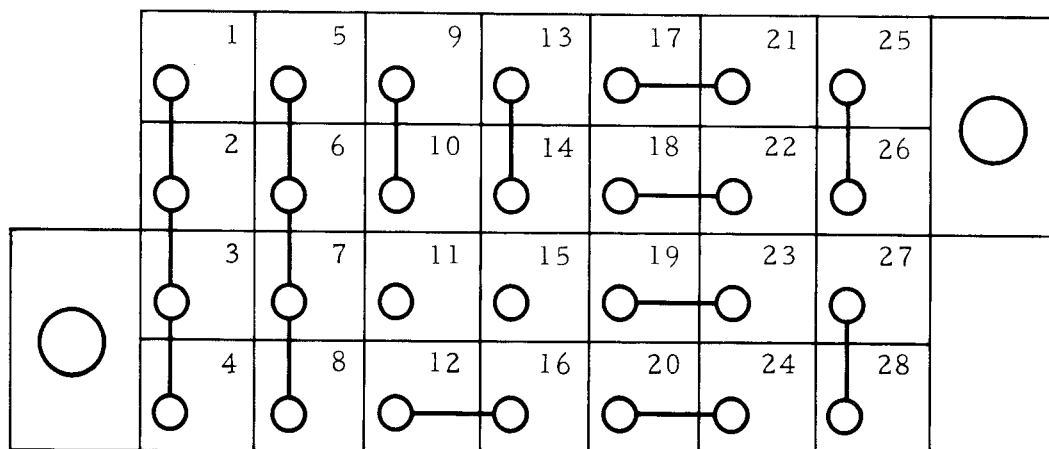
Table 4-19 is the TB2 wire configuration table listing pin position numbers, frequencies, and wire colors.

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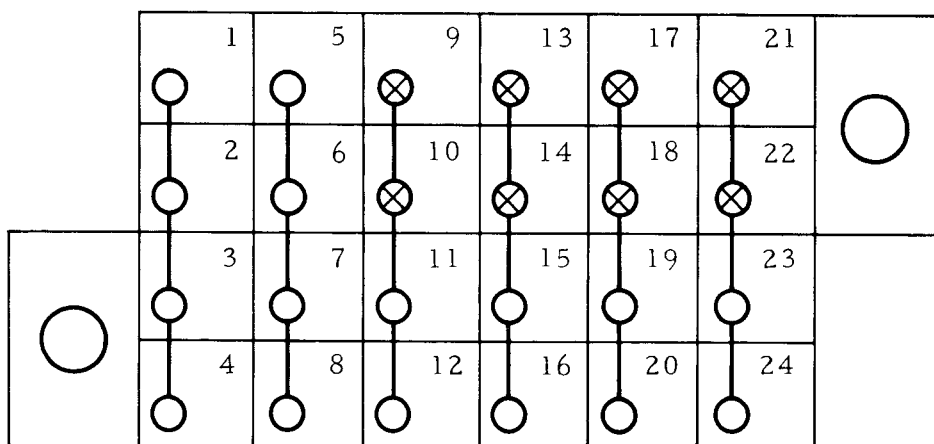
ALL RESISTOR VALUES IN OHMS

Figure 4-38. Current Control Circuit



TB2

(USED ONLY IN THE UNIVERSAL A/C TO FILTERED D/C CONVERTER)



TB1

(USED IN THE STANDARD AND THE UNIVERSAL A/C TO FILTERED D/C CONVERTER)

NOTES

1. PINS MARKED ⊗ HAVE WIRES ON BOTH SIDES.
2. TB1 IS LOCATED ON THE HEATSINK ABOVE TRANSFORMER.
3. TB1 IS LOCATED NEXT TO C4.
4. TB1 AND TB2 VIEWS SHOWN FROM FRONT OF PRINTER.

Figure 4-39. Terminal Block Pin Configuration

TABLE 4-19. TB2 WIRE CONFIGURATION

Wire Color	TB2 Pin Position Numbers			
	115V/60hZ	250V/60hZ	115/50hZ	250V/50hZ
Red	8	16	8	16
Green/Yellow	6	6	10	10
Green/White	9	9	6	6
Brown	3	7	3	7
Brown/Yellow	7	12	14	14
Brown/White	13	13	7	12
Orange/White	27	27	26	26
White	23	23	24	24
Violet/White	22	22	21	21
Red/White	Base Term.	Base Term.	C4	C4
Red/Black	C4	C4	Base Term.	Base Term
Wires Not Affected by Changes				
Black/White	4	4	4	4
Black (Fan)	5	5	5	5
Black (Fan)	1	1	1	1
Green	2	2	2	2
Yellow/Black	28	28	28	28
Yellow/White	25	25	25	25
Blue/White	20	20	20	20
Blue	19	19	19	19
Blue	18	18	18	18
Blue/White	17	17	17	17
Notes:				
1. When using the 250 VAC input voltage the F1 fuse has to be replaced with a 1.5A SLO-BLO fuse.				
2. The base terminal is a slot in the printer base shell located in front of the resonant transformer capacitor C4 located at the left rear corner of the printer chassis. It serves as a storage compartment for the red/white wire or the red wire - whichever is not being used.				

4.8.2 Standard AC-to-Filtered DC Converter

The standard version is basically the same as the universal converter described in paragraph 4.8.1, with the exception that it accommodates only one input voltage and frequency:

Nominal input voltage:	115 VAC
High input voltage:	127 VAC
Low input voltage:	90 VAC
Frequency range:	59 to 60.6 Hz

4.8.3 Output Specifications

Table 4-20 lists the output specifications for both the standard and universal AC-to-Filtered DC converters.

TABLE 4-20. OUTPUT SPECIFICATIONS

Item	Specification
<u>+21 Volts Output</u>	
Minimum:	+18.1 Volts
Nominal:	+21 Volts
Maximum:	+23.1 Volts
Ripple (Standby):	100 Millivolts P-P, $\pm 20\%$
Ripple (Selftest):	1.5 Volts P-P, $\pm 20\%$
Current (Standby):	0.5 Amps
Current (Selftest):	3.0 Amps
<u>-21 Volts Output</u>	
Minimum:	-18.9 Volts
Nominal:	-21 Volts
Maximum:	-23.1 Volts
Ripple (Standby):	200 Millivolts P-P, $\pm 20\%$
Ripple (Selftest):	1.5 Volts P-P, $\pm 20\%$
Current (Standby):	1.5 Amps
Current (Selftest):	4.0 Amps
<u>+9 Volts Output</u>	
Minimum:	+8.1 Volts
Nominal:	+9 Volts
Maximum:	+9.9 Volts

TABLE 4-20. OUTPUT SPECIFICATIONS (Contd)

Item	Specifications
Ripple (Standby):	50 Millivolts P-P, $\pm 20\%$
Ripple (Selftest):	200 Millivolts P-P, $\pm 20\%$
Current (Standby):	2.4 Amps
Current (Selftest):	2.4 Amps
<u>Input Power</u>	
Standby:	130 Watts
Self Test:	220 Watts
Power On Surge:	Approximately 1000 Volt-Amp for a period of 125 milliseconds, with an applied input voltage of 115 VAC rms.
Ambient Operating Temp.	10°C to 40°C
Thermosensor Rating	Normally closed. Opens at heat sink temperature of 75°C and closes at 55°C.

4.8.4 Voltage Regulator CCA Operation

The voltage regulator accepts the unregulated voltages from the AC-to-filtered DC converter and regulates these voltages to the required printer operating voltages. In addition to the regulation circuitry, voltage protection circuits (Crow Bar Method) are provided to protect the operating circuitry of the printer from an abnormal overvoltage condition.

The +21 volt unregulated voltage is regulated to a +12V output level by the regulator 7812KC (U3). This device is an integrated circuit regulator with internal current limiting and thermal shutdown features. No external circuit components are needed for the regulation itself, but to prevent high frequency oscillation, capacitors C10 and C9 are added. Diodes CR6 and CR4 function as a safety valve in case of a reverse voltage condition.

The crowbar circuit consists of the SCR D6, zener diode CR3, resistor R12 and capacitor C7. Whenever the output voltage exceeds the breakdown voltage of the zener diode (14 volts) the SCR will fire, short circuiting the output of the regulator. The regulator will either go into the current limiting mode or fuse F3 will open. F3 may not open, but the integrated circuit regulator will be thermally protected.

The operation of the -12 volt regulator is similar to the +12 volt regulator, except that it uses a 7912KC integrated circuit regulator (U2) and accepts the -21V unregulated voltage.

The +5 volt regulation is accomplished by using a 723 integrated circuit regulator (U1) as a voltage reference and comparator amplifier. The output of the 723 controls the base of transistor Q1 which functions as a series pass transistor. Transistor Q2 is used for current limiting. To provide a more accurate regulation, the voltage sensor is located on the mother board. The +5 volt regulator is also protected against overvoltage by a crow bar circuit with an overvoltage trip point of 6.3 volts. When the SCR fires, it will short circuit the input to the +5V regulator, and this will result in opening fuse F1.

4.8.5 Voltage Regulator Output

Table 4-21 lists the voltage regulator output.

TABLE 4-21. VOLTAGE REGULATOR OUTPUT

Parameter	Conditions	Min.	Max.
Positive 5 Volt Output	$I_L \leq 5 \text{ Amp}$	4.95	5.05
Positive 12 Volt Output	$I_L \leq 300 \text{ mA}$	11.4	12.6
Negative 12 Volt Output	$I_L \leq -300 \text{ mA}$	-11.4	-12.6
± 12 Volt Ripple	$I_L \leq \pm 300 \text{ mA}$		10×10^{-3}
Positive 5 Volt Ripple	$I_L \leq 5 \text{ Amp}$		
Positive 12 Volt Over Voltage Trip		13.5	16.5
Negative 12 Volt Over Voltage Trip		-13.5	-16.5
Positive 5 Volt Over Voltage		6.3	7.7

4.9 TCVFU CCA (Figure 9-18)

The optional TCVFU CCA controls the operation of the TCVFU motor in accordance with signals supplied to it by the Interface CCA and TCVFU tape reader. As shown in sheet 2 of figure 9-18, the TCVFU motor is connected to pins 2 and 1 of J17. Pin 2 of J17, labelled MOTOR+, is connected directly to the +9V supply. Pin 1 of J17, labelled MOTOR-, is connected to the collector junction of Q3. When Q3 is conducting, 9V RTN is connected to the collector junction of Q3. The TCVFU motor is running. When Q3 is cut off, the TCVFU motor is switched off. Normally Q3 is cut off and the TCVFU motor is not running.

Action starts when the operator presses the READ switch on the TCVFU tape reader, activating signal TRRQSW* on J1-12. An amplified version of TRRQSW*, signal TRRQ*, is routed through J16-20 to the Interface CCA and ultimately to the Processor CCA. The Processor CCA responds by activating read enable signal ENRDR*. This signal is routed through the Interface CCA to J1-15 of the TCVFU CCA, turning on Q2. With Q2 conducting, Q3 is turned on, switching on the TCVFU motor. Also, while Q2 is conducting, +5V LED SUPPLY is provided to the tape reader.

While ENRDR* is active, periodically the sprocket hole in the tape is sensed by the TCVFU reader, activating signal CH13 on J1-28 on the TCVFU CCA. With CH13 active, one-shot U1 is triggered on, momentarily turning on Q1. With Q1 conducting, Q3 is cut off, turning off the TCVFU motor. When U1 times out, the TCVFU motor is turned on once again. Thus, during the on-period of U1 (approximately 190 microseconds) the tape is stopped long enough to allow the TCVFU reader to sense the tape channel positions associated with a given sprocket hole.

SECTION V

MAINTENANCE

5.1 INTRODUCTION

This section contains information necessary to maintain the printer in good working order. Paragraph 5.2 includes removal/replacement procedures for the printer's replaceable assemblies and parts, and paragraph 5.3 contains electrical and mechanical adjustment procedures.

Figure 5-1 is a block diagram illustrating the sequence in which the various parts and assemblies must be removed for maintenance.

All procedures outlined in this section must be performed by qualified personnel only, using equipment capable of giving reliable and accurate measurements. Personnel performing any of these procedures must be familiar with the printer operation as well as with the mechanical configuration of the printer.

5.2 RECOMMENDED HAND TOOLS AND EQUIPMENT

The following hand tools and equipment are required to maintain the printer:

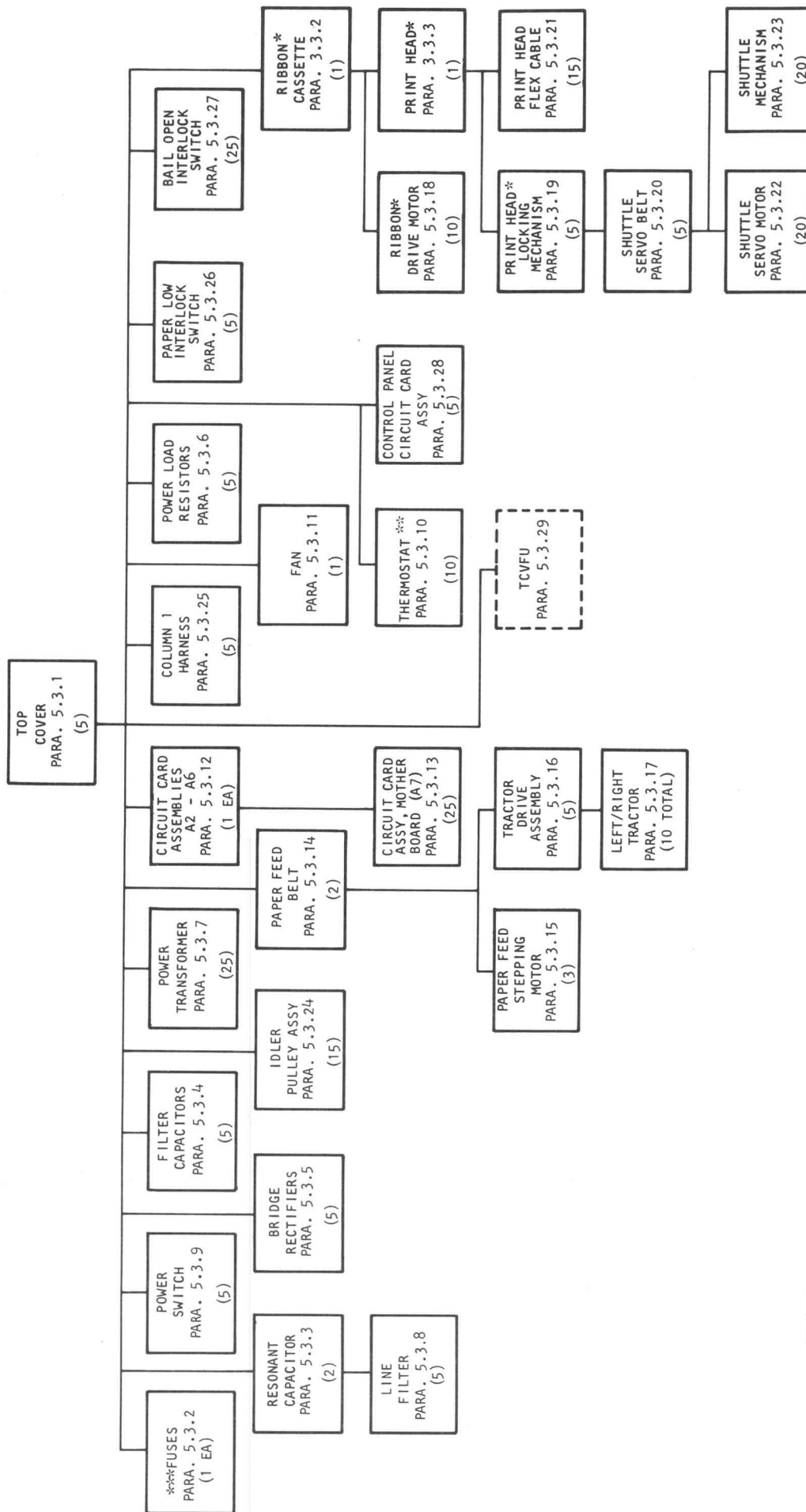
- a. Screwdriver, 1/4-inch blade, 8-1/8 inches long, Xcelite R144 or equivalent.
- b. Screwdriver, 3/16-inch blade, 7-5/8 inches long, Xcelite R3164 or equivalent.
- c. Screwdriver, 3/16-inch blade, 13-5/8 inches long, Xcelite R31610 or equivalent.
- d. Screwdriver, Phillips, 1/3-inch diameter, 4-1/4 inches long, Xcelite P12 or equivalent.
- e. Screwdriver, Phillips, 3/16 inch diameter, 6-5/8 inches long, Xcelite X101 or equivalent.
- f. Screwdriver, Phillips, 1/4-inch diameter, 8-1/8 inches long, Xcelite X102 or equivalent.
- g. Screwdriver, offset, 1/4-inch/5/16-inch blades.
- h. Hexdriver, 2mm Allen.
- i. Hexdriver, 2.5mm Allen.
- j. Nutdriver, 4mm, Xcelite No. 99-4 or equivalent.
- k. Nutdriver, 4.5mm, Xcelite No. 99-4.5 or equivalent.
- l. Nutdriver, 5mm, Xcelite No. 99-5 or equivalent.
- m. Nutdriver, 6mm, Excelite No. 99-6 or equivalent.
- n. Nutdriver, 7mm, Xcelite No. 99-7 or equivalent.
- o. Nutdriver, 8mm, Excelite No. 99-8 or equivalent.
- p. Needle-nose Pliers, No. 14-4.
- q. Slip-joint Plier, No. 11-6. r. Cutting Plier, 84 EHM EREM or
- r. Cutting Plier, 84 EHM EREM or equivalent.
- s. Tweezer, No. 226.

- t. Metric Scale, 300mm.
- u. Feeler Stock, 0.05mm.
- v. Feeler Stock, 0.4mm.
- w. Feeler Stock, 1.00mm (2 required).
- x. Soldering Iron.
- y. Desoldering Tool, Soldapullt Deluxe DS017.
- z. Dynamometer, ARPO (Jensen Catalog No. 110B090) or equivalent.
- aa. Oscilloscope, Tektronics 535 (or equivalent).
- bb. Digital Multimeter HP Model No. 3476A or equivalent.

5.3 REMOVAL/REPLACEMENT PROCEDURES

The following paragraphs contain removal/replacement procedures for the printer assemblies and parts shown in figure 5-1 and listed below:

Top Cover	(Paragraph 5.3.1)
Fuse	(Paragraph 5.3.2)
Resonant Capacitor	(Paragraph 5.3.3)
Filter Capacitor	(Paragraph 5.3.4)
Bridge Rectifier	(Paragraph 5.3.5)
Power Load Resistor	(Paragraph 5.3.6)
Power Transformer	(Paragraph 5.3.7)
Line Filter	(Paragraph 5.3.8)
Power Switch	(Paragraph 5.3.9)
Thermostat	(Paragraph 5.3.10)
Fan	(Paragraph 5.3.11)
Circuit Card Assembly	(Paragraph 5.3.12)
Mother Board	(Paragraph 5.3.13)
Paper Feed Belt	(Paragraph 5.3.14)
Paper Feed Step Motor	(Paragraph 5.3.15)
Tractor Drive Assembly	(Paragraph 5.3.16)
Left/Right Tractor	(Paragraph 5.3.17)
Ribbon Drive Motor	(Paragraph 5.3.18)
Print Head Locking Mechanism	(Paragraph 5.3.19)
Shuttle Servo Belt	(Paragraph 5.3.20)
Print Head Flex Cable	(Paragraph 5.3.21)
Shuttle Servo Motor	(Paragraph 5.3.22)
Shuttle Mechanism	(Paragraph 5.3.23)
Idler Pulley Assembly	(Paragraph 5.3.24)
Column 1 Harness	(Paragraph 5.3.25)
Paper Low Interlock Switch	(Paragraph 5.3.26)
Bail Open Interlock Switch	(Paragraph 5.3.27)
Control Panel Circuit Board Assembly	(Paragraph 5.3.28)
TCVFU (Option)	(Paragraph 5.3.29)



NOTES:

1. BROKEN LINES INDICATE OPTIONS.
2. *CAN BE REMOVED WITHOUT REMOVING THE TOP COVER.
3. **REQUIRES REMOVAL OF LINE FILTER MOUNTING PLATE AND POWER SWITCH HOUSING COVER.
4. NUMBERS IN PARENTHESES REPRESENT AVERAGE TIME, IN MINUTES, REQUIRED TO REMOVE AND REPLACE ITEM.
5. ***INPUT POWER FUSE ACCESSIBLE WITHOUT REMOVING TOP COVER.

Figure 5-1. Printer Assembly/
Port Removal Sequence

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MAINTENANCE

5.3.1 Top Cover Removal/Replacement (Figure 5-2)

Top cover removal replacement may be a prerequisite for all subsequent removal, replacement, and adjustment procedures. Note that the top cover is fastened to the base by two recessed screws at the front and by two quick-release latches at the rear. In addition, the top cover houses the control panel, which is fastened by a spring-loaded clip and must be detached for top cover removal. The removal procedure is as follows:

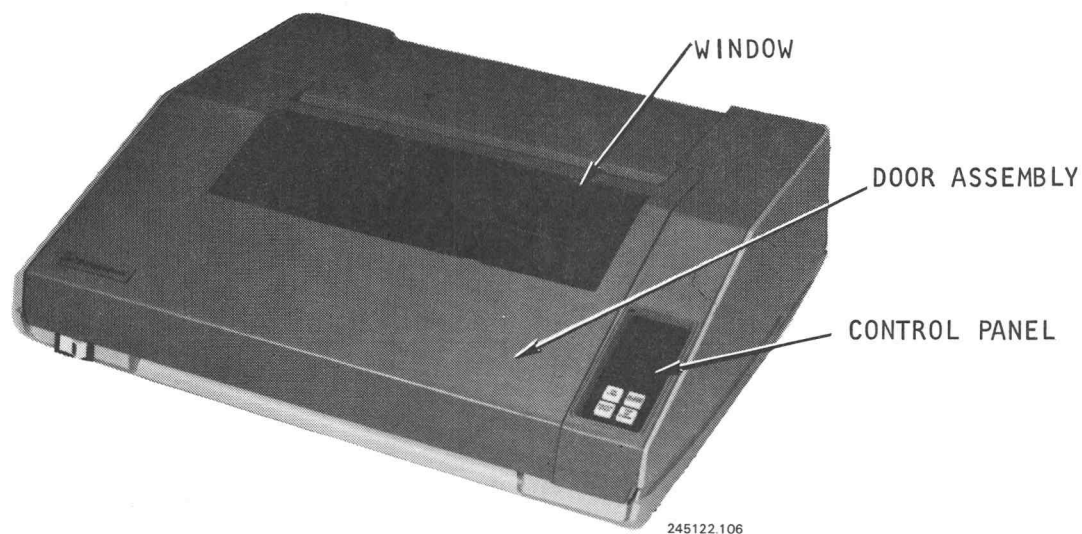


Figure 5-2A. Top Cover Removal/Replacement
Door Assembly Closed.

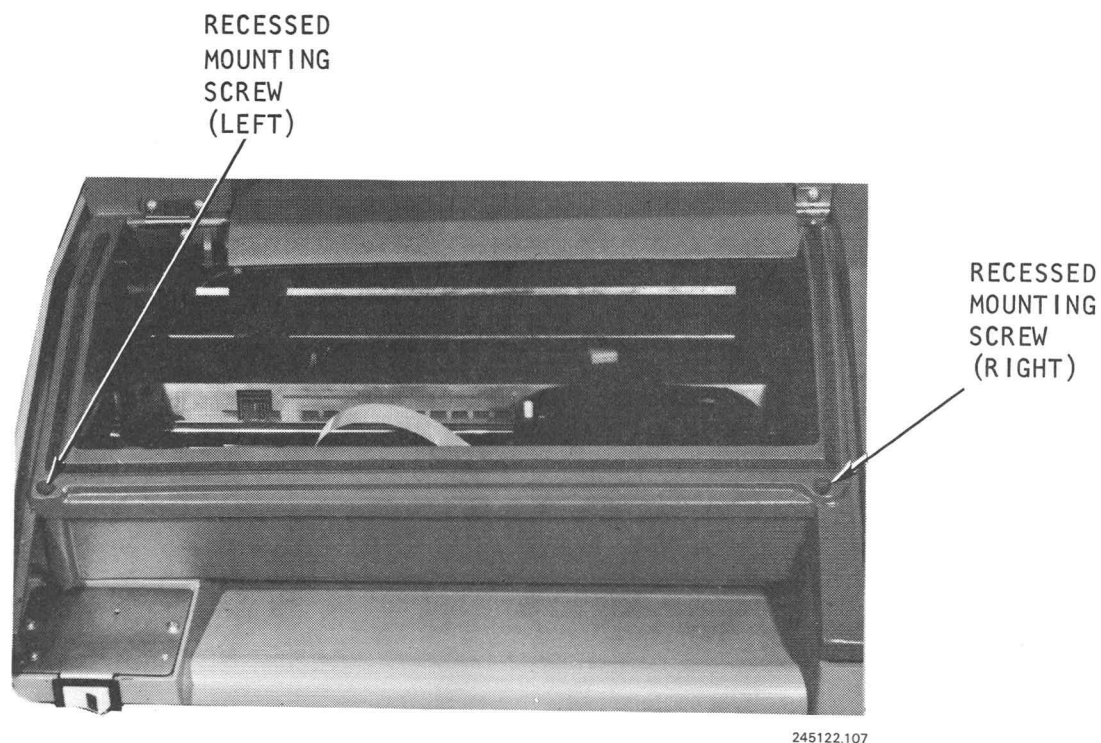


Figure 5-2B. Top Cover Removal/Replacement
Door Assembly Raised.

- a. Disconnect the power plug from the power source.

WARNING

Do not attempt to perform any removal/replacement or specified adjustment procedures with the power plug connected to the power source.

- b. Raise the door assembly to gain access to the two screws securing the top cover at the front.

- c. Loosen and remove the left and right recessed mounting screws at the front of the printer.

CAUTION

When performing step d, be careful not to apply any tension to the control panel harness.

- d. Unlatch the two quick-release latches at the rear and set the cover on its right side.

- e. While maintaining pressure on the retaining clip with one hand, grasp the control panel with the other hand (see figure 5-2C) and pull down. The top cover is now free to be removed.

- f. Set the top cover on a convenient flat surface.

- g. Place the control panel within the housing on the right side of the printer base assembly so that the two holes on the control panel circuit card assembly fit over the two molded pins.

- h. To replace, raise the front of the top cover and install the control panel inside the top cover. To do so, orient the control panel so that the cable harness is on the outside, and the pushbutton switches are at the top. Insert the top end of the control panel within the top cover opening with the edge of the control panel resting on the flange. Finally, press the bottom end of the control panel against the spring tension of the retaining clip and snap in place.

- i. Slowly lower the top cover of the printer. Make sure that the control panel harness is not pinched between the top cover and the printer base.

- j. Align the top cover at the front and rear, fasten the two quick release latches at the rear, and secure the two retaining screws at the front.

- k. Close the door assembly.

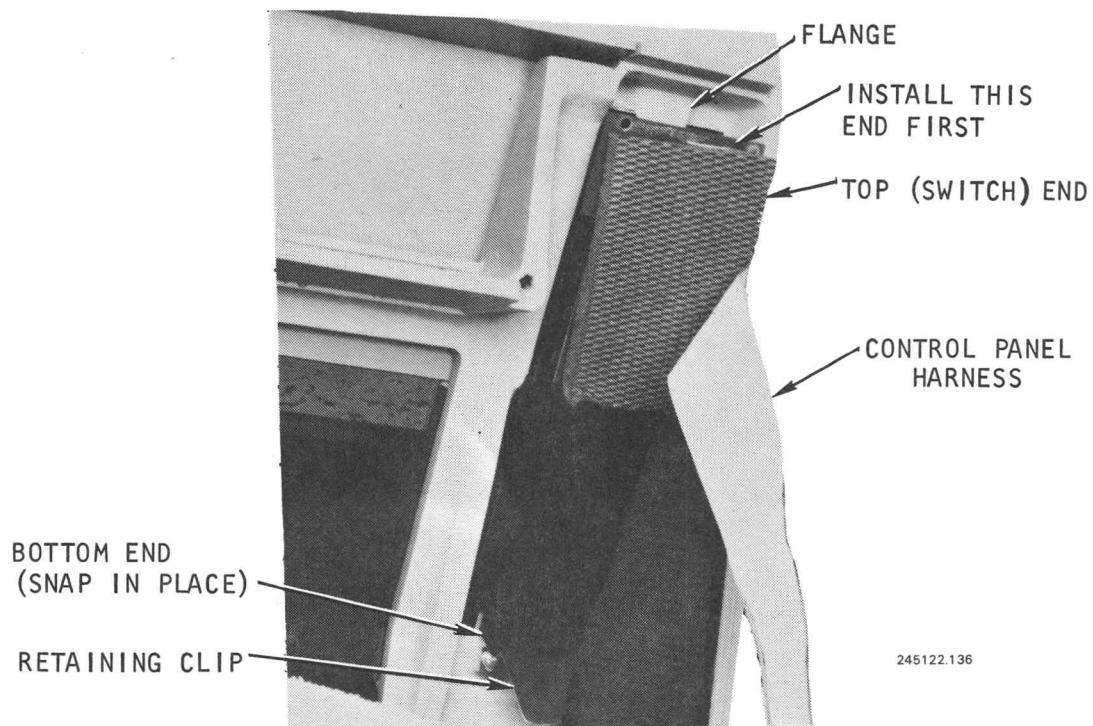


Figure 5-2C. Top Cover Removal/Replacement Control Panel Mounting Details (Viewed From Inside of Top Cover).

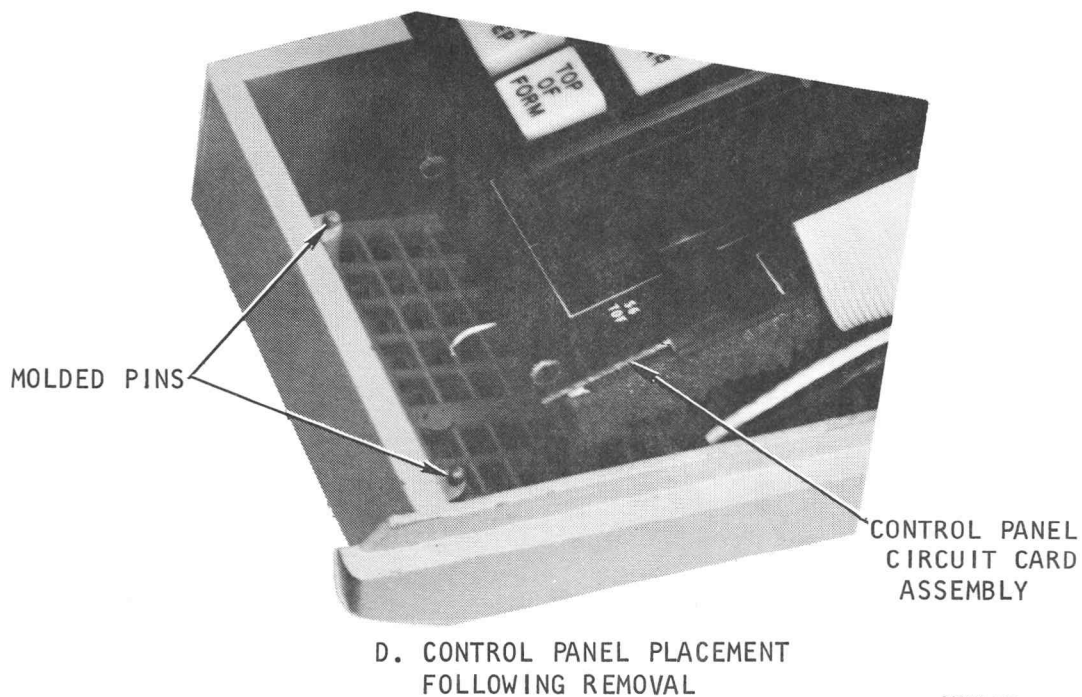


Figure 5-2D. Top Cover Removal/Replacement Control Panel Placement Following Removal

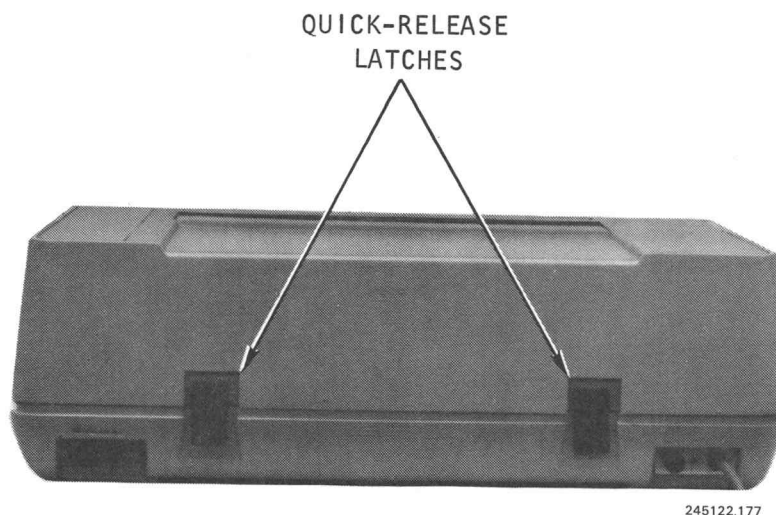


Figure 5-2E. Top Cover Removal/Replacement Rear View.

5.3.2 Fuse Removal/Replacement

The printer has a total of 16 bus-type fuses mounted in spring-loaded clips. When the top cover is removed, these fuses are accessible from the top of the printer. Another fuse, the main power fuse, is mounted at the rear of the printer near the line cord, and can be accessed without removing the top cover.

WARNING

Do not attempt to replace fuses with the power on.

5.3.3 Resonant Capacitor Removal/Replacement (Figure 5-3)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING)
- b. Remove the capacitor from its spring-loaded clamp.
- c. Remove the insulating hood to gain access to the capacitor terminal.
- d. Disconnect the push-on terminals and remove the capacitor.
- e. Reverse the procedure of steps a through d and replace the resonant capacitor.
- f. Replace the top cover per paragraph 5.3.1.

5.3.4 Filter Capacitor Removal/Replacement (Figure 5-3)

Filter capacitors C1, C2, and C3 are secured by a supporting bracket anchored at each end by a screw. Proceed as follows:

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Remove the two screws and supporting bracket.
- c. Disconnect the leads from both terminals by removing the terminal screws.
- d. Remove the capacitor.
- e. Orient the capacitor so that the positive terminal faces the rear of printer; then insert it into its mounting place.
- f. Replace the leads on the capacitor terminals and secure them with the two terminal screws.

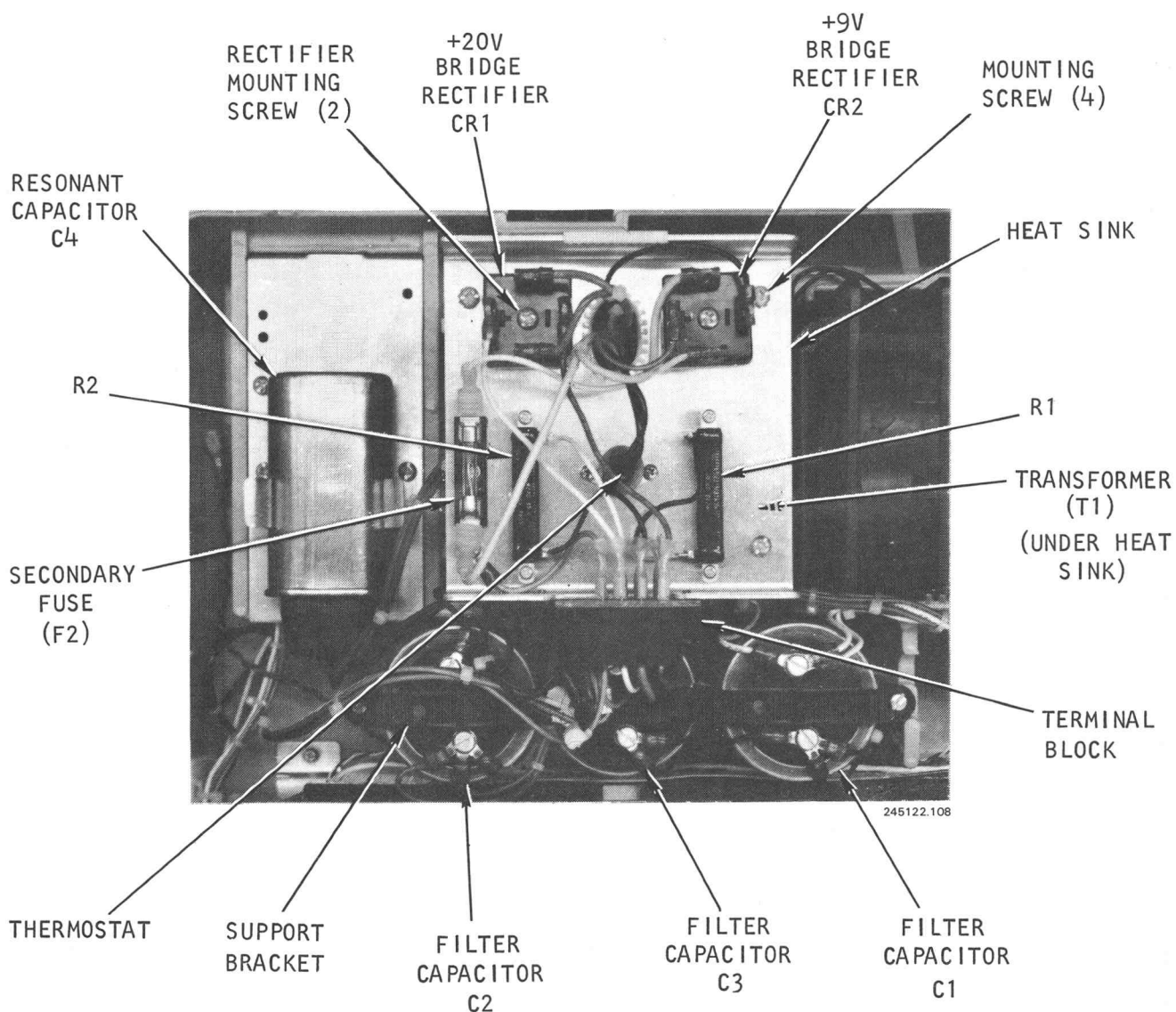


Figure 5-3. Power Supply Parts Removal/Replacement

- g. Place the supporting bracket over the three filter capacitors and secure them with the two terminal screws.

NOTE

When performing step g above, exercise caution not to pinch the leads.

- h. Replace the top cover per paragraph 5.3.1.

5.3.5 Bridge Rectifier Removal/Replacement (Figure 5-3)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Remove the four push-on connectors from bridge rectifier CR1 or CR2, where applicable, one connector at a time. Identify each lead with a tag, and note the +/- physical placement of the bridge rectifier.
- c. Remove the screw that secures the bridge rectifier to the heat sink, and remove the bridge rectifier.
- d. Orient the replacement bridge rectifier as noted in step b, then mount it to the heat sink.
- e. Connect the push-on connectors to the rectifier, one connector at a time. Use the identifying tag to match the lead with the terminal, and remove the tag after connection is made.

- f. Replace the top cover per paragraph 5.3.1.

5.3.6 Power Load Resistor Removal/Replacement (Figure 5-3)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Disconnect and tag the two R1 and R2 resistor leads.
- c. Remove the two mounting screws.
- d. When replacing the resistors, ensure that the resistor terminals are facing inward and that the stand-offs are installed between the resistors and heat sink (shown in figure 5-3).

- e. Replace the top cover per paragraph 5.3.1.

5.3.7 Power Transformer Removal/Replacement (Figure 5-3)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Remove the four screws that secure the heat sink to the four standoffs.

c. Remove the two blue push-on terminals that connect the transformer to the bridge rectifier, one terminal at a time. Identify each terminal with a tag.

d. Remove the two yellow push-on terminals, one from fuse F2 and one from the other bridge rectifier.

e. Slide the disconnected transformer leads through the feed hole in the heat sink; position the heat sink away from the top of the transformer.

f. Remove the two black leads from terminals 2 and 6 of the terminal block TB-1.

g. Remove the leads that connect the transformer to the resonant capacitor.

h. Using an 8mm wrench, remove the four standoffs and washers. Then remove the transformer.

CAUTION

Do not overtighten the four stand-offs that secure the transformer in place. Also, be sure that no wires are pinched between the standoffs and the heat sink.

i. Replace the power transformer by reversing steps a through h.

j. Replace the top cover per paragraph 5.3.1.

NOTE

One of four screws that mount the heat sink secures a ground lead. When replacing the heat sink, be sure that the ground lead eyelet is in place.

5.3.8 Line Filter Removal/Replacement (Figure 5-4)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

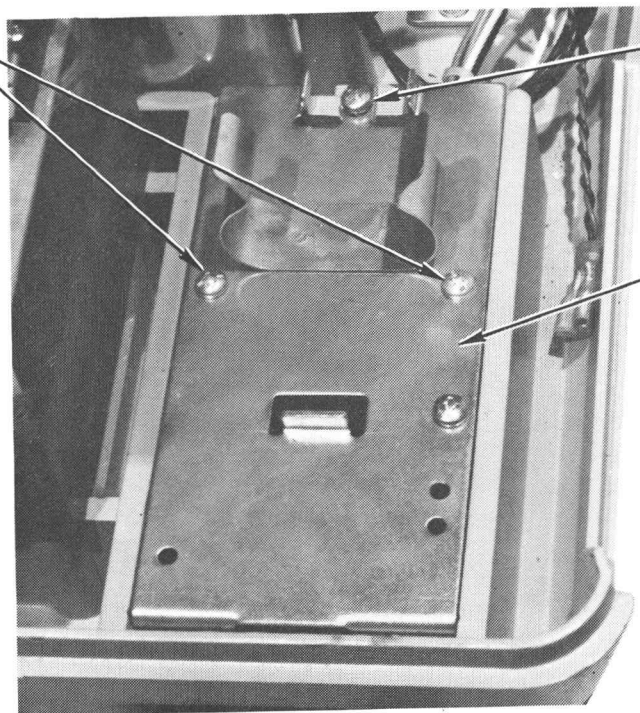
b. Remove resonant capacitor C4 from the bracket (see figure 5-3).

c. Remove the screw that secures the mounting plate to the printer housing casting (see figure 5-4), and turn the assembly over to gain access to the line filter.

d. Remove the line filter mounting screws and remove the filter.

e. Remove the four leads from the filter, one at a time, and tag each lead.

LINE
FILTER
MOUNTING
SCREWS



LINE FILTER
MOUNTING PLATE
SECURING SCREW

LINE
FILTER
MOUNTING
PLATE

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Figure 5-4. Line Filter Removal/Replacement

- f. Connect the four leads to the new line filter terminals as identified in step e.
- g. Mount the new line filter to the mounting plate.
- h. Turn the assembly (line filter and mounting plate) over and mount to the printer casting.
- i. Replace the top cover per paragraph 5.3.1.

CAUTION

Ensure that no leads are pinched between the mounting plate and printer housing.

5.3.9 Power Switch Removal/Replacement (Figure 5-5)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Remove the two screws and associated hardware that secure the power switch S1 housing cover, and remove the cover.
- c. Move the four switch leads, one lead at a time. Identify each lead with a tag.
- d. Remove the switch and replace with the new switch.
- e. Reconnect the four leads identified in step c.

CAUTION

Ensure that no wires are pinched between the cover and the printer housing.

- f. Replace the switch housing cover and secure with the two screws removed in step b.
- g. Replace the top cover per paragraph 5.3.1.

5.3.10 Thermostat Removal/Replacement

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Refer to paragraph 5.3.8 and remove the line filter mounting plate.
- c. Rotate the mounting plate so that the line filter is facing upward, and remove the thermostat push-on connector lead from terminal 1 of the line filter.
- d. Refer to paragraph 5.3.9 and remove the power switch housing cover.

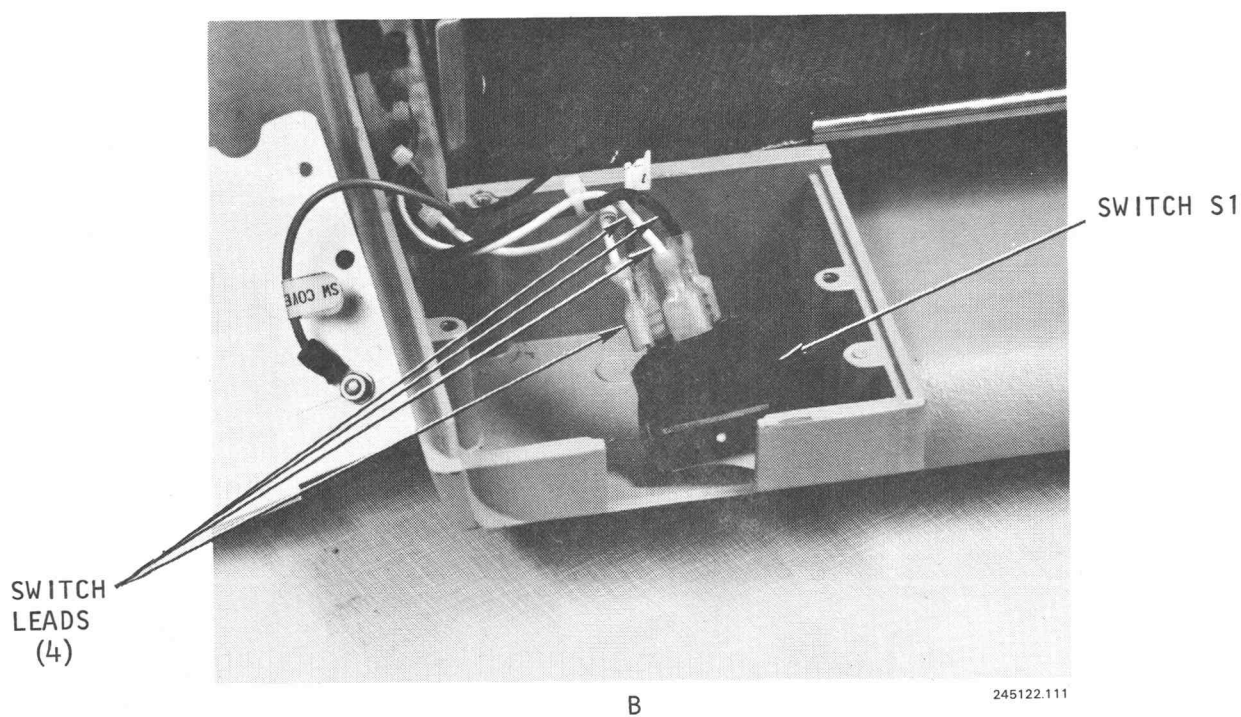
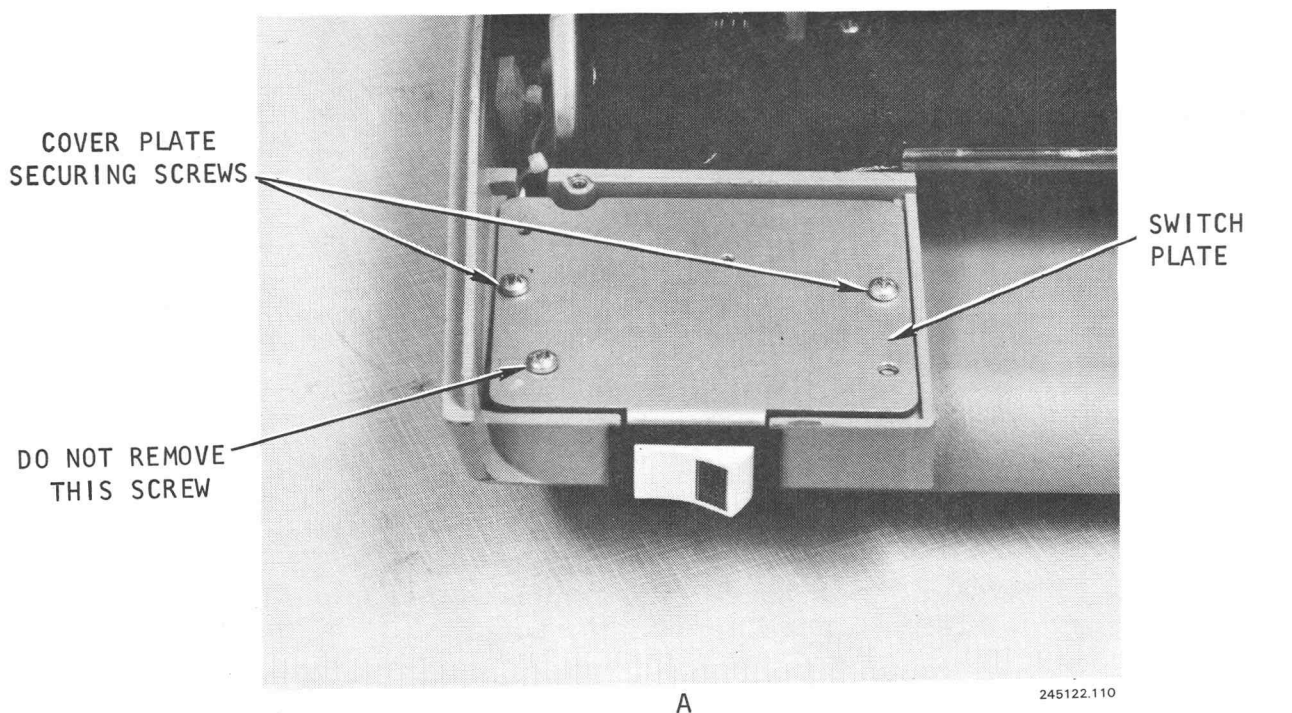


Figure 5-5. Power Switch Removal/Replacement

e. Disconnect the other thermostat push-on connector lead from main power switch S1.

f. Refer to figure 5-3 and remove the two screws that secure the thermostat to the heat sink; and remove the thermostat.

g. Install the thermostat in reverse order of the removal procedure given above.

h. Replace the top cover per paragraph 5.3.1.

5.3.11 Fan Removal/Replacement

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Disconnect the two power leads from terminal block pins 3 and 7.

c. Remove the fan.

d. Replace by connecting the power leads of the new fan to the terminal block pins 3 and 7, and insert the fan into the slot.

NOTE

The fan should be positioned so that air is blown toward the CCAs

e. Replace the top cover per paragraph 5.3.1.

5.3.12 Circuit Card Assembly Removal/Replacement

Circuit Card Assemblies A2 through A6 plug vertically into dual sockets within the mother board. Removal and replacement is as follows:

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Unplug the applicable CCA from its dual mating socket and insert the replacement board into the dual socket just vacated.

c. Test the performance of the CCA (A3 through A6 only) and adjust, if necessary, per paragraphs 5.4.1 through 5.4.4.

d. Replace the top cover per paragraph 5.3.1.

NOTE

If the Interface CCA (A2) is the optional Serial or DPC Centronics-Compatible, then the protocol switch settings are configured correctly before installing. A matrix of switch settings is given in section VI of this manual.

5.3.13 Mother Board (A7) Removal/Replacement (Figure 5-6)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Disconnect the interface cable.
- c. Remove the Interface CCA, Processor CCA, Motor Driver CCA, Wire Driver CCA, and Regulator CCA in that order.
- d. Disconnect the remaining interconnection cables from the mother board. Identify each cable with a tag.
- e. Remove paper feed stepping motor per paragraph 5.3.15.
- f. Remove the two screws and associated hardware that secure the mother board at the front.
- g. Lift and slide the mother board toward the front and out of the printer.
- h. Place the new mother board within the printer as shown in figure 5-6, and secure with the two screws removed in step f.
- i. Replace the paper feed stepping motor removed in step e.
- j. Connect the interface cable to the mother board.
- k. Reconnect the cables disconnected in step d.
- l. Replace the circuit card assemblies removed in step c in reverse order.
- m. Replace the top cover per paragraph 5.3.1.

5.3.14 Paper Feed Belt Removal/Replacement (Figure 5-7A)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Loosen, but do not remove, the three mounting screws of the paper feed stepping motor.
- c. Slide the motor forward within its slotted mounting holes as required, until the belt is slack.
- d. Slip the belt off the tractor pulley first, and then off the motor pulley.
- e. Slip the replacement belt over the motor pulley first, then over the tractor pulley.
- f. Slide the paper feed stepping motor within its slotted mounting holes until the belt is taut without binding. Tighten one of the three motor mounting screws.

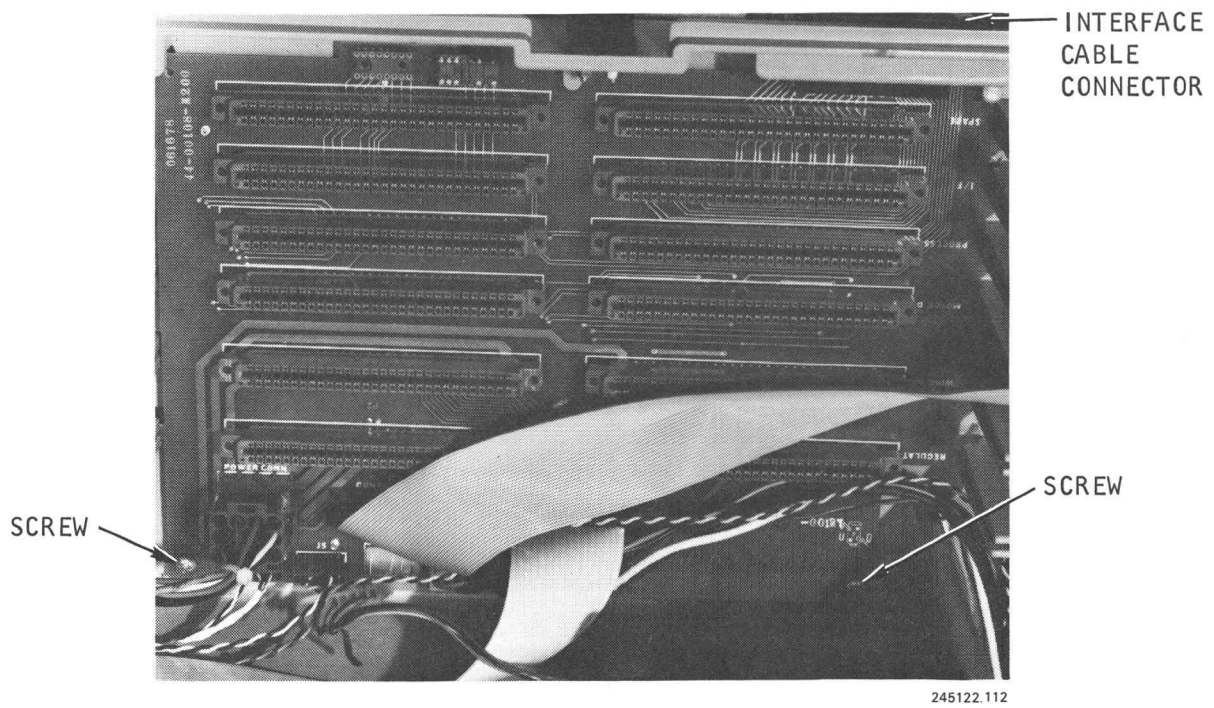
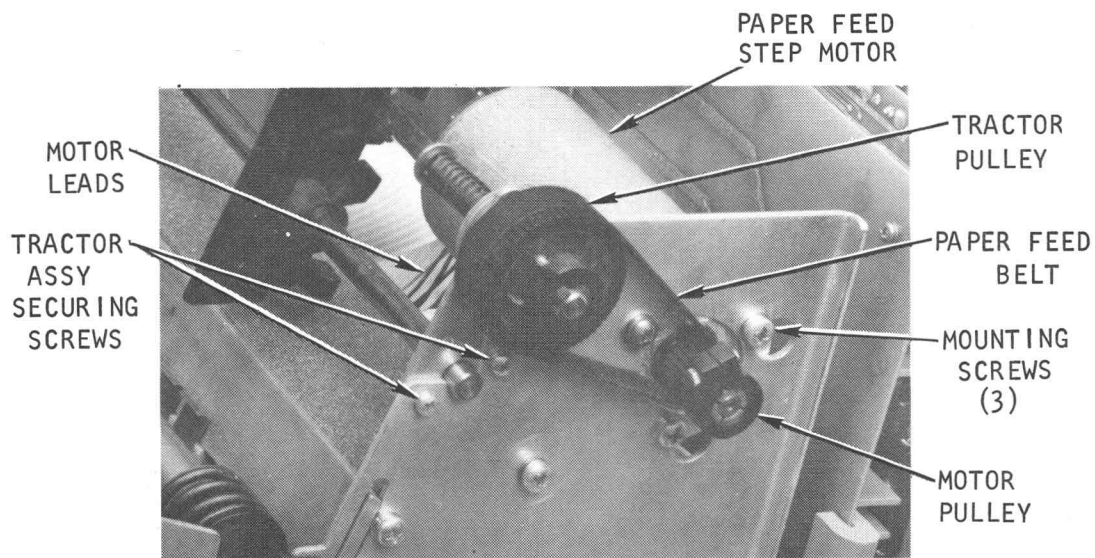
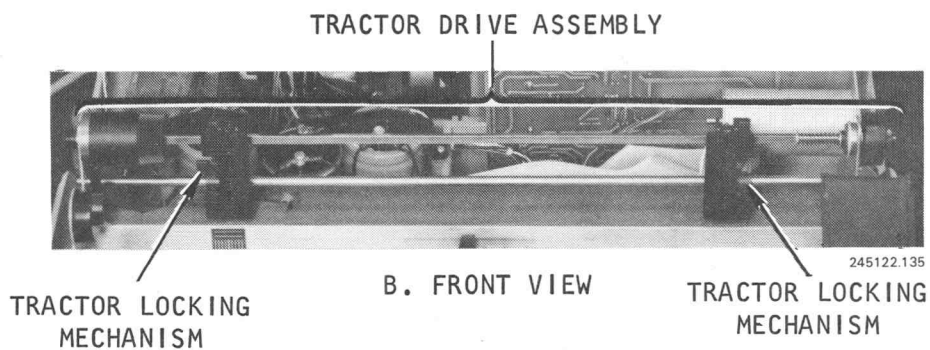


Figure 5-6. Mother Board Removal/Replacement



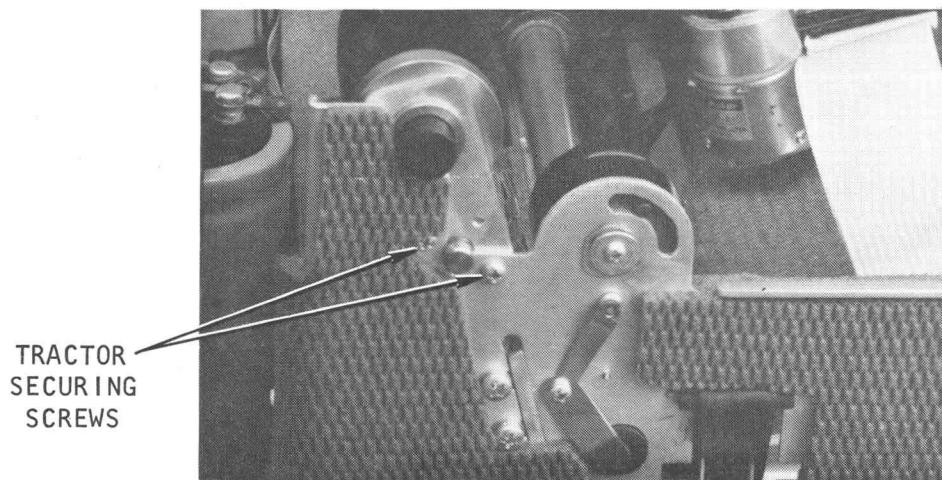
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A. RIGHT SIDE VIEW



245122.135

B. FRONT VIEW



245122.113

Figure 5-7. Paper Feed Tractor Assembly Removal/Replacement

g. Tighten the other two motor mounting screws.

h. Replace the top cover per paragraph 5.3.1.

5.3.15 Paper Feed Stepping Motor Removal/Replacement
(Figure 5-7A)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the paper feed belt per paragraph 5.3.14.

c. Disconnect the leads of the paper feed stepping motor from J6 of the mother board.

d. Remove the three mounting screws and remove the paper feed stepping motor.

e. To replace, align the three mounting holes of the paper feed stepping motor with the three slotted holes on the printer mounting brackets.

f. Replace, but do not tighten, the three mounting screws.

g. Place the paper feed belt over the motor pulley first, then over the tractor pulley.

h. Slide the motor within its slotted holes as required until the belt is taut without binding. Tighten one of the three mounting screws.

i. Tighten the other two mounting screws.

j. Connect the cable plug of the motor to J6 of the mother board.

k. Replace the top cover per paragraph 5.3.1.

5.3.16 Tractor Drive Assembly Removal/Replacement (Figure 5-7)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the paper feed belt per paragraph 5.3.14.

c. Remove the two screws at each end of the tractor drive assembly that secure the assembly to the printer mechanism frame, and remove the tractor drive assembly.

d. To replace, position the new tractor drive assembly into the printer and secure with two screws at each end.

e. Replace the paper feed belt per paragraph 5.3.14.

f. Adjust the paper feed belt, if required, per paragraph 5.4.8.

g. Replace the top cover per paragraph 5.3.1.

5.3.17 Left/Right Tractor Removal/Replacement (Figure 5-8)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Remove the paper feed belt per paragraph 5.3.14.
- c. Remove the tractor drive assembly per paragraph 5.3.16.
- d. Remove the left shaft support, vertical adjust assembly, and square tractor drive shaft (see figure 5-8).

CAUTION

The vertical adjust assembly includes several parts.
Exercise caution when removing to avoid losing parts.

- e. Release the tractor locking mechanism (see figure 5-7B) by pulling it forward, and slide the tractor from the spline bar to remove.

- f. To replace, ensure that the tractor locking mechanism is in the released (forward) position and slide the tractor onto the spline bar and lock. The locking mechanism should face the outside.

NOTE

There are two white alignment dots, one on each tractor. Ensure that the two alignment dots are directly opposite each other when installing the tractor. The notch on the spline bar should be at the left side.

- g. Install the spring, cylinder, yoke, collar, and shaft support onto the square drive shaft, shown in figure 5-8.

- h. Install the tractor drive assembly so that the side plates mate with the inside surface of the frame on both ends. The notch on the left end of the spline bar mates with the left side frame.

- i. Align the holes in the side plates with the holes in the frame and install two phillips head screws on each end.

- j. Replace the paper feed belt per paragraph 5.3.14.

- k. Replace the top cover per paragraph 5.3.1.

5.3.18 Ribbon Drive Motor Removal/Replacement (Figure 5-9)

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Remove the ribbon cassette per paragraph 3.3.2.
- c. Remove the print head per paragraph 3.3.3.

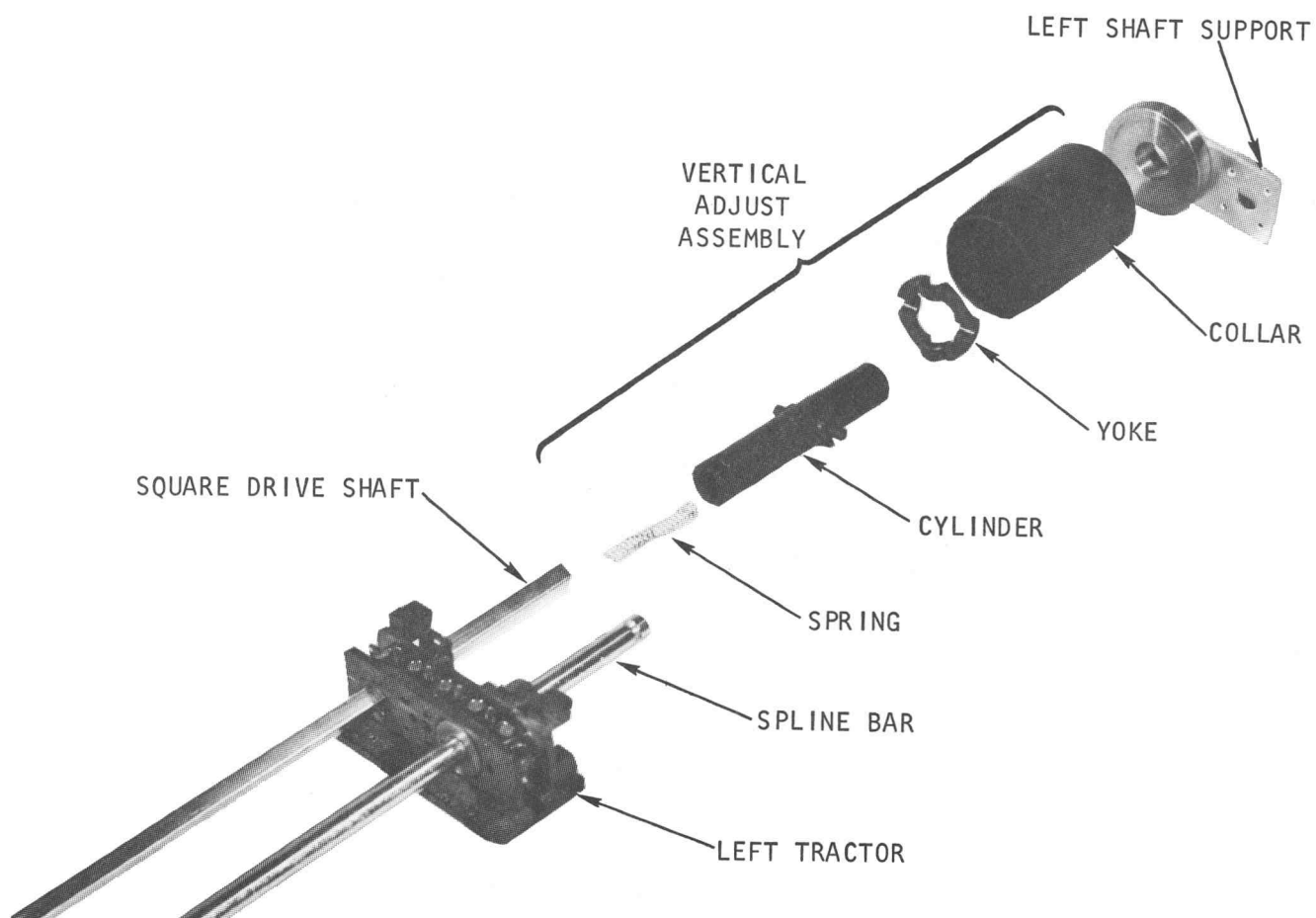


Figure 5-8. Left/Right Tractor Removal/Replacement

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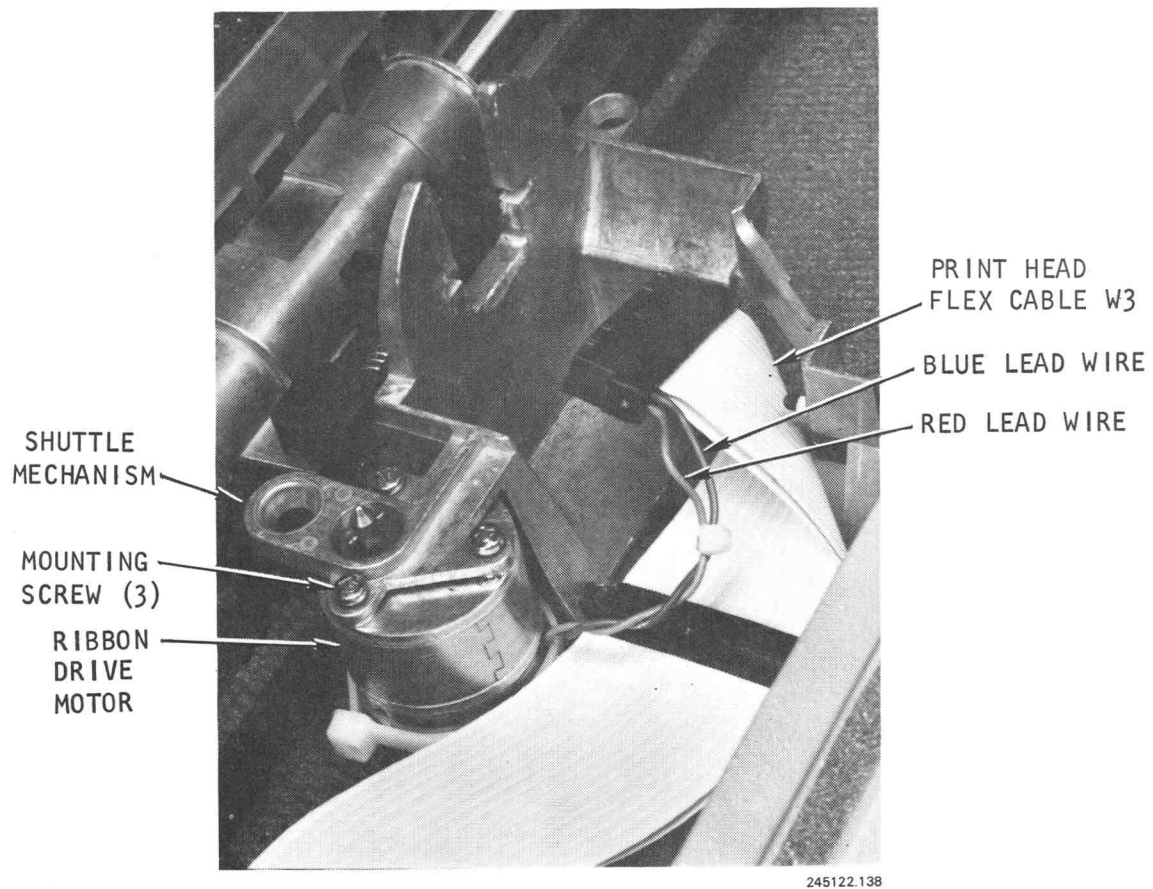


Figure 5-9. Ribbon Drive Motor Removal/Replacement

d. Disconnect the print head flex cable from the print head per paragraph 5.3.21.

e. Remove the two ribbon motor leads (blue and red) from pins 18 and 36 of the print head ribbon cable.

f. Remove the three screws that mount the ribbon motor to the shuttle mechanism, and remove the ribbon motor.

g. To replace, align the three ribbon motor mounting holes with the three mounting holes on the shuttle mechanism so that the blue and red motor leads are to the right and adjacent to the print head flex cable.

h. Mount the ribbon drive motor to the shuttle mechanism with three screws.

i. Mount the blue ribbon motor lead in pin 18 (top) of the print head ribbon cable, and the red lead in pin 38 (bottom).

j. Reconnect the print head flex cable per paragraph 5.3.21.

k. Replace the print head per paragraph 3.3.3.

l. Replace the ribbon cassette per paragraph 3.3.2.

m. Replace the top cover per paragraph 5.3.1.

5.3.19 Print Head Locking Mechanism Removal/Replacement (Figure 5-10)

The print head locking mechanism is removed or replaced under two conditions: when replacing a defective locking mechanism, or to gain access to the shuttle servo belt.

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the ribbon cassette per paragraph 3.3.2.

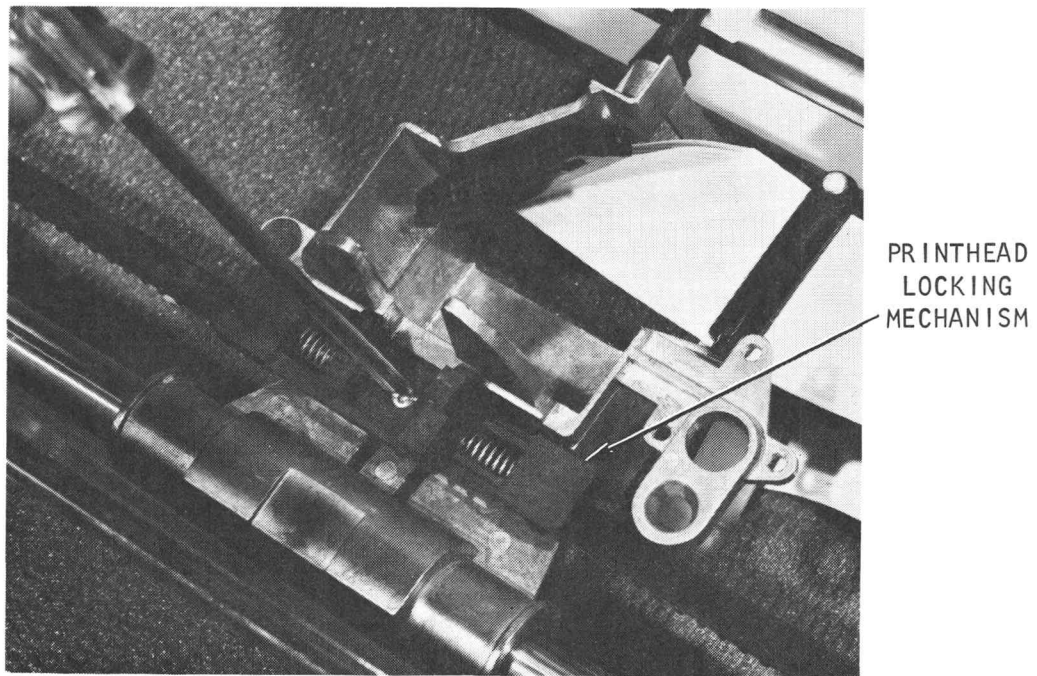
c. Remove the print head per paragraph 3.3.3.

d. Loosen the screw that mounts the locking mechanism until it is free of the printer frame.

e. To replace, insert the screw within the mounting hole of the locking mechanism, and mount the mechanism to the printer frame. The mounting screw should be tightened so that it does not inhibit free motion of the actuating arms. While operating the actuating arms, tighten the mounting screw until a slight binding is felt in the movement of the actuating arms, then back off screw a 1/4 turn.

NOTE

The guide pin next to the screw should fit into the hole in the shuttle frame.



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Figure 5-10. Print Head Locking Mechanism Removal/Replacement

- f. Replace the print head per paragraph 3.3.3.
- g. Replace the ribbon cassette per paragraph 3.3.2.
- h. Replace the top cover per paragraph 5.3.1.

5.3.20 Shuttle Servo Belt Removal/Replacement (Figure 5-11)

- a. Remove the top cover per paragraph 5.2.1 (note WARNING).
- b. Remove the ribbon cassette per paragraph 3.3.2.
- c. Remove the print head per paragraph 3.3.3.
- d. Remove the print head locking mechanism per paragraph 5.3.19.
- e. Loosen the shuttle servobelt by turning the tension adjustment knob (see figure 5-15) counterclockwise until the belt is slack.
- f. Referring to figure 5-11, slide each open end of the belt toward the rear of the printer and into its respective wide slot on the shuttle drive control assembly. This will disengage the belt from the shuttle drive control assembly.
- g. Slip each open end of the belt out of its respective wide slot, then unthread and remove the belt.
- h. To replace, thread the replacement belt under and over each pulley.
- i. Insert one segment of the right end of the belt into the wide slot (see figure 5-11), then push it into the narrow slot toward the front of the printer. This will anchor the right end of the belt to the shuttle drive control assembly. Ensure that the belt is properly seated.
- j. Seat the shuttle drive idler pulley within the recess in the frame casting per figure 5-15.
- k. With one hand, maintain tension on the left side of the belt so that the idler pulley remains seated within the recess.
- l. With the other hand, place one segment of the open end of the belt within the wide slot, then anchor the belt by sliding that segment within the narrow slot per figure 5-11.
- m. Tighten the belt with the adjustment knob by turning the tension adjustment knob clockwise until it touches the shoulder (see figure 5-15).
- n. Replace the print head locking mechanism per paragraph 5.3.19.
- o. Replace the ribbon cassette per paragraph 3.3.2.

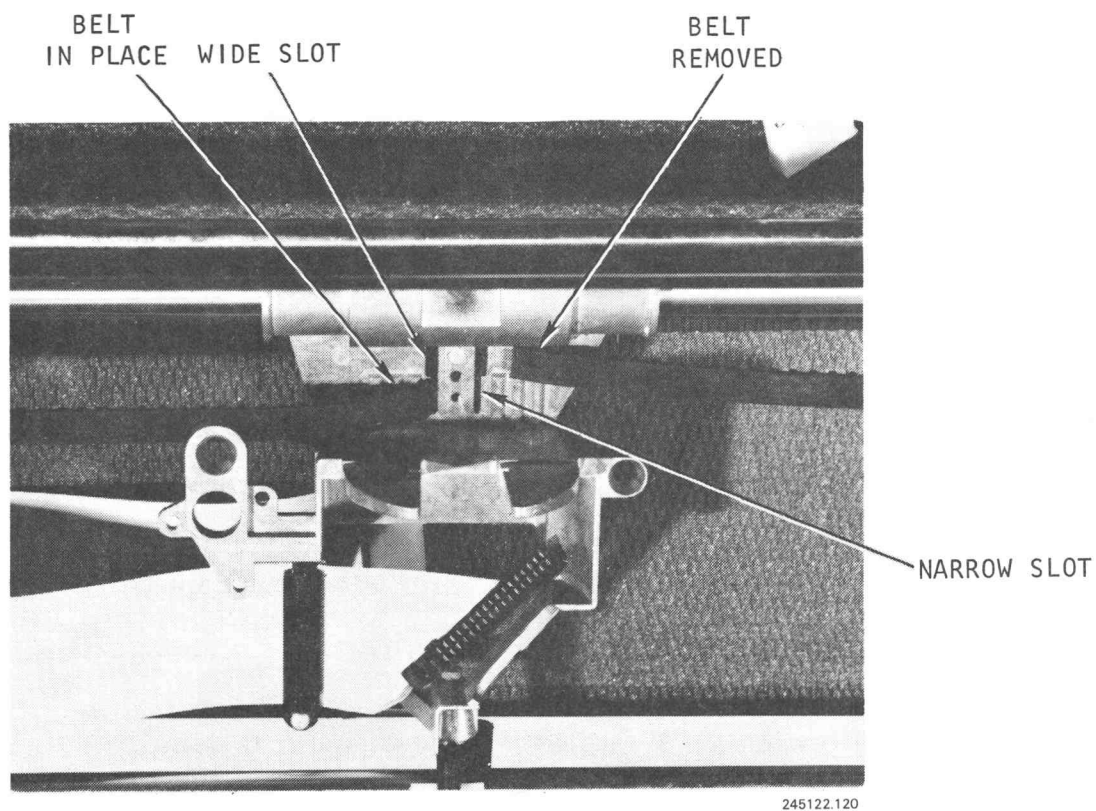


Figure 5-11. Shuttle Servo Belt Removal/Replacement

p. Replace the print head per paragraph 3.3.3.

q. Replace the top cover per paragraph 5.3.1.

5.3.21 Print Head Flex Cable Removal/Replacement (Figure 5-12)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the ribbon cassette per paragraph 3.3.2.

c. Remove the print head per paragraph 3.3.3.

d. Remove the two ribbon motor leads from the print head flex cable connector (blue lead connected to pin 18 and red lead connected to pin 38).

e. Disconnect the end of print head flex cable W3 from the mother board J3 connector.

f. Remove the shuttle servo belt per paragraph 5.3.20.

g. Remove the screw from the W3 cable clamp, and remove the clamp (see figure 5-14).

h. Remove the W3 cable from the snap cable mounted midway on the paper chute.

i. Carefully remove the W3 cable from the printer by sliding it out from between the capacitors and printer housing, and feed it out from underneath the left side of the platen bar.

j. To replace, perform steps d through i in reverse order.

k. Replace the print head per paragraph 3.3.3.

l. Replace the ribbon cassette per paragraph 3.3.2.

m. Replace the top cover per paragraph 5.3.1.

5.3.22 Shuttle Servo Motor (Shuttle Drive Control Assembly) Removal/Replacement (Figure 5-13)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the ribbon cassette per paragraph 3.3.2.

c. Remove the print head per paragraph 3.3.3.

d. Remove the shuttle servo belt per paragraph 5.3.20.

e. Disconnect the encoder cable connector from J9 of the mother board. Note the position of J9.

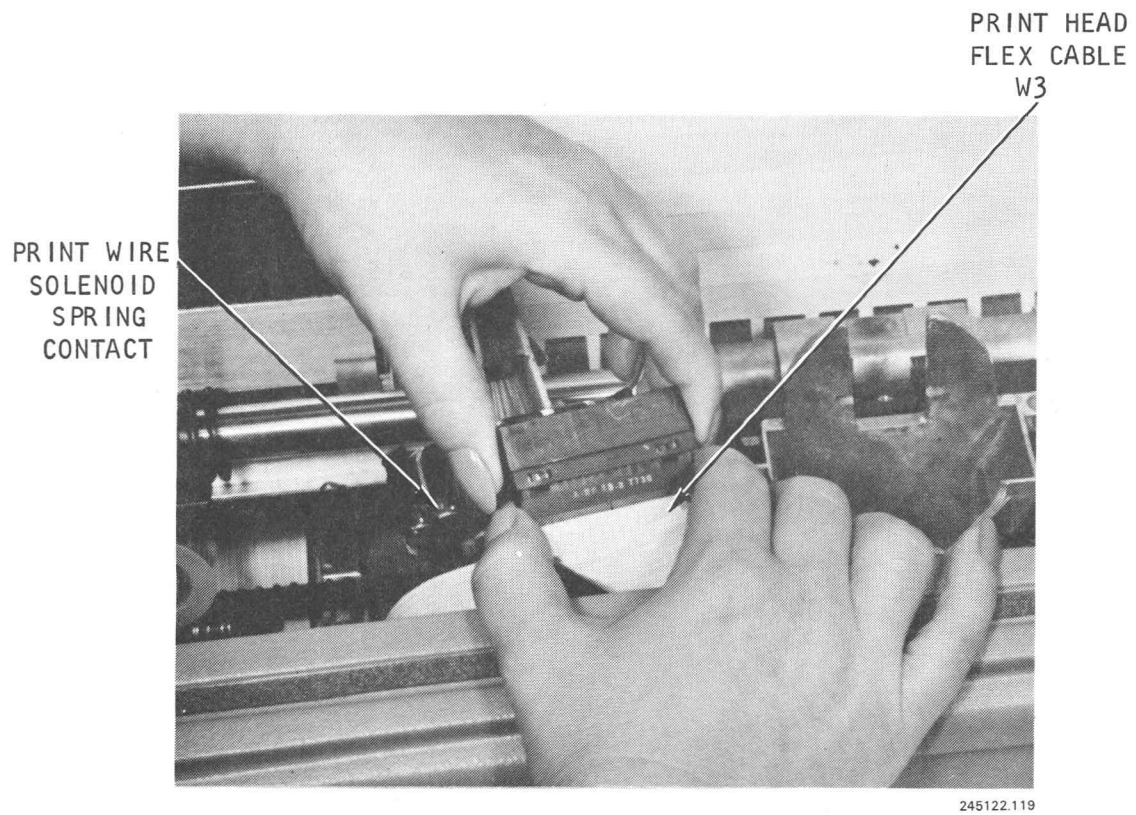


Figure 5-12. Print Head Flex Cable Removal/Replacement

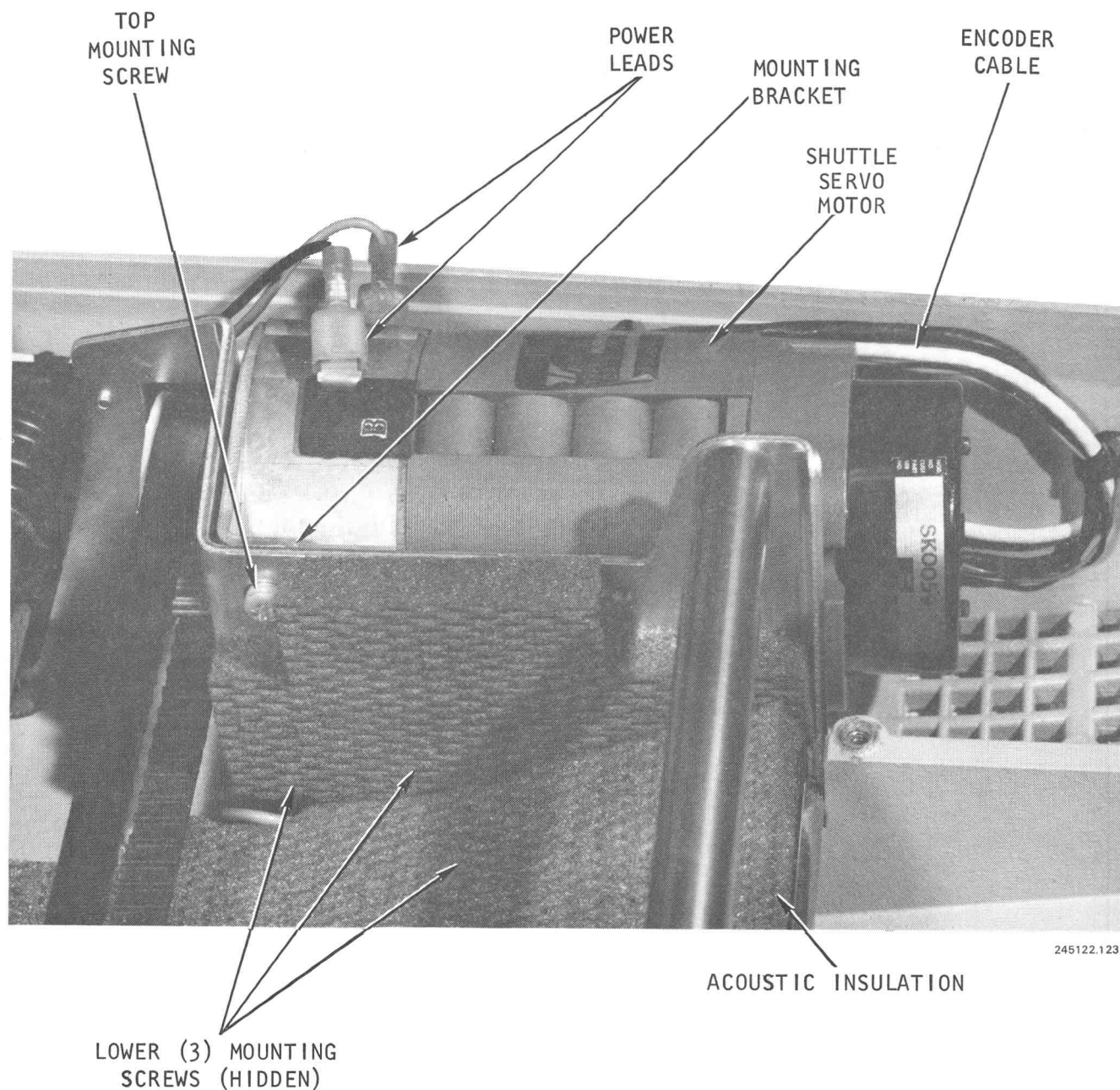


Figure 5-13. Shuttle Servo Motor (Shuttle Drive Control Assembly) Removal/Replacement

f. Remove the red and black power leads from the shuttle servo motor.

g. Remove the four screws and associated hardware (one on top, three at the bottom) that secure the shuttle servo motor to its mounting bracket, and remove the shuttle servo motor.

NOTE

To gain access to the bottom screws, it is necessary to lift the acoustic insulation padding at the right corner as well as the paper chute.

h. To replace, align the mounting holes in the shuttle servo motor bracket with the mounting holes in the mounting bracket on the printer.

i. Replace, but do not tighten, the top mounting screw, washer, and lockwasher.

j. Lift the acoustic insulation padding and the paper chute at the right corner of the printer, then replace the bottom three mounting screws with washers and lockwashers, one at a time.

k. Tighten all four mounting screws.

l. Insert the cable plug of the shuttle drive control assembly into connector J9 of the mother board, as noted in step e.

m. Connect the red and black power leads to the shuttle servo motor.

n. Replace the shuttle servo belt per paragraph 5.3.20.

o. Replace the print head per paragraph 3.3.3.

p. Replace the ribbon cassette per paragraph 3.3.2.

q. Replace the top cover per paragraph 5.3.1.

5.3.23 Shuttle Mechanism Removal/Replacement (Figure 5-14)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

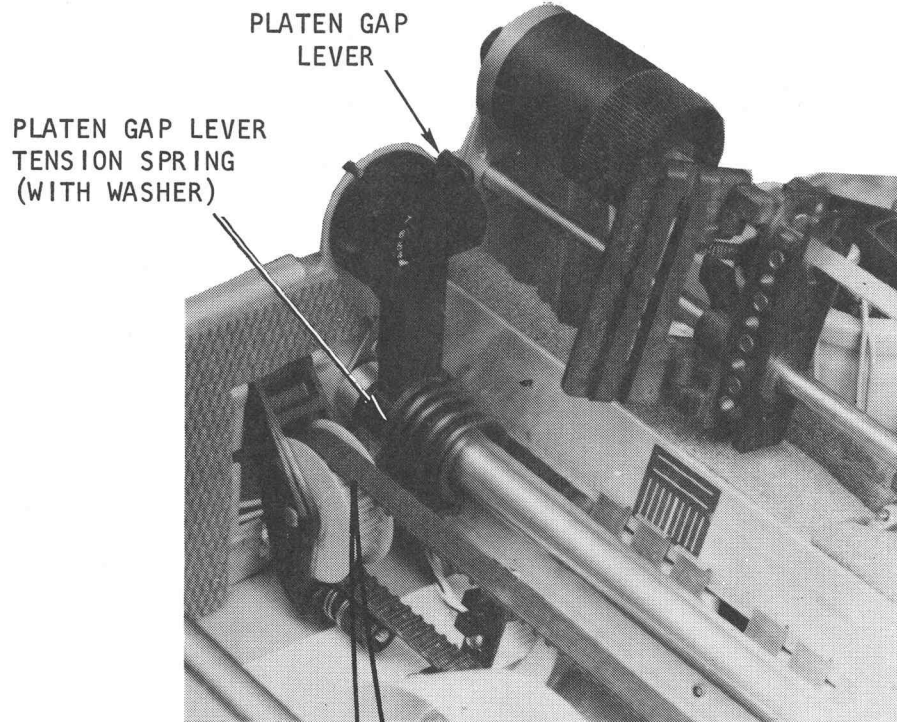
b. Remove the ribbon cassette per paragraph 3.3.2.

c. Remove the print head per paragraph 3.3.3.

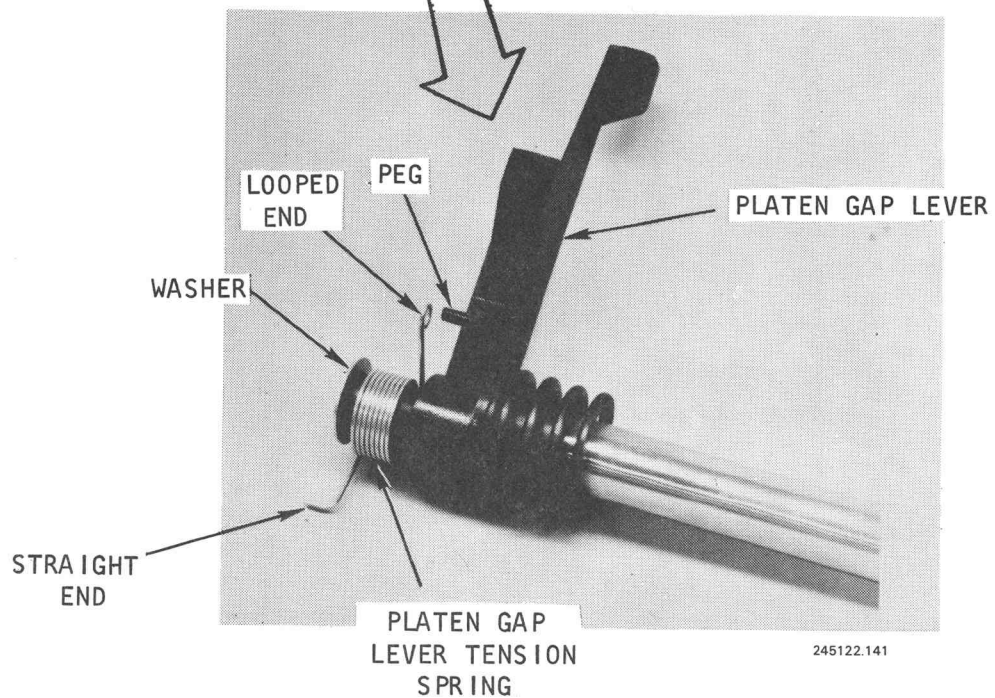
d. Disconnect the print head flex cable per paragraph 5.3.21.

e. Remove the print head locking mechanism per paragraph 5.3.19.

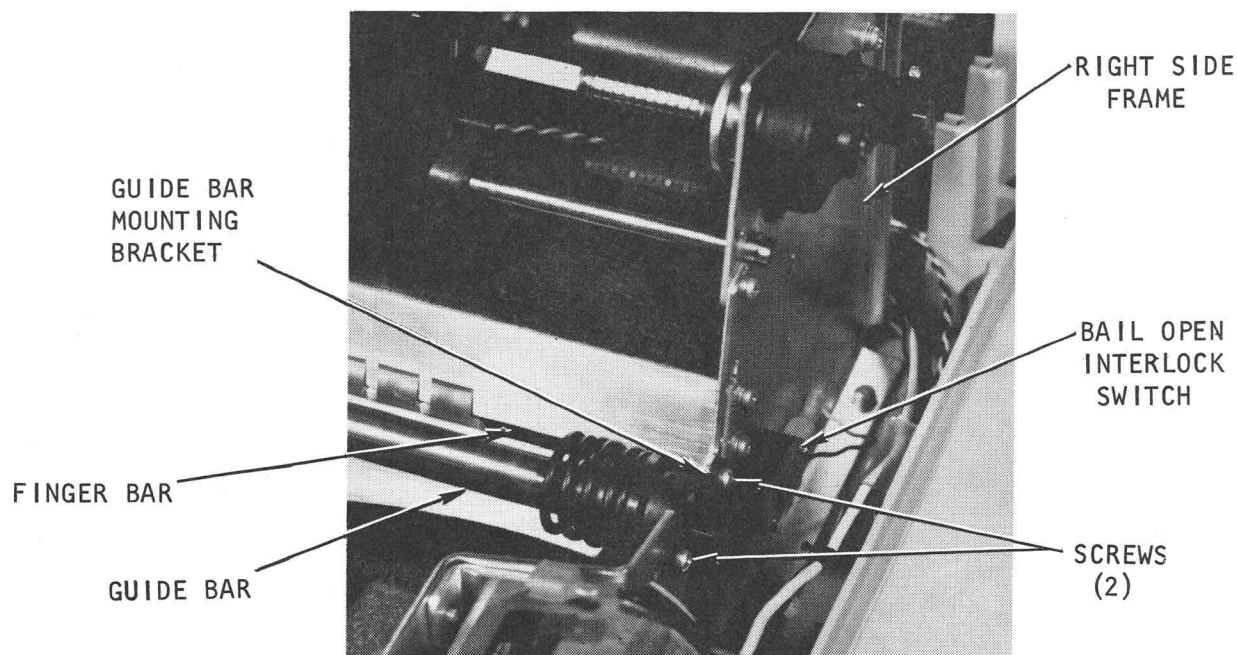
f. Remove the ribbon drive motor per paragraph 5.3.18. Do not disconnect the ribbon motor leads.



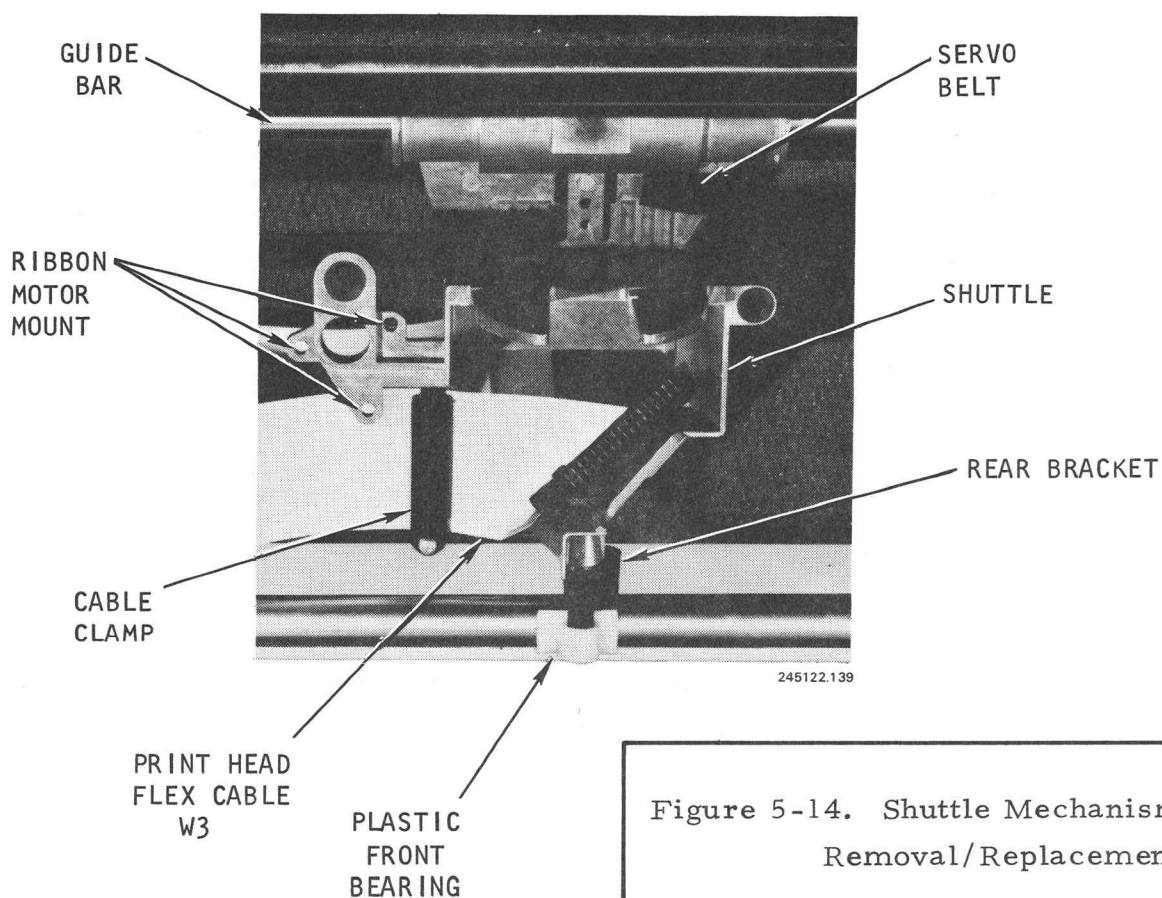
245122.115



245122.141



245122.140



245122.139

Figure 5-14. Shuttle Mechanism Removal/Replacement

- g. Remove the shuttle servo belt from the shuttle mechanism per paragraph 5.3.20.
- h. Loosen and remove the screw that mounts the cable clamp to the shuttle, and remove the cable clamp.
- i. Remove the two screws on the right side of the printer that secure the guide bar mounting bracket to the side frame.
- j. Lift the guide bar at the right end.
- k. Remove the front plastic bearing from the shuttle mechanism, then slide the shuttle mechanism to the right and out of the printer.
- l. To replace, insert the left side of the shuttle mechanism within the mounting hole on the left side frame, with the washer at the extreme end.
- m. Replace the plastic bearing on the shuttle, then position the bearing in the center on the front shuttle guide bar.
- n. Place the right side of the replacement shuttle mechanism within the cradle of the right side frame so that the actuating pin of the shuttle mechanism rests on the bail open interlock switch actuating arm. The lower part of the guide bar mounting bracket fits over the right end of the finger bar.
- o. Replace, but do not tighten, the two screws that secure the right side of the shuttle mechanism to the right side frame.
- p. Place the looped end of the platen gap lever tension spring over the peg protruding on the left side of the platen gap lever.
- q. With the platen gap lever in the closed (up) position, insert the straight end of the platen gap lever tension spring within the anchor hole in the left side frame.
- r. Tighten the two screws replaced in step o.

NOTE

When installing a new shuttle mechanism, it is necessary to adjust the rear bracket. This bracket is held to the shuttle frame by a screw through its center. To adjust, loosen the nut inside the frame and rotate the bracket until the lower bracket arm clears the bottom of the front guide bar by 0.002 inch (0.0508mm).

- s. Replace the shuttle servo belt per paragraph 5.3.20.
- t. Replace the print head locking mechanism per paragraph 5.3.19.
- u. Replace the ribbon drive motor per paragraph 5.3.18.

v. Reconnect the flex cable to the print head per paragraph 5.3.21, then replace the print head per paragraph 3.3.3.

w. Replace the cable clamp.

x. Replace the ribbon cassette per paragraph 3.3.2.

y. Replace the top cover per paragraph 5.3.1.

5.3.24 Idler Pulley Assembly Removal/Replacement (Figure 5-15)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the ribbon cassette per paragraph 3.3.2.

c. Loosen the shuttle servo belt by turning the belt tension adjustment knob counterclockwise. It is not necessary to completely remove the knob.

NOTE

The idler pulley assembly is housed within a recess on the left side of the shuttle mechanism frame and is held in place by belt tension. When the belt is slack, the assembly slips out of the recess, and is removed through a notched cutout.

d. With the belt loose, disengage the adjustment mechanism from the idler pulley frame, align the crosspiece of the idler pulley assembly with the notch in the cutout, then remove the assembly.

e. Remove the print head per paragraph 3.3.3.

f. Remove the print head locking mechanism per paragraph 5.3.19.

g. Slide the left end of the shuttle servo belt from the narrow slot to the wide slot, then remove the belt from the wide slot and slip it off the idler pulley.

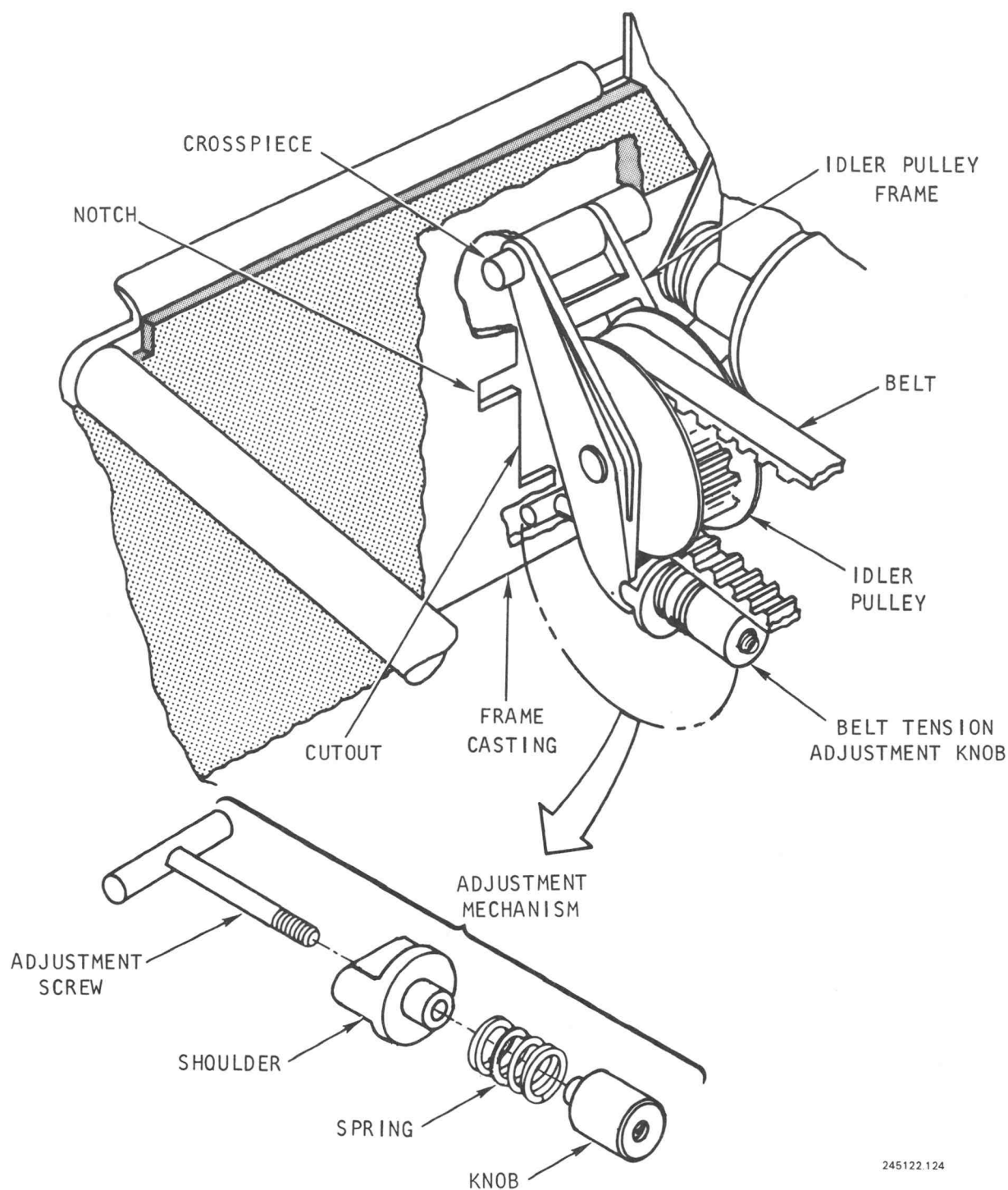
h. To replace, slip the left end of the belt under and around the new idler pulley.

i. Fit the crosspiece through the notch in the frame, and place the crosspiece into the recess in the frame.

j. Seat the adjustment mechanism in the idler pulley frame.

k. With one hand, maintain tension on the left side of the belt so that the idler pulley assembly remains seated within the recess.

l. With the other hand, place one segment of the open end of the belt within the wide slot, then secure the belt by sliding that segment within the narrow slot. Refer to figure 5-11.



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Figure 5-15. Idler Pulley Assembly Removal/Replacement

m. Tighten the belt with the adjustment knob by turning the knob clockwise until it touches the shoulder.

n. Replace the printhead locking mechanism per paragraph 5.3.19.

o. Replace the print head per paragraph 3.3.3.

p. Replace the ribbon cassette per paragraph 3.3.2.

q. Replace the top cover per paragraph 5.3.1.

5.3.25 Column 1 Harness Removal/Replacement (Figure 5-16)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Disconnect Column 1 harness W4 from its connector on the mother board.

c. Remove the three screws that secure the harness mounting bracket to the printer housing casting, and remove the harness.

d. Install the replacement harness by performing steps b and c in a reverse order.

e. Adjust, if required, per paragraph 5.4.6.

f. Replace the top cover per paragraph 5.3.1.

5.3.26 Paper Low Interlock Switch Removal/Replacement
(Figure 5-17)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the screw that secures the harness bracket to the printer housing casting, and remove the switch assembly.

c. Disconnect the cable from the switch by removing the small screws from the switch terminals. Note which wire is connected to which terminal.

d. Install the replacement switch assembly by performing steps b and c in reverse order, and adjust per paragraph 5.4.5.

e. Replace the top cover per paragraph 5.3.1.

5.3.27 Bail Open Interlock Switch Removal/Replacement (Figure 5-14)

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the two push-on connectors from the bail open interlock switch. Note which wire is connected to which terminal.

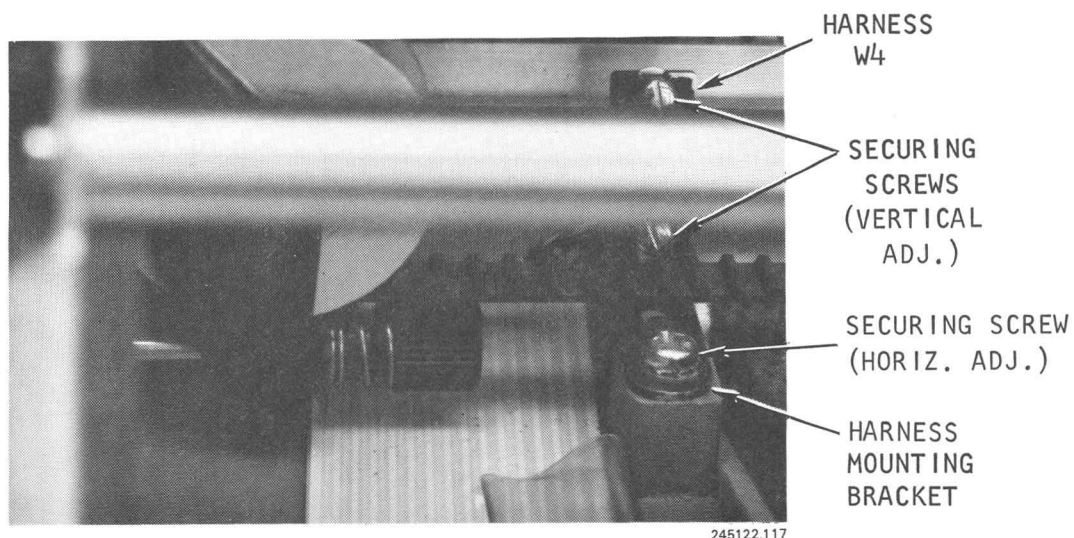


Figure 5-16. Column 1 Harness Removal/Replacement

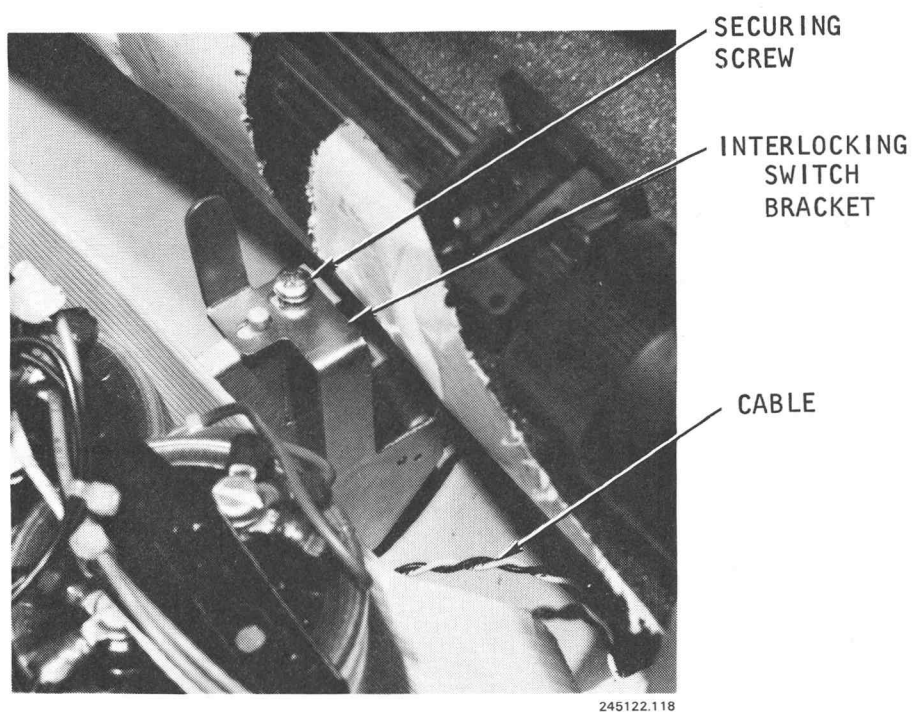


Figure 5-17. Paper Low Switch Interlock Assembly Removal/Replacement

c. Ensure that the platen gap lever shown in figure 5-14 is in the closed position (nearest the platen).

d. Remove the two screws, nuts, and lockwashers that secure the interlock switch to the printer frame.

NOTE

To gain access to the nuts and lockwashers for step d above, the acoustic insulation material must be raised.

e. Remove the interlock switch.

f. To replace, perform steps b through d in reverse.

g. Replace the top cover per paragraph 5.3.1.

5.3.28 Control Panel Circuit Card Assembly Removal/Replacement
(Figure 5-18)

The various replaceable control panel switches and indicators can be accessed when the control panel circuit card assembly is removed.

a. Remove the top cover per paragraph 5.3.1 (note WARNING).

b. Remove the three screws that secure the control panel CCA to the support bracket. If the control panel contains the optional form length selector switch, remove the switch knob.

c. Remove the support bracket.

d. To replace, disconnect the control panel harness (W2).

f. Tighten the three screws that secure the control panel CCA to the support bracket.

g. Replace the top cover per paragraph 5.3.1.

5.3.29 TCVFU (Option) Removal/Replacement (Figure 5-19)

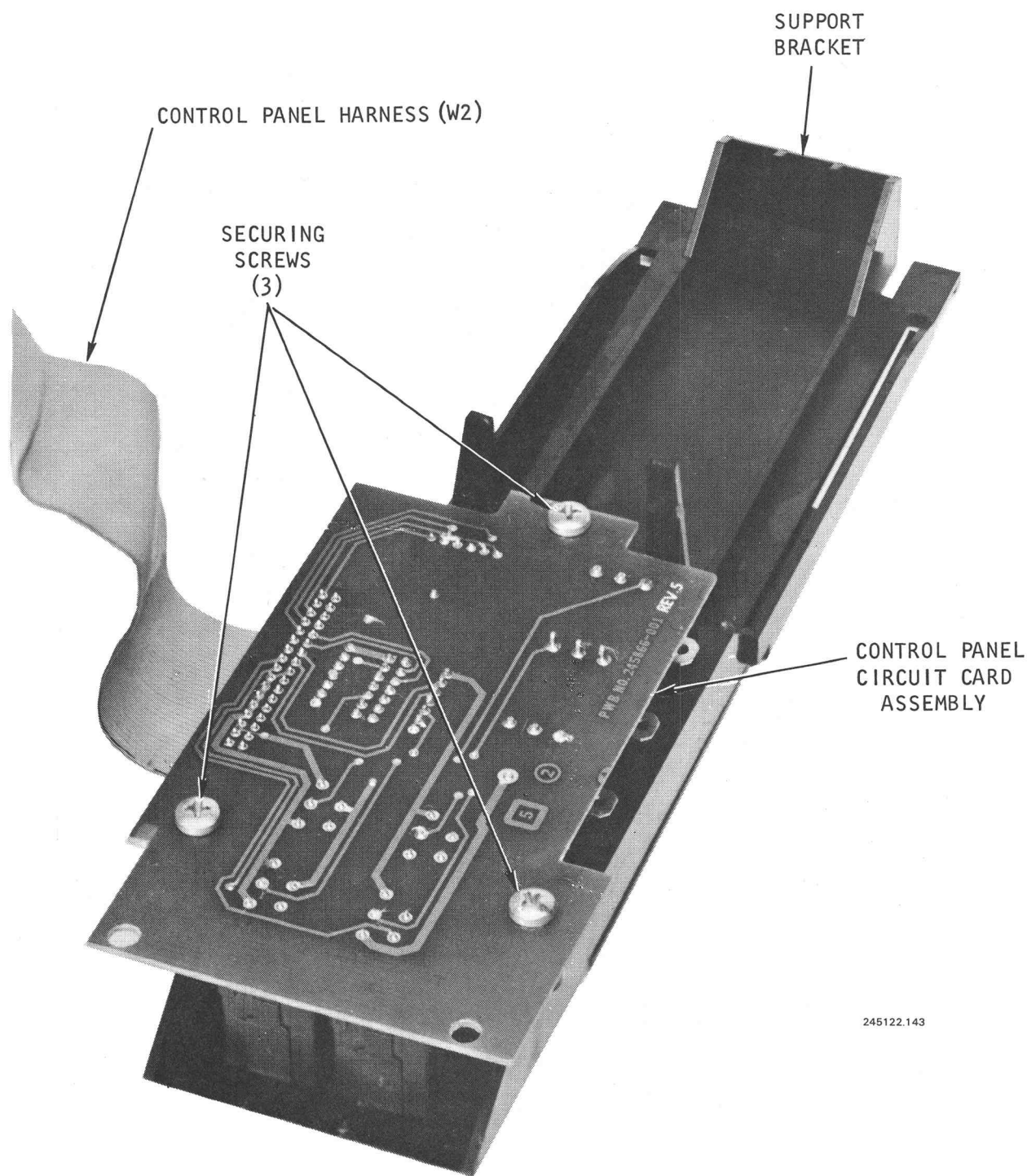
a. Disconnect the power plug from the power source.

b. Disconnect the TCVFU ribbon cable from J12 of the applicable Interface CCA.

c. Loosen and remove the two screws that fasten the TCVFU to the printer switch cover.

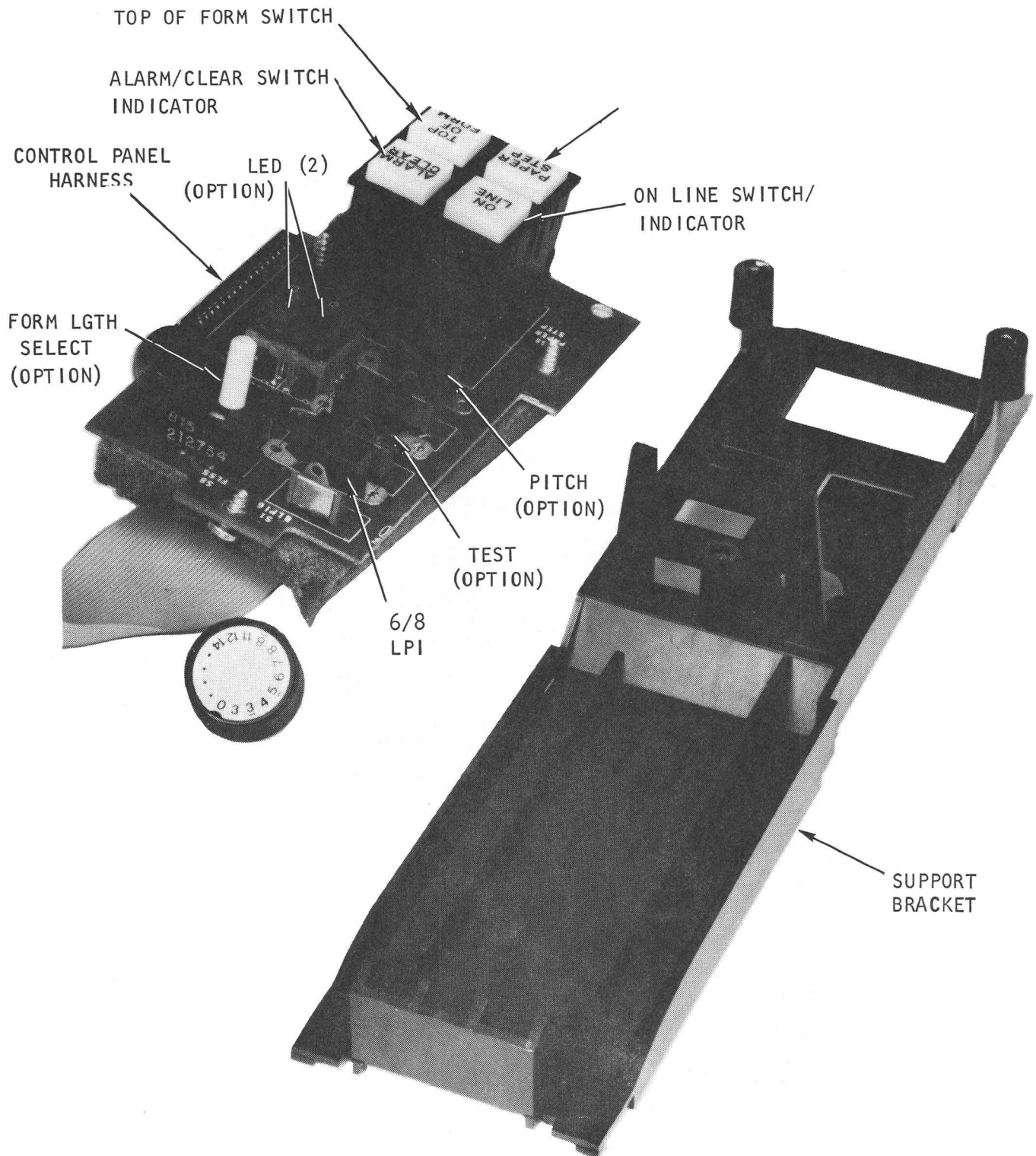
d. Carefully slide the TCVFU ribbon cable under the platen and out of the printer.

e. Remove the TCVFU from the printer.



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Figure 5-18. Control Panel Circuit Card Assembly Removal/Replacement

f. Replace, using the procedure of steps a through d in a reverse order.

5.4 ADJUSTMENTS

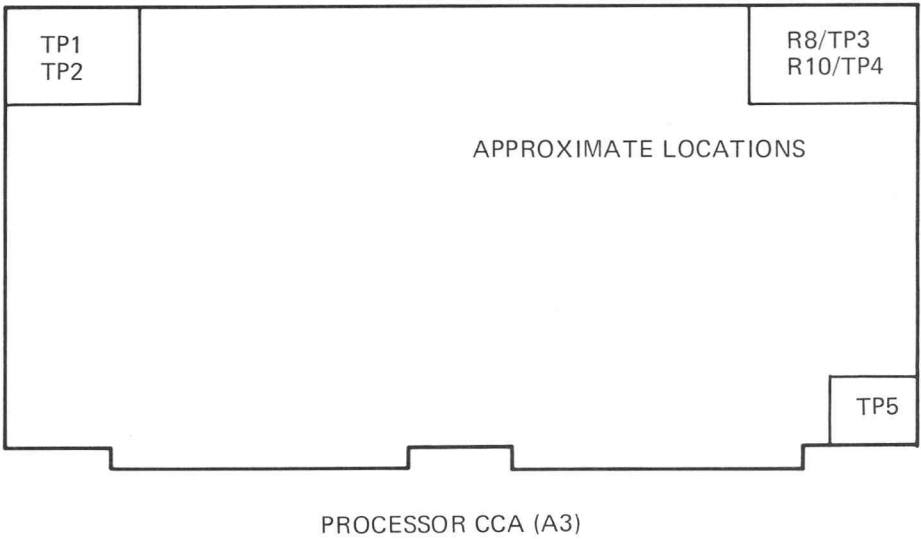
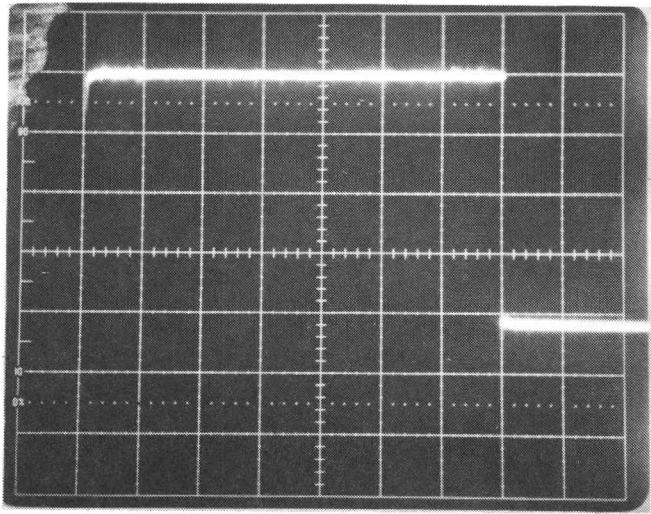
The following paragraphs contain procedures for performing both electrical and mechanical adjustments. Electrical adjustments are pre-set and sealed at the factory. However, on-site adjustments may be required when an electronic circuit card assembly or the shuttle servo motor has been removed and replaced.

The mechanical adjustments should be made whenever the related assembly/part has been removed and replaced. It is not necessary form these adjustments on a regularly scheduled basis.

5.4.1 Wire Driver On/Off Period (Figure 5-19)

This procedure requires the printer to be loaded with paper and the ribbon cassette and print head to be installed.

- a. Remove the top cover per paragraph 5.3.1.
- b. Connect an oscilloscope to TP-3 with a ground lead to TP-1 (Figure 5-19), and perform the following control settings on the oscilloscope:
 1. Vertical Intensity 1 VDC/DIV
 2. Auto Trigger
 3. Horizontal TIME/DIV 50 us
- c. Set the TEST switch to ON.
- d. Connect the power plug to the power source.
- e. Set the power switch S1 to the ON position.
- f. Momentarily press the ON LINE switch/indicator to start the print process.
- g. Monitor TP-3, and adjust R10 for the waveform shown in Figure 5-19 ($355\mu s \pm 15\mu s$).



3870-1

Figure 5-19. Wire Driver On/Off Period Test Points and Waveform

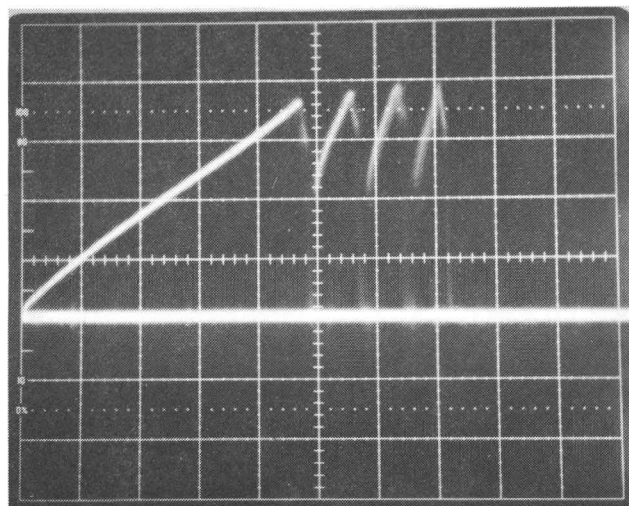
NOTE

In steps h and i, counterclockwise rotation will reduce the pulse width.

- i. Monitor TP-4 and adjust R8 for the waveform shown in Figure 5-19.
 - j. Set power switch/indicator S1 to the off position, and disconnect the power plug from the power source.
 - k. Remove the oscilloscope leads from TP-4 and TP-1 on the Processor CCA.
 - l. Replace the top cover per paragraph 5.3.1.
- 5.4.2 Wire Driver Current (Figure 5-20).
- a. Remove the top cover per paragraph 5.3.1.
 - b. Connect a dual channel oscilloscope with the A probe to the bottom side of R5 and the B probe to the top side of R5 (Figure 5-20), and perform the following control settings on the oscilloscope:
 - 1. Vertical Sensitivity - 1 VAC/DIV A and B.
 - 2. A and B Algebraic Add Function
 - 3. B - Invert
 - 4. Auto Trigger
 - 5. Horizontal TIME/DIV - 50us

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- d. Set the TEST ON/OFF switch to ON.
- e. Connect the power plug to the power source.
- f. Set the power switch/indicator to ON.
- g. Momentarily press the ON LINE switch/indicator to start the print process.
- h. Adjust R1 to obtain the waveform amplitude as shown in Figure 5-20 (3.8 VDC to 4.2 VDC).
- i. Set the power switch/indicator to OFF, and disconnect the power plug from the power source.
- j. Remove the oscilloscope leads from R5 on the Wire Driver CCA.
- k. Replace the top cover per paragraph 5.3.1.



WIRE DRIVER BOARD (A5)

3870-2

Figure 5-20. Wire Driver Current Monitoring Points and Waveform

5.4.3 Shuttle Speed Control (Figure 5-21)

This procedure requires the printer to be loaded with paper and the print head to be installed.

- a. Remove the top cover per paragraph 5.3.1.
- b. Connect an oscilloscope to TP-3 with a ground lead to TP-4 of the Motor Driver CCA (Figure 5-21), and perform the following control settings on the oscilloscope:
 1. Vertical sensitivity - 1 VDC/DIV
 2. Normal Trigger, Channel 1.
 3. Horizontal TIME/DIV - 100 ms
- d. Set the TEST ON/OFF switch to ON.
- e. Connect the power plug to the power source.
- f. Set power switch/indicator S1 to the ON position.
- g. Momentarily press the ON LINE switch/indicator to start the print process.

h. Adjust the oscilloscope trigger and horizontal display controls so the leading edge of the waveform occurs at the first vertical line (Figure 5-21).

i. Adjust R5 for the waveform shown in Figure 5-21 (945 ms +15 ms).

j. Set the power switch/indicator to the OFF position, and disconnect the power plug from the power source.

k. Remove the oscilloscope leads from the Motor Driver CCA.

l. Replace the top cover per paragraph 5.3.1.

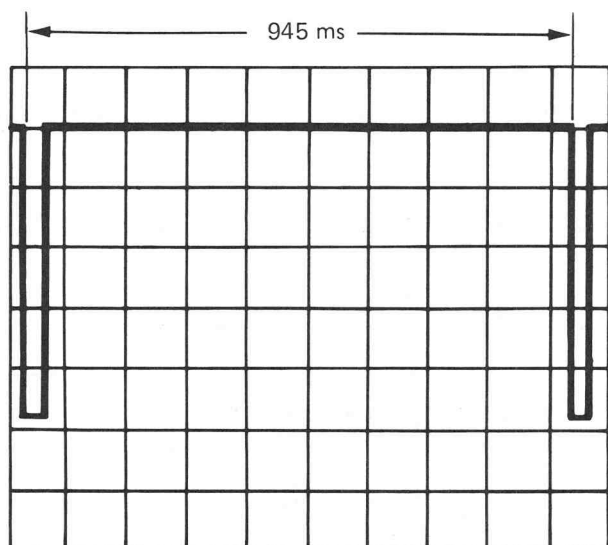
5.4.4 5 VDC (Figure 5-22)

a. Verify that the printer power cable is connected to the source of power and that power switch/indicator S1 is set to the OFF position.

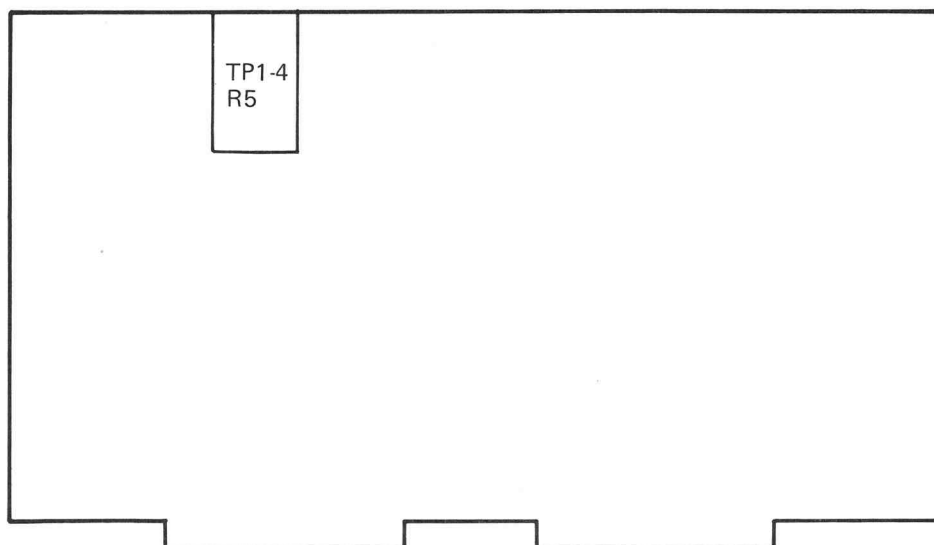
b. Remove the top cover per paragraph 5.3.1.

c. Connect a voltmeter positive lead to TP-2, negative lead to TP-1 on the Processor CCA (Figure 5-19).

d. Set the power switch/indicator to ON.



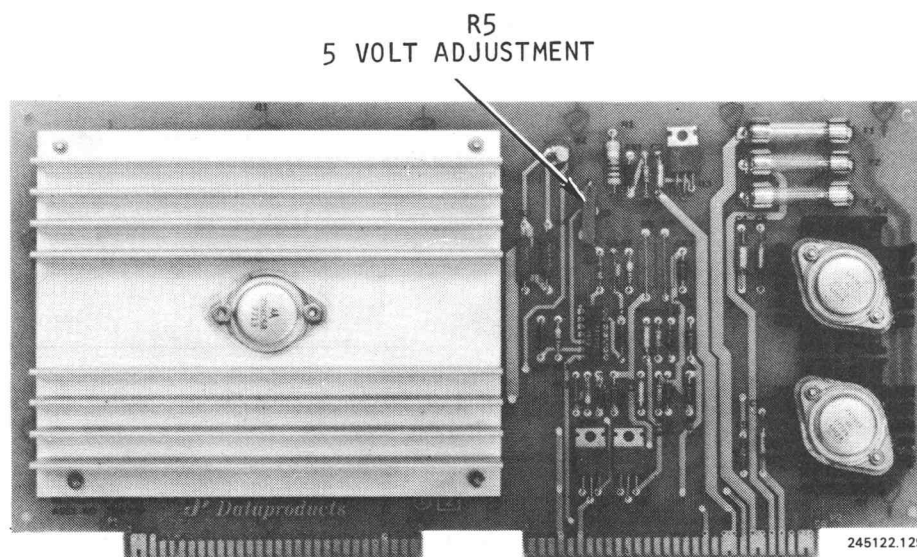
SCOPE SETTING
 VERTICAL SENSITIVITY = 1VDC
 HORIZONTAL SWEEP = 100 MILLSEC
 TRIGGER MODE = NORMAL



MOTOR DRIVER CCA (A4)

3870-3

Figure 5-21. Shuttle Speed Control Adjustment, Monitoring Point and Waveform.



REGULATOR CCA (A6)

Figure 5-22. 5 VDC Adjustment and Monitoring Points

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- e. Locate the Regulator CCA, and adjust R5 (Figure 5-20) for 5 +5% VDC.
- f. Set power switch/indicator S1 to the OFF position.
- g. Remove the voltmeter leads from the Processor CCA.
- h. Replace the top cover per paragraph 5.3.1.

5.4.5 Paper Low Interlock Switch (Figure 5-25)

- a. Remove the top cover per paragraph 5.3.1. (note WARNING).
- b. Load the printer with single copy paper per paragraph 3.3.1.
- c. Loosen the screw that secures the switch mounting bracket to the printer casting (see figure 5-17).
- d. Ensure that the platen gap lever is in the closed position after loading paper.
- e. Position the switch mounting bracket so that the switch actuating arm (see figure 5-25) actuates the switch into the closed position when pressed against the paper, and tighten the screw. Switch closure is indicated by an audible click.
- f. Connect the power plug to the power source.
- g. Place the power switch to the on position and verify that the ALARM/CLEAR indicator remains extinguished. If the ALARM/CLEAR indicator illuminates, place the power switch to the off position and repeat steps d through g.

NOTE

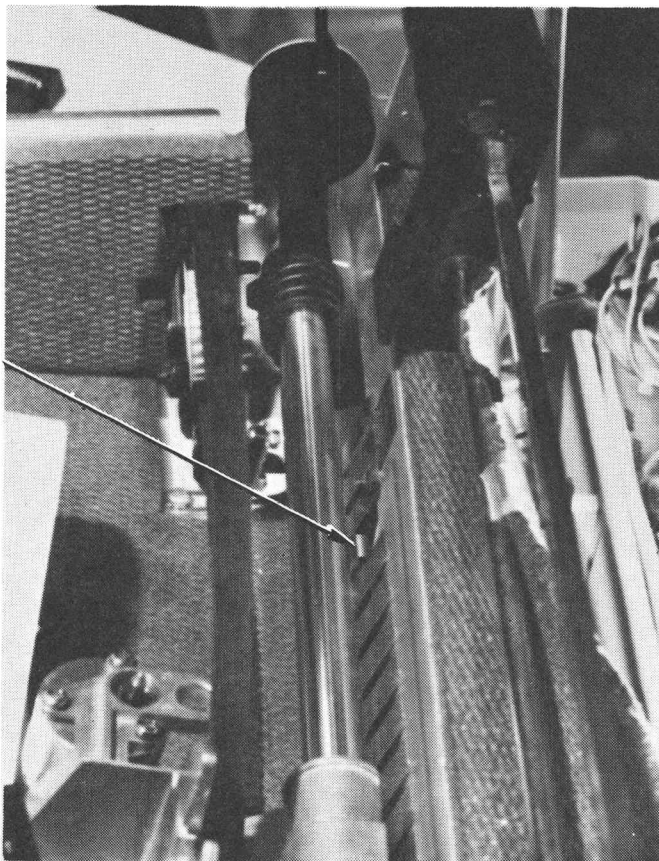
The ALARM/CLEAR indicator will illuminate when the paper low interlock is in the open position and printing is attempted.

- h. Press the PAPER STEP switch until the last form exits from the printer. The ALARM/CLEAR switch will illuminate when self-test is initiated.
- i. Place the power switch to the off position, and disconnect the power plug from the power source.
- j. Replace the printer cover per paragraph 5.3.1.

5.4.6 Column 1 Harness (Figure 5-26)

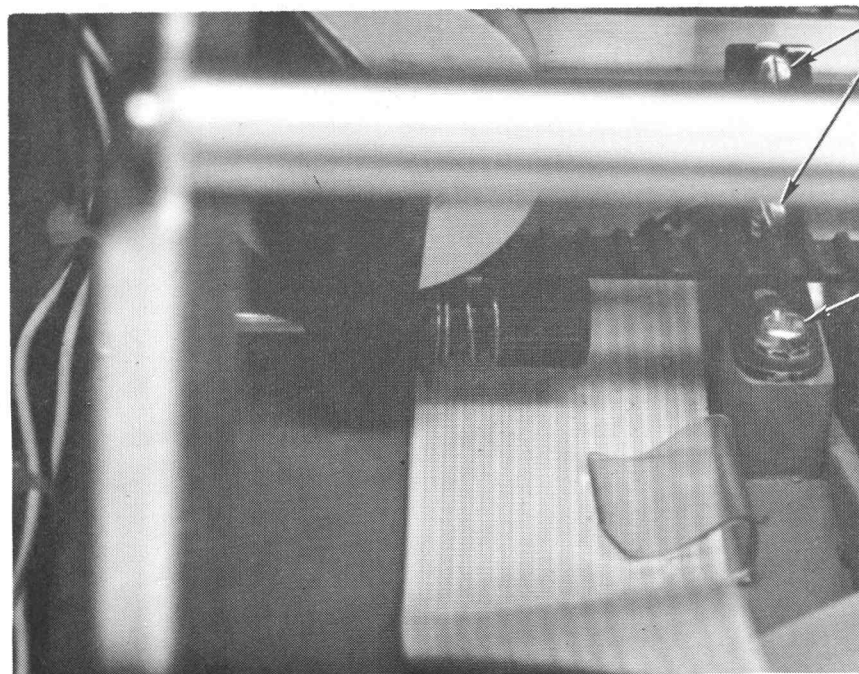
The purpose of this adjustment is to ensure that the flange on the shuttle mechanism does not interfere with the column 1 harness. Adjustment involves positioning the column 1 harness up or down, or in or out, as necessary, until it clears the flange. The procedure is as follows:

PAPER LOW
INTERLOCK
SWITCH
ACTUATING ARM



245122.130

Figure 5-23. Paper Low Interlock Switch Adjustment



VERTICAL
ADJUSTMENT
MOUNTING
SCREWS

HORIZONTAL
ADJUSTMENT
MOUNTING
SCREW

245122.117

Figure 5-24. Column 1 Harness Adjustment

- a. Remove the top cover per paragraph 5.3.1 (note WARNING).
- b. Remove the ribbon cassette per paragraph 3.3.2.
- c. If the column 1 harness is not in the correct vertical position, loosen the two vertical adjust mounting screws and slide the column 1 harness up or down, as necessary, to obtain the correct vertical position. Tighten the screws.
- d. If the column 1 harness is not in the correct forward/backward position, loosen the horizontal adjustment mounting screw and slide the column 1 harness in or out, as necessary, to obtain the correct horizontal position. Tighten the screw.
- e. Replace the ribbon cassette per paragraph 3.3.2.
- f. Replace the top cover per paragraph 5.3.1.

5.4.7 Shuttle Servo Belt (Figure 5-27)

The tension of the shuttle servo belt is set by means of the belt tension adjustment knob. For proper tension, turn the knob against the spring tension clockwise until it just makes contact with the shoulder.

5.4.8. Paper Feed Belt (Figure 5-28)

The tension of the paper feed belt is controlled by the position of the paper feed step motor.

- a. Remove the top cover per paragraph 5.3.1. (note WARNING).
- b. Loosen the three screws that secure the paper feed step motor to the shuttle and platen assembly frame.
- c. Position the paper feed motor so that the paper feed belt is taut.
- d. Tighten the three screws that secure the paper feed step motor to the shuttle and platen assembly frame.
- e. Replace the top cover per paragraph 5.3.1.

5.4.9 Head-to-Platen Alignment (Figure 5-29)

With no paper installed and form thickness control set to position 1, the gap between the face of the print head and the platen is $.015 \pm .001$ inch ($0.381\text{mm} \pm 0.0254$). The carriage guide bar is mounted to the side frame in bushings with eccentrics. The position of the bar is controlled by the platen gap lever/cam used to open the print station. To achieve the required gap dimension, the screw securing the lever to the shaft is loosened and the shaft is manually rotated.

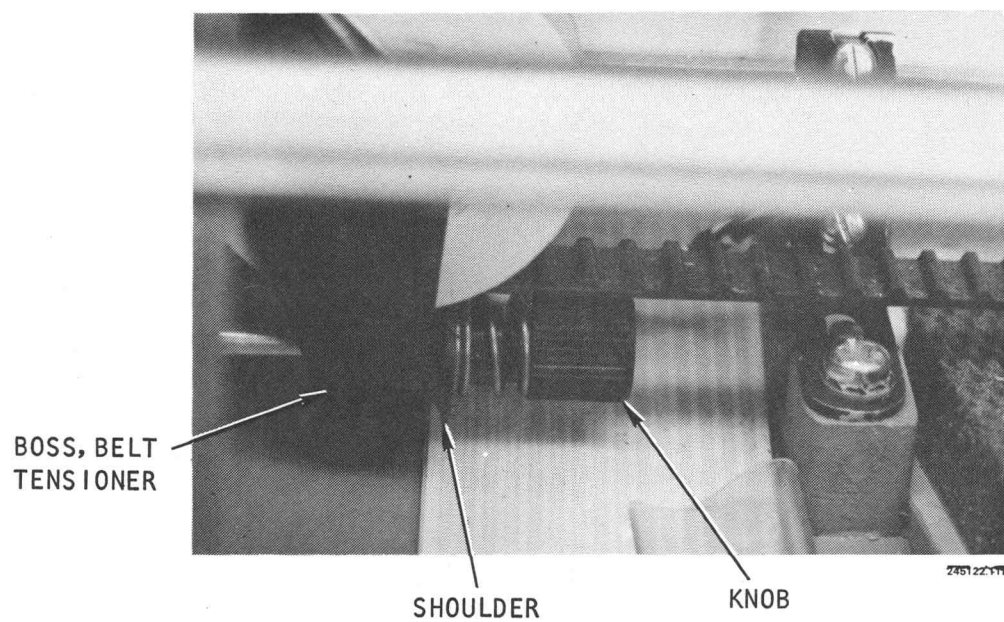


Figure 5-25. Shuttle Servo Belt Adjustment

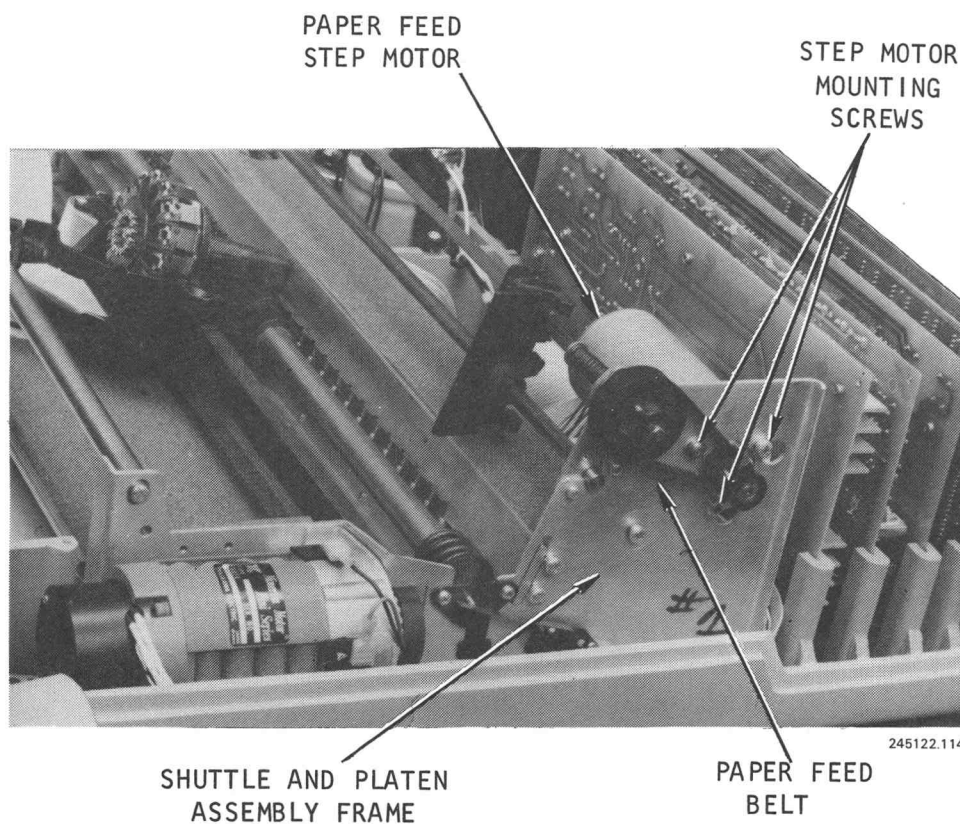


Figure 5-26. Paper Feed Belt Adjustment

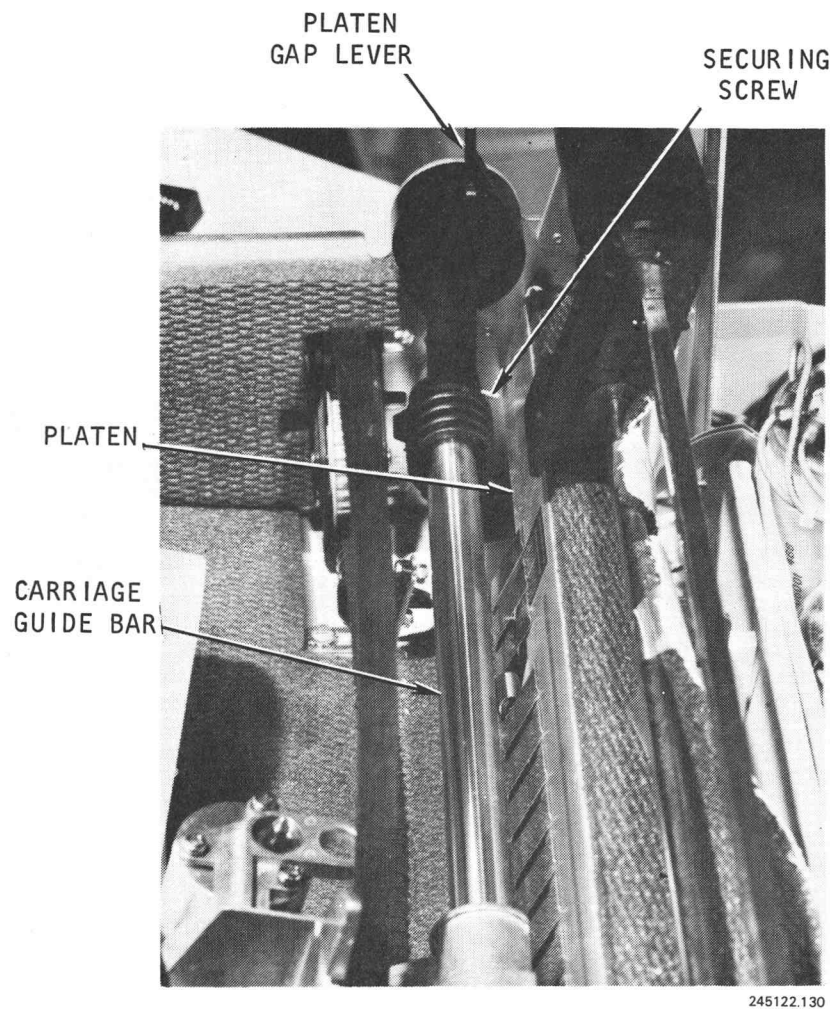


Figure 5-27. Head to Platen Alignment

SECTION VI

OPTIONS

NOTE

Contact your nearest Tektronix field office or representative concerning any options not included in the standard instrument.

6.1 INTRODUCTION

This section describes the options available for the printer and their functions. Options described in this section are as follows:

- a. Universal Power Supply
- c. Print Density Options
- d. Format Control Options
- e. Optional Interface Signals
- f. Interface Connector
- g. Long-Line Interface
- h. DPC Centronics-Compatible Interface
- i. Serial Interface
- j. Automatic Line Feed
- k. Diagnostic Display
- l. Elapsed Time Meter
- m. Rear Forms Load
- n. Pedestal
- o. Paper Receptacle
- p. Ground Isolation
- q. Seven Bit Only Interface

6.2 UNIVERSAL POWER SUPPLY

The universal power supply allows the printer to accept operating power from a variety of sources having the following voltages and frequencies:

Voltage:	90 to 136, 187 to 257 VAC
Frequency:	50 or 60 Hz \pm 1 Hz
Phase:	Single

OPTIONS

Changing from one combination to another is accomplished without the need to replace components or assemblies (refer to paragraph 2.6). When the printer is configured with the universal power supply, the power cord will not include a two-pole universal connector plug.

OPTIONS

6.4 PRINT DENSITY OPTIONS

The printer can be configured to produce non-standard character and line spacing, as follows:

6.4.1 Condensed Character Spacing

This option allows the printer to print with a horizontal pitch of 16.7 characters per inch, in addition to the standard spacing of 10 characters per inch. A switch located on the Auxiliary Control Panel allows selection of either standard or condensed pitch. An octal 22 control code may be used to override this switch and enable condensed printing, regardless of switch setting. To reset the pitch to that established by the switch before override, any format code may be used.

Implementation of this option requires the use of the OPTION HEADER.

6.4.2 Selectable Line Pitch

This option allows the operator to select a vertical pitch of either 6 or 8 lines per inch by means of a switch located on the Auxiliary Control Panel. Selection of vertical pitch cannot be made by interface code. Underlining is not permitted when operating in the 8 lines per inch mode. Any underlined characters transmitted to the printer when 8 lines per inch is selected will be converted to blanks.

6.5 FORMAT CONTROL OPTIONS

The following format control options are described in this paragraph:

- a. Fixed Form Length
- b. Variable Perforation Skipover
- c. Forms Length Selector Switch
- d. Tape Controlled Vertical Format Unit
- e. Direct Access Vertical Format Unit

6.5.1 Fixed Form Length

The basic printer is configured to provide automatic TOP OF FORM positioning when used with 11-inch forms. This feature may be optionally modified to allow use of 12-inch forms to suit international requirements. Implementation of this modification requires the use of the OPTION HEADER. Requirements for operation with other form lengths can be met by use of the Form Length Selector Switch (paragraph 6.5.3) or the Vertical Format Unit options (Paragraphs 6.5.4 or 6.5.5).

6.5.2 Variable Perforation Skipover

The standard 3-line skipover distance may be modified to 0, 4, or 6-line skipover by means of jumpers installed on the OPTION HEADER.

OPTIONS

The presence of either vertical format unit (TCVFU or DAVFU) transfers control of the skipover distance to the Bottom of Form and Top of Form data contained in the VFU memory.

6.5.3 Form Length Selector Switch

This option allows the operator to handle a variety of commonly used forms lengths and to automatically advance the paper to the top of form by means of an interface code or the TOP OF FORM switch on the Control Panel. Selection of one of eleven forms lengths is made by means of a rotary switch located on the Auxiliary Control Panel. The switch positions correspond to the forms lengths of 3, 3½, 4, 5½, 6, 7, 8, 8½, 11, 12, and 14 inches. Switch positions A through E default to 11-inch form lengths.

6.5.4 Tape Controlled Vertical Format Unit (TCVFU)

The Tape Controlled Vertical Format Unit (TCVFU), consisting of an optical tape reader and associated electronics, is offered as an option to enable the handling of a variety of vertical formats, and to allow rapid paper slewing within individual formats.

Data is read from tape following each power-up operation, and stored in memory. The memory load will start when a hole is detected in the least significant tape channel (left-most), and continues until a hole is again detected in this channel.

Tape load operation is initiated by pressing the tape reader switch, located on the tape reader assembly, when the printer is in the off-line mode. VFU memory is loaded (1) when the printer is powered up, (2) following any tape change, or (3) following the detection of a VFU error. If an error occurs while loading tape, the ALARM indicator will illuminate. To recover, the CLEAR switch must be pressed and the load operation repeated. At the end of the operation, indicated by the tape coming to a stop, the tractors will be synchronized with the memory at the Top of Form position.

Once the memory has been loaded, the tape reader turns off and all mechanical activity ceases. VFU instructions are transmitted to the printer by activating the Paper Instruction (PI) bit at the same time that coded instructions are presented on the data lines.

As paper is advanced, the buffer memory is electronically "rotated" in synchronization, as a tape loop would be rotated in a mechanical system. Turning off the power will result in loss of synchronization between form and TCVFU.

Implementation of this option requires the OPTION HEADER.

6.5.5 Direct Access Vertical Format Unit (DAVFU)

The Direct Access Vertical Format Unit (DAVFU) is offered as an option to enable handling of a variety of vertical formats, and allow paper slewing within a form in a manner identical to the TCVFU described in paragraph

6.5.4. Instead of loading the memory from a tape loop, the DAVFU provides for direct loading from the user system via the printer interface lines.

A DAVFU START code (156 octal) accompanied by print instruction signal PI, may be sent to the printer at any time data is requested. Upon recognition of the DAVFU START code, subsequent codes are used to load the VFU memory rather than to cause printing or paper motion.

Once the number of memory positions corresponding to the length of form (252 lines maximum) has been loaded, a STOP LOAD code (157 octal) accompanied by paper instruction signal PI, is sent to the printer. This code causes the printer to return to the normal mode whereby all recognized codes are used for printing or paper motion. Once the memory has been loaded via the interface, DAVFU-controlled paper motion instructions and operation are identical to those of TCVFU.

Once the DAVFU is loaded, the Form Length Selector Switch (Paragraph 6.5.3), and the Perforation Skipover feature (paragraph 6.5.2) are disabled. Perforation Skipover will occur whenever BOF is detected and will stop when TOF is detected.

Implementation of this option requires the OPTION HEADER.

6.6 OPTIONAL INTERFACE SIGNALS

The following optional interface signals are available with both the standard DPC Short-Line Parallel Interface and the optional DPC Long-Line Parallel Interface.

a. PARITY BIT

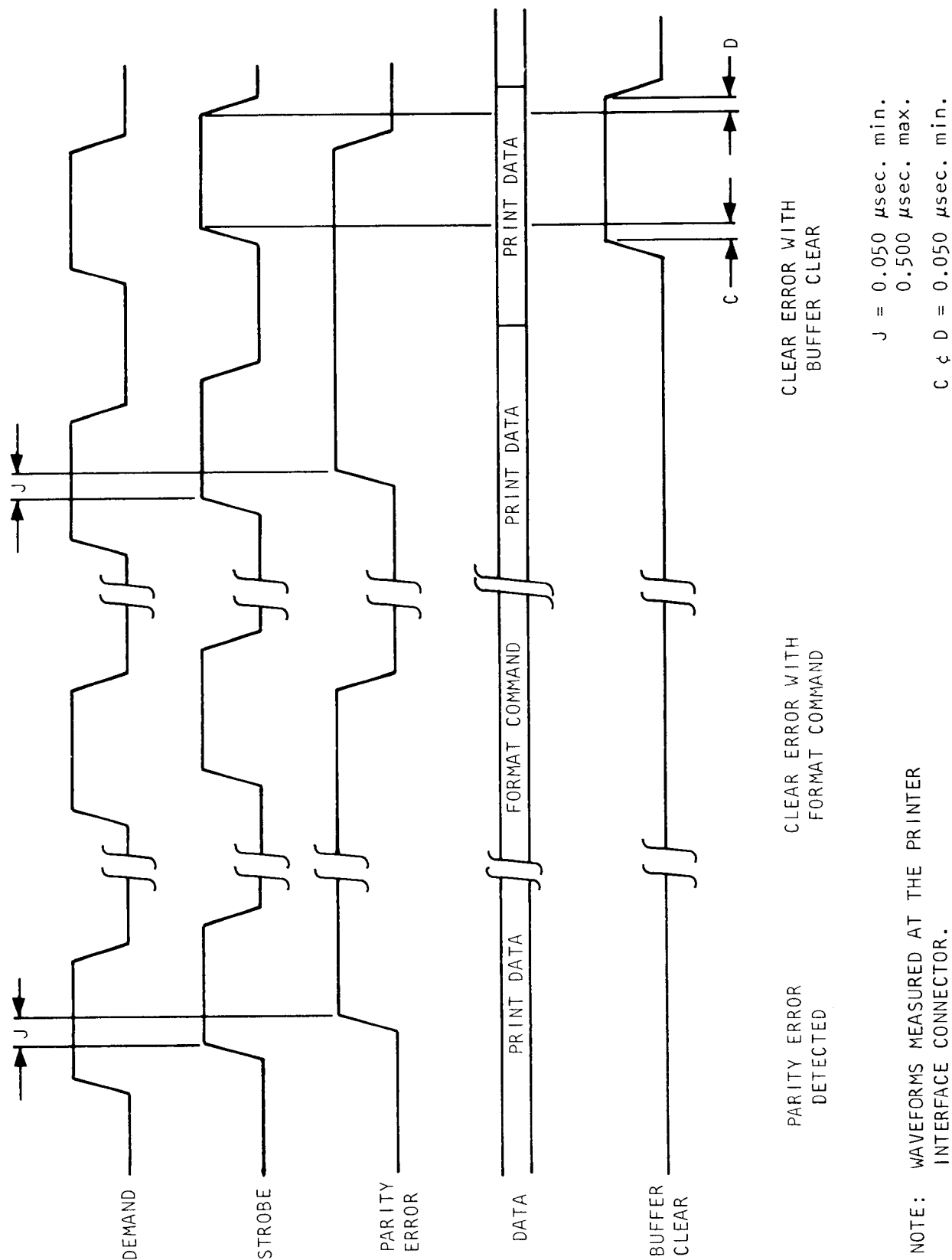
This user-generated signal is used when Parity Error detection is required. If odd parity is selected, the PARITY BIT signal must be active when the total number of active high data bits (including the PAPER INSTRUCTION signal, if used) is even. If even parity is selected, the PARITY BIT signal must be active whenever the total number of active high data bits (including the PAPER INSTRUCTION signal, if used) is odd. Implementation of this option requires the OPTION HEADER.

b. PARITY ERROR

This printer-generated signal informs the user that a parity error has been detected on interface data. The PARITY ERROR signal can be reset by either BUFFER CLEAR or a format code. The timing constraints for this signal are shown in figure 6-2.

c. PAPER INSTRUCTION

This user-generated signal informs the printer that information on the data lines is to be treated either as format data, or as a DAVFU start or stop code. This signal can only be used when the TCVFU or DAVFU option is installed; however, a line of data can be terminated, using the standard ASCII



245122 1 31

Figure 6-2. Parity Error Generator, Timing Diagram

format codes (Paper Instruction signal inactive) even though the TCVFU or DAVFU option is installed. The paper Instruction signal is looked at only when the DEMAND signal is active.

d. BOTTOM OF FORM

This printer-generated signal is supplied to the user, and is active when the bottom of form (BOF) position has been reached. The BOF position is determined by the form length as wired in the standard printer, or as dictated by the TCVFU or DAVFU data when these options are enabled.

e. TOP OF FORM

Same as BOF above except the top of form position is transmitted.

f. PAPER MOVING

This printer-generated signal informs the user that the paper feed motor is energized.

6.7 INTERFACE CONNECTOR

An optional 50-pin Winchester connector with pin assignments, as listed in table 6-2, is available. The Winchester mating connector and pins are not supplied with the printer.

6.8 LONG-LINE INTERFACE

The optional Long-Line Interface is a modified version of the standard DPC Short-Line Parallel Interface. It allows the user to communicate with the printer over an extended cable length of up to 492 feet (150 meters). Signals between the user and the printer should be transmitted over twisted pair wires, using 22 AWG wire with one to three twists per inch. In all other respects, this interface is identical to the standard DPC Short-Line Parallel Interface.

OPTIONS

TABLE 6-2. DATAPRODUCTS INTERFACE 50-PIN WINCHESTER
CONNECTOR PIN ASSIGNMENTS

Signal	Pin	Signal	Pin
READY	CC	DATA 1	B
READY RTN	EE	DATA 1 RTN	D
ON LINE	<u>y</u>	DATA 2	F
ON LINE RTN	AA	DATA 2 RTN	J
DEMAND	E	DATA 3	L
DEMAND RTN	C	DATA 3 RTN	N
PARITY ERROR	<u>r</u>	DATA 4	R
PARITY ERROR RTN	<u>t</u>	DATA 4 RTN	T
BOTTOM OF FORM	M	DATA 5	V
BOTTOM OF FORM RTN	P	DATA 5 RTN	X
INTERFACE IN	<u>v</u>	DATA 6	Z
INTERFACE OUT	<u>x</u>	DATA 6 RTN	<u>b</u>
PAPER MOVING	W	DATA 7	<u>n</u>
PAPER MOVING RTN	Y	DATA 7 RTN	<u>k</u>
TOP OF FORM	S	DATA 8	<u>u</u>
TOP OF FORM RTN	U	DATA 8 RTN	<u>w</u>
+5 VOLTS	HH	PARITY	<u>z</u>
GND	FF	PARITY RTN	BB
		PAPER INSTRUCTION	<u>p</u>
		PAPER INSTRUCTION RTN	<u>s</u>
		STROBE	<u>j</u>
		STROBE RTN	<u>m</u>
		BUFFER CLEAR	A
		BUFFER CLEAR RTN	H

NOTE: Underscoring denotes lower case characters.

6.9 DPC CENTRONICS-COMPATIBLE INTERFACE

The DPC Centronics-Compatible Interface allows the user to interface with the DPC M200 printer in a manner compatible with Centronics printers. Data is transmitted over a short cable with a maximum length of 49 feet (15 meters), using twisted pair wires.

6.9.1 Logic Levels

Logical "1" = More positive than +2.4 VDC, and less positive than +5 VDC.

Logical "0" = More positive than 0 VDC and less positive than +0.4 VDC

Interface signals, with some exceptions, are active when in the logical "1" state. Exceptions: Signals DATA STROBE, ACKNOWLEDGE, INPUT PRIME, and FAULT are active when in the logical "0" state.

6.9.2 Operation and Interface Timing

The operation and interface timing of the DPC Centronics-Compatible Interface are described in detail in section IV of this manual.

6.9.3 Interface Connector

The interface connector mounted on the printer is a 50-pin AMP HDP-20, with pin assignments as listed in section IV of this manual. Mating connector and contact pins are not supplied with the printer. An optional adapter cable that terminates in a Centronics-type 36-pin connector is available. Table 6-3 lists the pin assignments of the Centronics-type-36-pin connector.

OPTIONS

Table 6-3. DPC CENTRONICS-COMPATIBLE INTERFACE 36-PIN CONNECTOR PIN AND SIGNAL ASSIGNMENTS

Pin	Signal	Definition
13	SLCT (SELECT)	A printer-generated signal which indicates that the printer has been selected. When SLCT signal is active: <ul style="list-style-type: none"> (a) The ALARM light is off. (b) The printer operator has pressed the ON LINE switch, or an octal (021) has been received via the data bus. (c) The printer is ready to accept data.
10	ACKNLG*	A printer-generated signal which acknowledges that the printer has received a data word. If the data word produces a busy condition, the acknowledge signal will not be generated until the busy condition is reset.
28	ACKNLG RTN*	
1	DATA STROBE*	A user-generated signal which defines when information on the data lines is stable and may be stored in the printer buffer.
19	DATA STROBE RTN*	
11	BUSY	A printer-generated signal that indicates that the printer is unable to receive print or format data. A select code can be transmitted during a busy condition.
29	BUSY RTN	
31	INPUT PRIME*	A user-generated signal that clears the printer buffer and initializes the interface logic. The input prime signal is asynchronous to the interface logic. This signal does not affect print or paper motion cycles.
30	INPUT PRIME RTN*	
32	FAULT	A printer generated signal indicating that one of the following faults has occurred. <ul style="list-style-type: none"> (a) Printer is out of paper (b) Shuttle is not moving (c) Printer is not selected

TABLE 6-3. DPC CENTRONICS-COMPATIBLE INTERFACE 36-PIN
CONNECTOR PIN AND SIGNAL ASSIGNMENT (Contd)

Pin	Signal	Definition
15	OSCXT OSCXT RTN	A printer-generated signal that transmits a 100 kHz square wave to the user.
12	PE PAPER INSTRUCTION PAPER INSTRUCTION RTN	A printer-generated signal that indicates the printer is Out of Paper. This user-generated signal informs the printer that information on the data lines is to be treated as format data. This signal can only be used when the TCVFU or DAVFU option is installed; however, a data line can be terminated using the standard ASCII format codes (PAPER INSTRUCTION signal inactive) even though the TCVFU and DAVFU options are installed. Note: The PAPER INSTRUCTION signal is looked at only when the Strobe Signal is active.
2 20	DATA 1 DATA 1 RTN	User Data
3 21	DATA 2 DATA 2 RTN	User Data
4 22	DATA 3 DATA 3 RTN	User Data
5 23	DATA 4 DATA 4 RTN	User Data
6 24	DATA 5 DATA 5 RTN	User Data
7 25	DATA 6 DATA 6 RTN	User Data
8 26	DATA 7 DATA 7 RTN	User Data
9 27	DATA 8 DATA 8 RTN	User Data

OPTIONS

6.9.4 Parameter Switches

There are three parameter switches in the DPC Centronics-Compatible Interface CCA:

a. SW1-2

When set to OFF, enables auto print, causing printer to print automatically following receipt of 132 characters (normal) or 220 characters (condensed). When set to ON, disables auto print.

b. SW1-3

When set to OFF, enables 220-character auto print. When set to ON, disables 220-character auto print, causing printer to print automatically after 132 characters (provided that auto print is enabled), even when the printer is in the condensed mode.

c. SW1-4

When set to ON, enables CR termination, causing printer to terminate data load cycle upon receipt of a carriage return code. When set to OFF, printer will not stop loading data upon receipt of a carriage return code.

6.10 SERIAL INTERFACE

The serial interface operates in an asynchronous receive-only mode, and may be used with or without a modem. Serial data is received from the user via current loop or standard EIA RS232 receivers. The interface will operate with a variety of baud rates ranging from 110 to 9600. Signals are transmitted over a cable with a maximum length of 50 feet (15.3 meters).

6.10.1 Logic Levels

a.	<u>RS-232C</u> -	MARKING OFF	SPACING ON
		-3.0 VDC to -25 VDC	+3.0 VDC to +25 VDC

b. 20 mA Current Loop

MARKING IDLE	SPACING BREAK
17.0 mA to +20 mA	0.0 mA to 1 mA

6.10.2 Operation

Serial interface operation is described in detail in section IV of this manual.

6.10.3 Interface Connector

The interface connector mounted on the printer is a 50-pin AMP HDP-20. Pin assignments are as listed in section IV of this manual. Mating connector and pins are not supplied with the printer. An optional adapter cable is available that terminates in a 25-pin HDP-20 connector. Table 6-4 lists the 25-pin connector pin assignments.

TABLE 6-4. SERIAL INTERFACE 25-PIN CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Definition
7	(AB)	Signal Ground - This conductor establishes the common ground reference potential for all interface circuits.
1	(AA)	N/C
3	(BB)	Received Data - This user-generated signal transmits all print, format and control code information to the printer. This signal will only be looked at when the following signals are in the on condition: <ul style="list-style-type: none"> (1) Data Terminal Ready (2) Data Set Ready (Optional) (3) Received Line Signal Detector (Optional)
20	(CD)	Data Terminal Ready - DTR - This printer-generated signal indicates that the printer is able to receive data. This signal is on when: <ul style="list-style-type: none"> (1) Printer power is on (2) No printer fault exists (3) Printer is on line (4) Print buffer is not full <p>If the DTR signal goes off due to a Paper Out condition, it is possible that valid data may still be stored in the printer buffer. In order to print the remaining data, paper must be reloaded and the on line mode re-entered via the on line control panel switch. Any data remaining in the buffer will be printed and the printer will receive more data as soon as the DTR signal goes on.</p>

TABLE 6-4. SERIAL INTERFACE 25-PIN CONNECTOR PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
11, 19	BUSY	<p>This printer-generated signal is used to send status to the user. BUSY will be in the on condition whenever:</p> <ol style="list-style-type: none"> (1) Data Terminal Ready is in the off condition. (2) Input Buffer is more than 3/4 full. <p>Data loading can continue after BUSY goes active; however, any data transmitted after the buffer is full will not be stored in the printer and the DTR signal will go off.</p>
17*	(RxD+)	<p>Receive Data Plus - This user-generated signal transmits all print and control code information to the printer. This pin is positive with respect to (RxD-) when loop current is flowing (marking). This signal also indicates the status of the user equipment. Current is maintained in the loop, except while data is being transmitted, to indicate that the user equipment is in a ready condition. The absence of loop current for the period of one full transmission character will be interpreted by the printer as BREAK, indicating that the user equipment is not in a ready condition.</p>
16*	(RxD-)	<p>Receive Data Minus - This signal is the current loop return for Receive Data.</p>
14*	(TxD+)	<p>Transmit Data Plus - This printer-generated signal indicates that the printer is able to receive data. Current is allowed to flow in the transmit loop when:</p> <ol style="list-style-type: none"> (1) Printer power is on. (2) No printer faults exist (3) Printer has been placed on line (4) Print buffer is not full (5) Printer is not BUSY <p>This pin is positive with respect to (TxD-) when loop current is flowing ("Ready").</p>
13*	(TxD-)	<p>Transmit Data Minus - This signal is the current loop return for Transmit Data.</p>

TABLE 6-4. SERIAL INTERFACE 25-PIN CONNECTOR PIN ASSIGNMENTS (Contd)

Pin	Signal	Definition
6*	(CC)	Data Set Ready - This user-generated signal indicates the status of the user equipment. The off condition of the DSR signal indicates that the printer must disregard signals on the other interface lines. The on condition indicates that the user equipment is in a ready condition.
4	(CA)	Request to Send - This printer-generated signal is held in the off condition to maintain the printer in the receive only mode.
8	(CF)	Received Line Signal Detector - This user-generated signal, when in the on condition, indicates that the data communication equipment is receiving a signal from the signal source which meets its suitability criteria. These criteria are established by the data communication equipment manufacturer.
5	(CB)	Clear to Send - This user-generated signal indicates that the user system is ready to receive data.
2	(BA)	Transmitted Data - This printer-generated signal transmits control information to the user system. The printer can not transmit unless an on condition is present on all the following signals: (1) Request to Send (CA) (2) Clear to Send (CB) (3) Data Set Ready (CC) (4) Data Terminal Ready (CD)
22	(CE)	Ring Indicator - This user-generated signal indicates that a ringing signal is being received by the printer. When this signal is in the on condition, it will activate the Data Terminal Ready line on the first ring. The printer must be powered up, ready, and on line.
* Pins are used for current loop mode.		

6.10.4 Parameter Switches

There are three parameter switch sets in the Serial Interface CCA, with functions as shown in figure 6-3.

6.10.5 Word Format

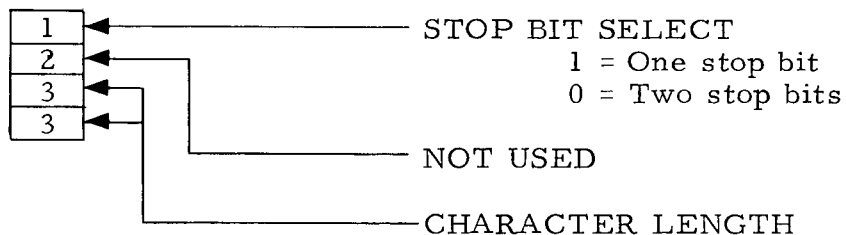
Figure 6-4 shows the word format for the "carriage return" sample character, OD_H . Note that data is transmitted in low-true form.

NOTE

Parity enable and odd/even parity for the Serial Interface CCA are configured by the use of jumpers in the Option Header.

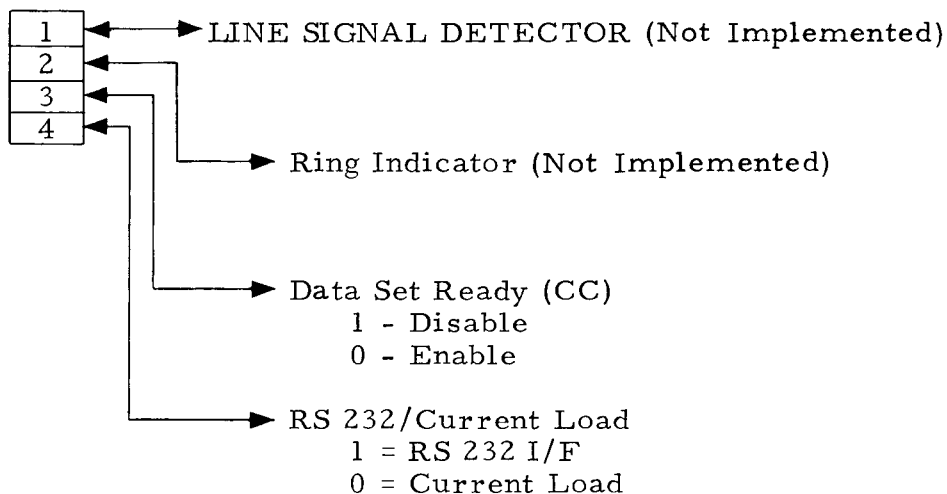
OPTIONS

SW 1



	5 BITS	6 BITS	7 BITS	8 BITS
POS 3	1	1	0	0
POS 4	1	0	1	0

SW 2

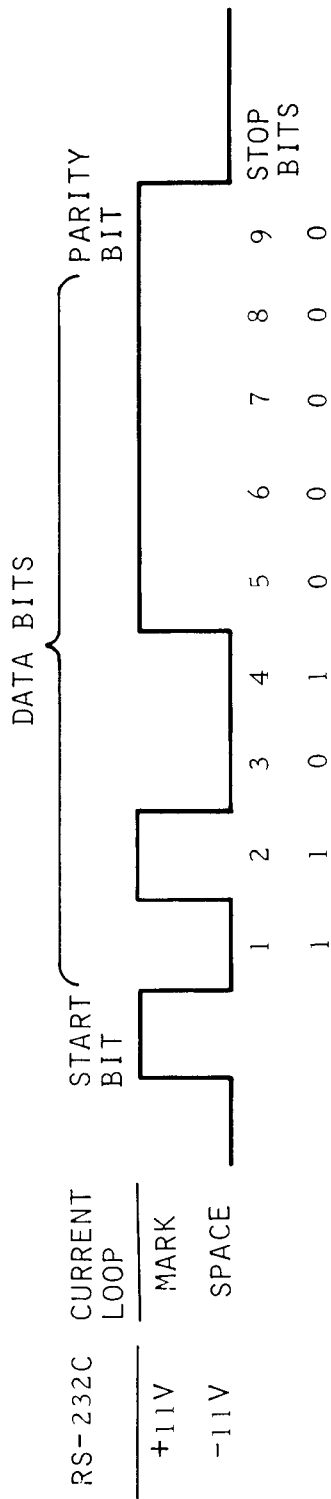


SW 3

BAUD RATE

	110	150	300	600	1200	2400	4800	9600
1	0	0	1	0	0	0	0	0
2	0	1	0	0	1	0	1	0
3	1	0	0	0	1	1	0	0
4	1	1	1	1	0	0	0	0

Figure 6-3. Parameter Switch Settings



NOTE: SAMPLE CHARACTER CR = ODH
ODD PARITY, LOW-TRUE LOGIC

245123 601

Figure 6-4. Serial Interface, Typical Word Format

OPTIONS

6.11 AUTOMATIC LINE FEED

When implemented, this option allows a line feed to occur upon detection of a carriage return code at the interface. A line feed code will also cause a line advance. Implementation of this option requires the use of the OPTION HEADER.

6.12 PRINTER STATUS DISPLAY

This option provides a two-digit display mounted on the Auxiliary Control Panel which indicates which major printer function was being performed and which faults occurred when the printer malfunctioned. This feature enables the operator to quickly identify the nature of a fault and determine if it can be corrected locally. Numeric display definitions are given in section VII of this manual.

6.13 ELAPSED TIME METERS

This option provides two elapsed time meters which enable the user to measure both "power on" and "print time" within $\pm 10\%$ accuracy.

6.14 REAR FORMS LOADING

The printer may be optionally configured for rear forms loading. The standard front and bottom forms loading capability will not be affected.

6.15 PEDESTAL

A pedestal is available for those applications requiring a floor-mounted printer. It is shipped separately from the printer in disassembled state to reduce shipping costs and storage space requirements. A shelf is attached to the rear of the pedestal providing for passive stacking of paper as it exits from the printer. Refer to section II for pedestal assembly and printer-to-pedestal mounting procedures.

6.16 PAPER RECEPTACLE

The paper receptacle, which attaches to the rear of the printer and is detachable, provides for passive stacking of paper that has exited the printer. This option is designed for use with those printers operating on table tops and other flat surfaces. Upon attachment to the printer, the receptacle is free-standing and requires no additional support. Maximum stack height of the paper is 7 inches (177 mm). A 16" x 14" (406 mm x 356 mm) form is the largest that can be stacked in the receptacle.

6.17 GROUND ISOLATION

The standard printer is shipped with logic and frame grounds interconnected. If ground isolation is desired, it may be accomplished by removing a jumper in the power supply. Refer to the power distribution and wiring diagram in section IX.

6.18 SEVEN BIT ONLY INTERFACE

This option allows the printer to operate with a controller which is capable of providing only seven data bits rather than eight bits as required in the standard interface. When operating with this option, the character set is limited to 96 characters. Implementation of this option requires the OPTION HEADER. Refer to section III for installation instructions.

SECTION VII

TROUBLESHOOTING

7.1 INTRODUCTION

This section contains information necessary to troubleshoot the printer. Troubleshooting is organized at two levels: the printer system level, and the power distribution level.

7.2 PRINTER SYSTEM TROUBLESHOOTING

The printer system troubleshooting guide, table 7-1, lists the optional status display indicators, their definitions, probable causes and remedies. For assistance in circuit board isolation or assembly troubleshooting, refer to table 7-2, the Fault Probability Guide.

7.2.1 System Fault Analysis

This paragraph provides a description of the status codes listed in table 7-1 and an explanation of the way in which each is evolved. Some of the status displays are not error conditions but merely indicate which print system routine is being performed or was being performed when a fault condition occurred.

Fault isolation involving the Interface CCA assumes that the printer is configured with a standard DPC Short-Line Parallel Interface CCA. If the printer is configured with any of the optional Interface CCAs, refer to the applicable logic diagram in section IX, volume II of this manual to find the equivalent logic circuit and pin connections.

a. Switch Check Routine/Ready - Status Display 00

This routine monitors the control panel switches and various fault condition switches, which include the following:

1. Form Length Switch
2. On Line Switch
3. Top of Form Switch
4. Paper Step Switch
5. Vertical Pitch Switch
6. Alarm/Clear Switch
7. Bail Open Switch
8. Cover Open Switch (Optional)
9. TCVFU Switch (Optional)

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b. Out of Paper - Status Display 01

The paper low interlock switch S5 provides a means of detecting when the printer runs out of paper. When paper is installed in the printer, this switch is held in an energized position. The loss of paper from in front of this switch allows the switch contacts to open, thereby supplying a high level at connector P2-41 of the Processor CCA (see figure 9-15, sheet 7). This high input is provided to input port driver U21-11. When U21-1 is enabled, U21-9 is then set, gating DBUS 5 through I/O port transceiver U15 (sheet 5) to bus driver U25 and Processor Chip U1 (sheet 2).

Under program control, the data bits are examined and determined to be in a paper low condition. The shuttle is parked if it had been moving, and the ribbon drive motor and the ON LINE indicator are turned off. The ALARM indicator is turned on, and the system data bus lines from bi-directional driver U20 on the Processor CCA (see figure 9-15, sheet 5) are sent to the status display indicators where a status code of 01 is displayed.

Installation of paper and pressing the ALARM/CLEAR switch will restore the printer to normal operation.

c. Cover Open - Status Display 03

An optional cover open switch is provided on the printer. If the printer cover is opened while printing, the printer will go to an off-line condition, and the print head will be parked at the end of the present print cycle.

With the cover closed, the cover open switch is held in an energized position. Opening the cover allows its contacts to close, supplying a low level at connector P2-43 of the Processor CCA (see figure 9-15, sheet 7). This low level is placed on input port driver U21-13. When U21-1 is enabled, U21-7 is set, gating DBUS 6 low through I/O port transceiver U15 (sheet 5) to bi-directional driver U25 and Processor Chip U1 (sheet 2).

Under program control, the data bits are tested and found to be in a cover-open condition. The shuttle is parked, and the ribbon drive motor and ON LINE indicator are turned off. Pressing the ON LINE switch while the cover is open will light the ALARM indicator. The system data bus lines from the bi-directional driver U20 on the Processor CCA (see figure 9-15, sheet 5) are then sent to the status display indicators on the control panel, where a status code of 03 will be displayed.

Closing the cover and pressing the CLEAR switch will clear the fault condition and restore the printer to normal operation.

d. Bail Open - Status Display 04

The platen gap lever, if left open or if opened during printer operation, will take the printer off line and prevent printer operation due to a bail open condition. With the platen closed, the bail switch is in a de-energized position. Opening the platen supplies a high level at connector P2-45 of the Processor CCA (see figure 9-15, sheet 7). This high level is placed on input port

TABLE 7-1. PRINTER SYSTEM TROUBLESHOOTING GUIDE

Status Display	Definition	Probable Cause	Remedy
00	Switch check routine/ready	Undefined	Replace or repair CCA as required. Install paper. Close cover or adjust or replace switch. Close platen gap lever or adjust or replace switch. Install tape, correct jam condition. Validate tape. Install valid tape. Limit tape to a maximum of 254 lines. Install character generator ROM. Send stop code after even data byte, limit data bytes to 255 or less, validate input data.
01	Out of paper		
03	Cover open	No paper Cover not closed or switch defective Platen lever open or switch defective No tape, broken tape or jammed tape during TCVFU operation Unable to read and verify tape successfully No channel 1 hole punched in tape Tape too long Character Generator ROM not installed Stop code after ODD number of bytes, too many data bytes, parity error	Replace or repair CCA as required. Restart load operation.
04	Bail open		
09	No tape - tape reader jammed	Undefined	Replace or repair CCA as required. Restart load operation.
10	TCVFU Read/Compare		
12	No TOP OF FORM on tape	Load operation not completed within allowed time Undefined No shuttle motion within specified time	Replace or repair CCA as required. Mechanical interference, broken belt, defective motor. Install correct interface card. Replace or repair Processor CCA. Place self test switch to OFF position
13	Channel not found		
20	No Character Generator	Interface card not inserted Clear F/F failed to reset Self test switch in test position	Replace or repair Processor CCA Replace or repair Processor CCA; repair mechanical problem
26	DAVFU fault		
40	Print right normal	Shuttle pitch is wrong for line of data Shuttle has passed the point where printing should begin	
41	Print left normal		
42	Print right compressed	Denotes Self Test routine is being performed with I/F card installed	
43	Print left compressed		
44	Print right expanded		
45	Print left expanded		
48	TCVFU load routine		
50	Position seek		
52	Shuttle park		
55	Form feed routine		
56	6 Lines Per Inch routine		
57	8 Lines Per Inch routine		
58	Step routine		
62	Buffer not full		
63	Buffer interrogate		
64	No shuttle motion		
65	No interface card		
66	No clear to alarm C/R flip-flop		
67	Self Test		
68	Shuttle pitch and format switch do not compare		
69	Character column counter incorrect - mechanical failure		
70	Self Test with I/F		

TROUBLESHOOTING

driver U21-2. When U21-1 is enabled, U21-18 (data Bus 4) is gated to the I/O port transceiver U15 (sheet 2) and driver U25 and processor chip U1 (sheet 2).

Under program control, the data bits are tested and found to be in a bail-open condition. If the printer is powered up with the bail open, the ALARM light will be lit and a status code of 04 will be displayed. If the bail is opened while the printer is operating, the shuttle is parked, and the ribbon drive motor and ON LINE indicator are turned off. Pressing the ON LINE switch with the bail open will turn on the ALARM light and gate the system data bus lines from bi-directional driver U20 on the Processor CCA (see figure 9-15, sheet 5) to the status display indicators. A status code of 04 will then be displayed.

Closing the bail and pressing the CLEAR switch will clear the the fault condition and restore the printer to normal operation.

e. No Tape - Tape Reader Jam - Status Display 09

One of the options available to the printer system is the tape controlled vertical format unit (TCVFU). This option sets up the correct format control for the printer.

When a TCVFU load operation is desired, the printer must be in the off line mode, and the switch located on the tape reader unit must be manually pressed. Pressing the tape reader switch develops the signal TRRQ (Tape Reader Request) on the Interface CCA (see figure 9-11, sheet 4). Signal TRRQ on J12-20 is sent to driver U25-15 which, when enabled at U25-1, gates U25-5 (DB7) onto the interface data bus. Under program control, this sequence is examined and determined to be a call for a TCVFU load routine.

Signal ENRDR* (Enable Reader) at P2-48 (see figure 9-11, sheet 4) is developed from the Processor CCA to enable the TCVFU drive motor. Movement of the tape reader develops a tape reader strobe pulse. This strobe pulse is developed from the tape sprocket feed holes and arrives at connector J12-28 on the Interface CCA as signal CH13 (Tape Channel 13). The input is sent to driver U25-17, and when enabled by CS7* at U25-1, it outputs U25-3 (DB8) onto the interface data bus.

Under program control, this data bus is examined, and if no strobe pulse occurs at DB8, it is determined that either no tape has been installed, or a tape reader jam has occurred. The TCVFU drive motor then turns off, the ALARM indicator illuminates, and a status code of 09 is displayed.

Correction of the problem that caused the error condition, pressing the CLEAR switch and repeating the load operation will restore normal printer operation.

f. TCVFU Read/Compare - Status Display 10

If the TCVFU fails to read and compare for two consecutive times during the five read operations allowed, tape operation will halt and a status code of 10 will be displayed.

During the TCVFU load routine, data read from the TCVFU tape is input to the VFU memory. A programmed count of five allows the user to read the tape and compare it with the VFU memory for a maximum of five times. Each time the tape is read and no comparison occurs, the VFU memory is changed to reflect the new data, and the programmed count of five is decremented. If the VFU memory does not match the tape within two consecutive readings and within the five tries allowed, a fault condition has occurred. The TCVFU drive motor then turns off, the ALARM indicator will be illuminated, and a status code of 10 will be displayed.

Correction of the cause of the error condition, pressing the CLEAR switch, and restarting the tape read operation will restore normal printer operation.

g. No Top of Form - Status Display 12

The TCVFU tape may be punched with any combination of twelve channels, with the exception that channel 1 represents the top of form, and channel 12 represents the bottom of form. During the initial tape read operation, a check is made to ensure that the top of form hole punched in channel 1 is correctly punched in the tape.

The output of channel 1 (CH1) arrives at J12-34 of the DPC Parallel Interface CCA (see figure 9-11, sheet 4). The CH1 output from the tape reader goes low when that channel is sensed. If after reading the tape CH1 has not been sensed, driver U25-18 (DB1), the interface bus line, will not be activated. Under program control, this sequence will be checked and the TCVFU drive motor will be turned off, the ALARM indicator will be illuminated, and a status code of 12 will be displayed.

Inserting a correctly punched tape, pressing the CLEAR switch, and restarting the tape load operation will restore normal printer operation.

h. Channel Not Found - Status Display 13

Failure to find the Top of Form within 254 lines after it has appeared the first time will cause a status code of 13 to be displayed. After each line of TCVFU data is read, a check is made to determine if a TOF Code, Channel 1, is present. The output of Channel 1 arrives at J12-34 of the DPC Parallel Interface (see figure 9-11, sheet 4). Signal CH1 from the tape reader goes low when that channel is sensed. Failure of driver U25-18 (DB1), the interface data bus line, to be activated before a preprogrammed count of 254 has expired, will inform the printer system that the tape is too long. The TCVFU drive motor will be turned off, the ALARM indicator will be illuminated, and a status code of 13 will be displayed.

Insertion of a tape of correct length, pressing the CLEAR switch, and restarting the tape load operation will restore normal printer operation.

TROUBLESHOOTING

i. No Character Generator - Status Display 20

A program check is performed to ascertain whether or not the character generator ROM, MEM5, on the Processor CCA (see figure 9-15, sheet 4) is installed. Under program control, a specified ROM location containing all zeros is read and compared. Failure of the ROM to be installed will bring the ROM output to a high level. Comparison of the specified ROM location when the PROM has not been installed will cause a fault condition. Printer operation will stop, the ALARM indicator will be illuminated, and a status code of 20 will be displayed.

Installation of a character generator ROM, pressing the CLEAR switch, and restarting the print operation will restore normal printer operation.

j. DAVFU Fault - Status Display 26

The Direct Access Vertical Unit (DAVFU) allows format information to be loaded directly from the user system into memory without the need for a tape loop.

In the DPC Parallel interface, DAVFU memory is loaded by sending a start code (156 octal) with the Paper Instruction (P.I.) high. Loading is halted by sending a stop code (157 octal) with the P.I. high.

When loading DAVFU memory, the first data byte received represents tape channels 1 through 6, and the second data byte represents channels 7 through 12. Thus, the data bytes must be loaded in pairs to prevent formatting errors. The maximum number of data byte pairs read into memory is 255, not including start and stop codes.

During the loading of the DAVFU memory, the following errors will be detected: (1) receipt of a stop code after an odd number of data bytes, (2) sending more data bytes than allowed, (3) parity error detection during the loading of DAVFU data.

k. Receipt of a Stop Code After An Odd Number of Data Bytes

The receipt of a DAVFU start code raises DEMAND, which clocks address counter U36-1 (see figure 9-11, sheet 3) of the DPC Parallel Interface. U36-3, AC BIT1, will therefore be high on each even DAVFU data byte. AC BIT1 is gated to NAND gate U41-13 (sheet 7) where it is ANDed with DA STOP CODE at U41-12. If the stop code is high at the same time as AC BIT1, which denotes an odd DAVFU data byte, U41-11 will go low to U41-4. U41-6 goes high to D-type flip flop U13-12, which when set by clock FF2 at U13-11, outputs a low signal at U13-8 called DAVFU FAULT*, denoting an error condition.

1. Sending More Data Bytes Than Allowed - Each DEMAND pulse clocks address counter U36 (see figure 9-11, sheet 3) of the DPC Parallel Interface. The address counter bit outputs, ACBIT1 through ACBIT 9, input to the Top Count PROM, MEM3, (sheet 7). When MEM3-11 (PL/DA TOP CNT) goes high, signifying that the maximum amount of DAVFU data capable of being

loaded has been reached and no stop code has been received, NAND gate U41-8 will go low. U41-6 goes high to flip-flop U13-12 which, when set by clock FF2 at U13-11, outputs a low signal at U13-8 called DAVFU FAULT*, denoting an error condition.

2. Parity Error - A parity error will also be detected during loading of the DAVFU memory. If a parity error occurs during the transmission of DAVFU data, flip flop U2-8 of the DPC Parallel Interface will go low (see figure 9-11, sheet 2). This low condition is sent to flip flop U13-10 (sheet 7), setting it. U13-8 goes low, outputting signal DAVFU FAULT*, denoting an error condition. A DAVFU fault condition will halt the loading of DAVFU data and turn on the ALARM indicator.

Pressing the ALARM/CLEAR switch and restarting the load procedure will restore normal printer operation.

1. Print Right Normal - Status Display 40

This routine defines the shuttle servo motor as moving at a right pitch and not in an expanded or compressed print mode. Normal print mode is 10 characters per inch.

m. Print Left Normal - Status Display 41

This routine defines the shuttle servo motor as moving at a left pitch and not in an expanded or compressed print mode. Normal print mode is 10 characters per inch.

n. Print Right Compressed - Status Display 42

This routine defines the shuttle servo motor as moving at a right pitch and in a compressed print mode. Compressed print is 16 characters per inch.

o. Print Left Compressed - Status Display 43

This routine defines the shuttle servo motor as moving at a left pitch and in a compressed print code. Compressed print is 16 characters per inch.

p. Print Right Expanded - Status Display 44

This routine will print from left to right at 5 characters per inch.

q. Print Left Expanded - Status Display 45

This routine will print from right to left at 5 characters per inch.

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r. TCVFU Load Routine - Status Display 48

The TCVFU tape is read, and the data is stored in the VFU memory. If the tape read does not compare with the VFU memory within a maximum of five times, a fault condition will occur. A VFU-loaded signal to the user, except in the case of the DPC Centronics-Compatible Interface CCA, will also be set or reset.

s. Position Seek - Status Display 50

This routine is used to position the print head in the quickest way to print a new line.

t. Shuttle Park - Status Display 52

This routine is used to reinitialize the shuttle location with respect to the column one sensor, and also to park the shuttle. The shuttle is parked approximately seven character columns to the right of the sensor.

u. Initialize Routine - Status Display 54

This routine initializes the paper feed motor, various flags, registers, ports; parks the shuttle; checks for an Interface CCA; and shuts off the display indicator lamp.

v. Form Feed Routine - Status Display 55

This routine slews paper the required distance as indicated by the Forms Length Counter (FLC) plus the number of lines required for Perforation Skipover (SKPLNS).

w. Six Lines Per Inch Routine - Status Display 56

This routine moves the paper feed motor through four phases, resulting in the moving of paper one line feed at six lines per inch.

x. Eight Lines Per Inch Routine - Status Display 57

This routine moves the paper feed motor through three phases, resulting in the moving of paper one line feed at eight lines per inch.

y. Step Routine - Status Display 58

This routine moves the paper feed motor one phase. The phase that is on when the routine is entered will be turned off, and the next phase will be turned on.

z. Buffer Not Full - Status Display 62

A LOAD BUFFER signal is sent to the Interface CCA to initiate a load operation. A 30 ms delay is allowed to complete the load operation. If the BUFFER FULL signal signifying that the load operation is complete does not arrive before the 30 ms load delay times out, the shuttle will be parked.

U12-6, BUFFER FULL F/F on the DPC Parallel Interface CCA (see figure 9-11, sheet 5), will be low to denote a BUFFER FULL signal. This signal is sent to Line Driver U39-2 (sheet 9). When enabled by U39-1 (CS6*), U39-18, DBUF 1 will be output high to the system data bus.

Under program control, the system data bus is checked, and if signal BUFFER FULL has not arrived within the allotted 30 ms allowed from the start of the load operation, the shuttle will be parked, and a status code of 62 will be displayed.

aa. Buffer Interrogate - Status Display 63

This routine is used to interrogate the buffer for the terminating code, DAVFU format information, illegal characters, underline codes, and the first and last printable characters.

bb. No Shuttle Motion - Status Display 64

A means of detecting the absence of shuttle motion is provided in the printer system by sensing the encoder pulses. The encoder logic is comprised of two D-type flip-flops, U30-5 and U30-9 on the Processor CCA (see figure 9-15, sheet 6). U30-9 will be output when the shuttle is moving to the right, and U30-5 will be output when the shuttle is moving to the left.

A programmed time delay of one second is provided during which time a check is made to see if shuttle motion has occurred.

Flip-flop encoder outputs U30-9 and U30-5 are gated by U43-10 (ENC INT REQ)* to the 8080 CPU chip as an interrupt, and also to input port U21-15 (sheet 7). When U21-1 is enabled, U21-5 (DBUS 7) will be output high or low, depending on the status of the encoder signal at U21-15. This output is sent to the Processor CCA, where it is checked under program control. If encoder pulses fail to occur within the allotted time, a fault condition has occurred. The shuttle and ribbon drive motors will be turned off, READY and ON LINE will go low, and a status code of 64 will be displayed.

Pressing the CLEAR switch will reinitialize the printer system.

cc. No Interface CCA - Status Display 65

A means of verifying that the Interface CCA is installed in the printer has been provided. During the power up and initializing procedures, a check is made to verify installation of an Interface CCA. Data of all zeros is written into location zero of the Interface RAM. This data is then read back. If it compares, the Interface RAM flag is set, denoting that the Interface CCA is in the printer. If the data read back does not compare, the Interface RAM flag is reset to inform the Processor CCA of the absence of the Interface CCA.

If the printer is in the self test mode, the Interface CCA is not needed, and printing will continue. If not in the self test mode, a check of the Interface RAM flag is made, and if it is in the reset condition, printer operation

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is discontinued, the ALARM indicator is illuminated, and the status code of 65 will be displayed.

Installation of an Interface CCA and pressing the CLEAR switch will restore the printer to normal operation.

dd. No Clear to Alarm C/R Flip Flop - Status Display 66

During power up, a software reset signal is provided to initialize the printer circuitry. A check is then made on the CLEAR flip flop to be certain that it has been reset. On the Processor CCA (see figure 9-15, sheet 6), CLEAR flip-flop output U28-9 will be low when in a reset condition. This output is sent to input port driver U19-11 (sheet 7). When U19-1 (CS13*) is enabled, U19-9 (DB5) will be low if the CLEAR flip-flop is reset, or high if the CLEAR flip-flop is not reset. This data is sent to the CPU and Control section of the Processor CCA, where it is checked under program control. If the CLEAR flip flop is found not to be reset, all motors are turned off, a status code of 66 will be displayed, and printer operation will come to a halt.

Correcting the condition that caused the failure and powering the printer down, and then up, will clear the fault condition.

ee. Self Test - Status Display 67

This routine sets up the self test buffer, generating a fixed pattern printout. One hundred thirty two characters and a line feed are loaded into the buffer. Both status displays are checked by counting from 0 to F. Whether or not an Interface CCA is installed in the printer is also checked. If no Interface CCA is installed, the Processor CCA RAM is selected as the print buffer, starting the printout with a small "a". If the Interface CCA is installed, the Interface CCA RAM is selected as the print buffer, starting the printout with a capital "A".

ff. Shuttle Pitch Wrong for Line of Data - Status Display 68

During the executive routine portion of the program, a comparison of shuttle pitch and horizontal format switch setting is made to be certain that the shuttle is correctly set for the line of data to be printed. If the switch is found to be incorrectly set, the shuttle is parked, a status code of 68 is displayed, and the program is reinitialized.

gg. Shuttle Has Passed Point Where Printing Should Begin - Status Display 69

During the executive routine portion of the program, the direction in which the shuttle is moving is checked, and a check is then made to see if printing is to be normal, compressed, or expanded. The character column counter, which contains the correct character column position of the print head, is then checked to make certain that it is correct for the type of printing to be done. If it is not correct, a status code of 69 will be displayed and the routine will be restarted.

hh. Self Test With Interface - Status Display 70

This display denotes that the self test routine is being performed with the Interface RAM being used as the print buffer. The printout will start off with a capital "A".

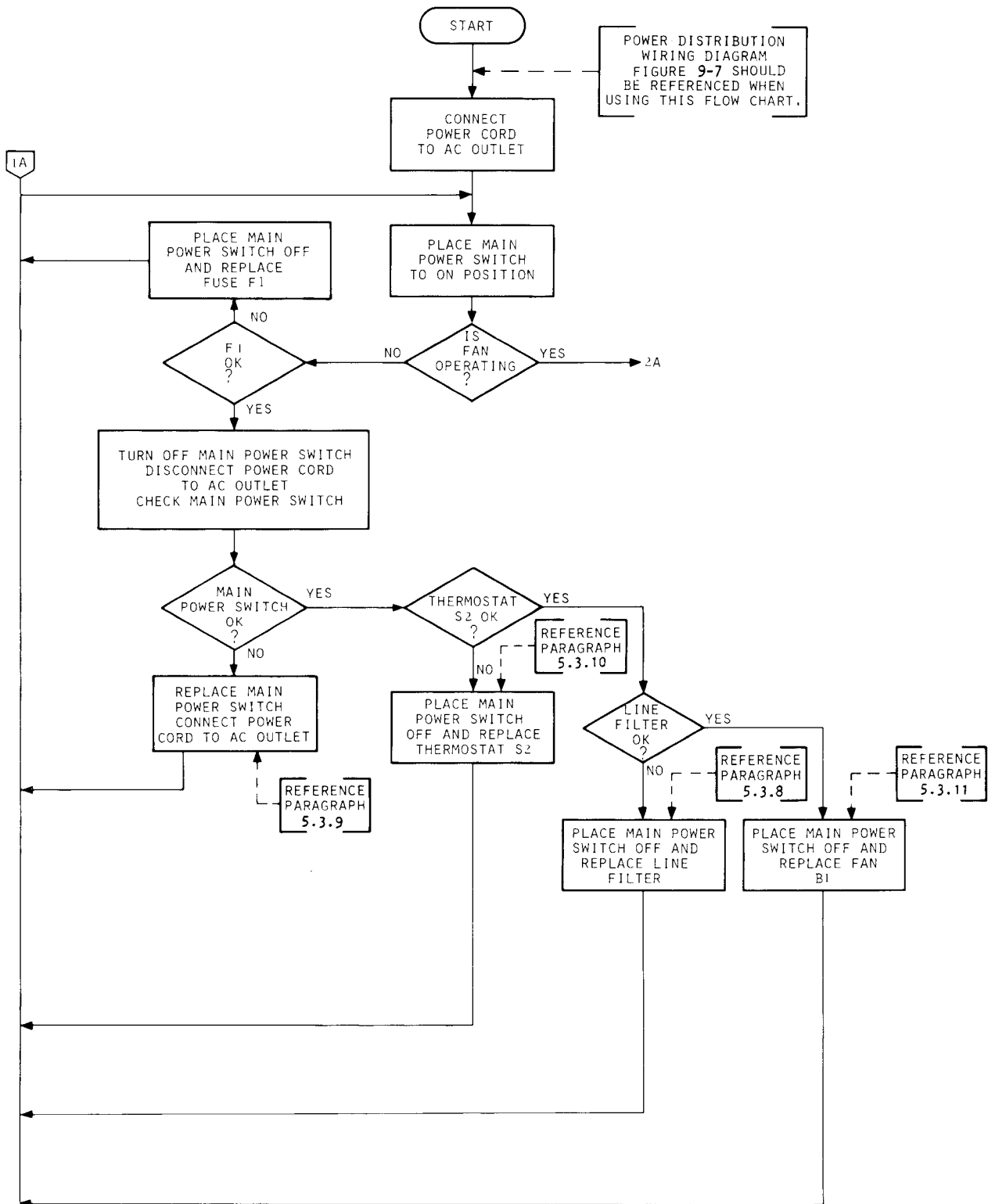
7.3 POWER DISTRIBUTION

Figure 7-1 is a troubleshooting flow chart of the power supply and other components related to power generation and distribution. Figure 9-6 in volume II is a power distribution diagram. Use figures 9-7 or 9-8, and 9-6 in conjunction with figure 7-1 to isolate any faulty power components.

7.4 PRINTER SYSTEM TROUBLESHOOTING

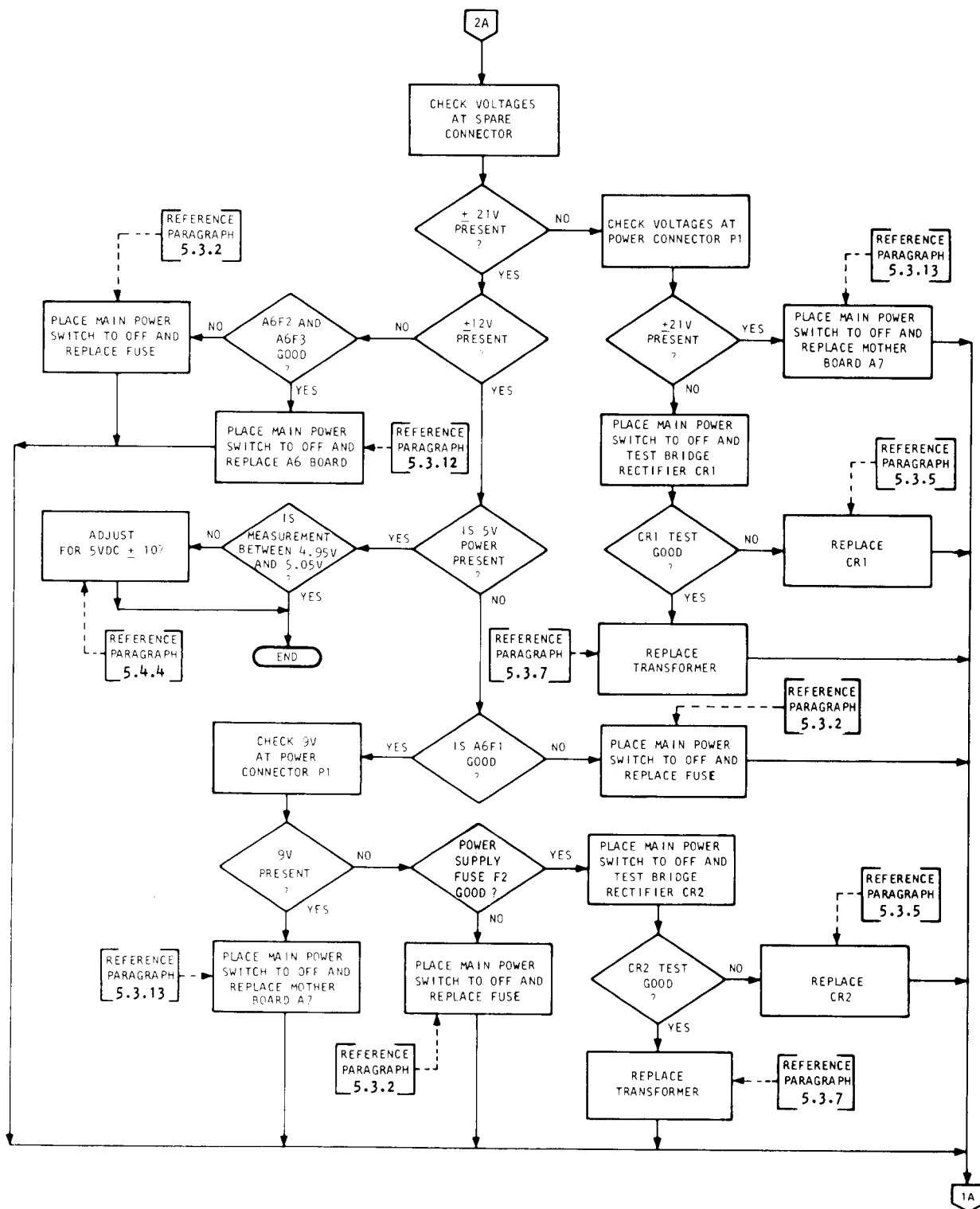
Table 7-2 lists some typical malfunctions that may occur in the printer, and gives one or more possible causes for each malfunction and the recommended maintenance actions for each. Possible causes of malfunction are listed in a descending order of probability. The last item to be tested in any logic-related malfunction is Mother Board CCA A7, not itemized in table 7-2.

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Figure 7-1A. Power Distribution Troubleshooting Flow Chart



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Figure 7-1B. Power Distribution Troubleshooting Flow Chart

TABLE 7-2. FAULT PROBABILITY GUIDE

Malfunction Symptom	Probable Cause	Maintenance Action	Ref. Para.
Print density not uniform.	a. Wire Driver ON/OFF period misadjusted. b. Forms thickness setting does not match form. c. Wire Driver current misadjusted. d. Wire Driver CCA A5 defective. e. Processor CCA A3 defective.	Adjust Change forms thickness control setting to match form. Adjust. Replace Wire Driver CCA A5. Replace Processor CCA A3.	5.4.1 5.4.2 5.3.12 5.3.12
Print line is skewed.	Tractor phasing incorrect.	Correct Tractor phasing.	5.3.17
Print rate too slow.	a. Shuttle speed on Motor Driver CCA A4 misadjusted. b. Excessive shuttle friction.	Adjust shuttle speed. Clean guide bar with isopropyl or denatured alcohol, or Loctite safety solvent.	5.4.3 --
Random print errors or printer does not respond to user system input.	a. Interface cable not connected properly. b. Interface cable defective. c. Defective interface CCA A2. d. Serial Interface CCA only: interface parameter switches incorrectly set. e. Processor CCA A3 defective.	Ensure proper interface cable connection Replace interface cable. Replace interface CCA A2. Set interface parameter switches per figure 6-3.	-- -- 5.3.12 --
Dots missing from printer character.	a. Worn ribbon. b. FORMS THICKNESS control setting does not match forms thickness. c. Wire driver ON/OFF period misadjusted. d. Any one of fuses A4F1 through A5F1 on Wire Driver CCA defective. e. Wire Driver CCA A5 defective. f. Print head defective. g. Processor CCA A3 defective. h. Defective print head flex cable.	Replace Processor CCA A3. Replace ribbon cartridge. Place forms thickness control to proper setting. Adjust Replace defective fuse. Replace Wire Driver CCA A5. Replace print head. Replace Processor CCA A3. Replace print head flex cable assembly (W3).	5.3.12 3.3.2 3.3.1 5.4.1 5.3.2 5.3.12 3.3.3 5.3.12 5.3.21
Margin alignment inconsistent, or non-uniform.	a. Loose shuttle servo belt. b. Loose pulley on shuttle servo motor. c. Column 1 harness loose d. Flange on carriage loose. e. Forms thickness control does not match form thickness f. Processor CCA A3 defective. g. Defective shuttle servo motor.	Tighten shuttle servo belt. Tighten pulley with an Allen head wrench. Adjust column 1 harness. Tighten flange. Place form thickness control to correct setting.	5.4.7 -- 5.4.6 -- 3.3.1
Print head overshoots left or right margin.	a. Column 1 harness misadjusted. b. A4F3 fuse defective (right overshoot). c. A4F4 fuse defective (left overshoot). d. Column 1 harness defective. e. -21 volt power absent (left overshoot). f. +21 volt power absent (right overshoot). g. Shuttle servo motor defective h. Motor Driver CCA A4 defective. i. Processor CCA A3 defective.	Replace CCA A3. Replace shuttle servo motor Readjust column 1 harness. Replace A4F3. Replace A4F4. Replace column 1 harness.	5.3.12 5.3.22 5.4.6 5.3.2 5.3.2 5.3.25 -- --
		Replace shuttle servo motor. Replace Motor Driver CCA A4. Replace Processor CCA A3.	5.3.22 5.3.12 5.3.12

TABLE 7-2. FAULT PROBABILITY GUIDE (Contd)

Malfunction Symptom	Probable Cause	Maintenance Action	Ref. Para.
Paper does not advance when the PAPER STEP switch is pressed.	Printer is in the on line mode? YES NO J10-31 on the control panel goes low when the PAPER STEP switch is pressed. NO YES P2-46 Processor CCA connector goes low when the PAPER STEP switch is pressed? NO YES U21-16 on the Processor CCA goes low when the PAPER STEP switch is pressed? NO YES U16-18 on the Processor CCA is low during the positive going edge of the clock pulse? NO YES P1-17 on the Processor CCA (STEP*) goes low after pressing the PAPER STEP switch? NO YES U8-6 on the Motor Driver CCA (STEP*) goes low after pressing the PAPER STEP switch? NO YES U8-4 on the Motor Driver CCA goes high after pressing the PAPER STEP Switch? NO YES P1-47 on the Motor Driver CCA goes to approximately +21V after pressing the PAPER STEP switch? NO YES P1-18 on the Motor Driver CCA (Phase 1) goes low after initial power on? NO YES	Press the ON LINE switch to go off line. PAPER STEP switch defective. Replace control panel assembly. Defective cable connection from the Control Panel PAPER STEP switch to the Processor CCA. Repair or replace as necessary. Defective I. C. U21. Defective circuitry on the Processor CCA. Repair or replace Processor CCA. Defective I. C. U16 or connection. Defective connection from Motor Driver CCA to the Processor CCA. Defective I. C. U8 or associated circuitry. Defective F1, Q11, Q12, or associated circuitry, or +21V supply voltage. Defective connection from the Motor Driver CCA to the Processor CCA, or the Processor CCA defective.	-- 5. 3. 28 -- 5. 3. 12 5. 3. 12 -- -- 5. 3. 2 5. 3. 12

TABLE 7-2. FAULT PROBABILITY GUIDE (Contd)

Malfunction Symptom	Probable Cause	Maintenance Action	Ref. Para.
When PAPER STEP switch is pressed and released, paper advances continuously.	a. PAPER STEP switch defective. b. Motor Driver CCA A4 defective. c. Processor CCA A3 defective.	Replace Control panel assembly. Replace Motor Driver CCA A4. Replace Processor CCA A3.	5. 3. 28 5. 3. 12 5. 3. 12
Paper does not align to top of form position.	a. Paper improperly loaded. b. 6/8 LPI switch option improperly set. c. FORM LENGTH switch option improperly set. d. Paper feed belt broken. e. TCVFU improperly loaded. f. Tape reader defective. g. VFU tape defective.	Reload Paper. Verify that 6/8 LPI switch is set to correct position. Verify that FORM LENGTH switch setting agrees with forms being used. Replace paper feed belt. Reload TCVFU. Replace tape reader. Replace VFU tape.	3. 3. 1 -- -- 5. 3. 14 3. 3. 4 5. 3. 29 3. 3. 4
ON LINE indicator does not go on after ON LINE switch is pressed; ALARM indicator is on.	a. Printer is out of paper. b. Paper low interlock switch misaligned. c. Platen gap lever in open position, or bail open interlock switch misadjusted or defective. d. Processor CCA defective.	Load paper. Adjust. Close platen gap lever, adjust bail open interlock switch, or replace if defective. Replace Processor CCA A3.	3. 3. 1 5. 4. 5 5. 3. 27
Printer continues printing after paper supply has been exhausted.	Paper low interlock switch misadjusted or defective.	Replace or adjust paper low interlock switch as appropriate.	5. 3. 12
Ribbon is not advancing.	Ribbon cassette improperly installed or defective? YES NO P1-5 on the Motor Driver CCA at +21V? NO YES P1-20 on the Processor CCA (RMTR*) goes low on a print or form feed operation? NO YES P1-20 on the Motor Driver CCA (RM*) goes low on a print or form feed operation? NO YES U13-6 on the Motor Driver CCA goes high on a print or form feed operation? NO YES P1-7 on the Motor Driver CCA (RMNEG) goes low on a print or form feed operation? NO YES	Install or replace as needed. Fuse A4F1 open or +21V supply missing. Replace fuse or repair power supply as needed. Defective Processor CCA A3. Replace. Defective connection between Processor CCA and the Motor Driver CCA A4. Repair. Defective I. C. U13 or associated circuitry. Replace I. C. or repair circuitry as necessary. Defective Q14. Replace. Defective Ribbon Motor. Replace	3. 3. 2 5. 3. 2 5. 3. 12 -- -- 5. 3. 18

TABLE 7-2. FAULT PROBABILITY GUIDE (Contd)

Malfunction Symptom	Probable Cause	Maintenance Action	Ref. Para.
Carriage does not move or moves erratically.	a. Mechanical interference such as paper jam. b. Idler pulley misadjusted. c. Push-on terminals to shuttle servo motor disconnected. d. Shuttle servo belt broken. e. Fuse A4F3 and/or A4F4 on Motor Driver CCA A4 defective. f. Power supply voltage absent g. Motor Driver CCA A4 defective. h. Processor CCA A3 defective.	Remove cause of interference. Adjust Idler Pulley adjustment knob. Connect terminals to shuttle servo motor. Replace Replace fuse(s)	-- 5.3.24 5.3.22 5.3.20 5.3.2
	a. Printer power cord not connected to power source. b. Primary power fuse F1 defective. c. Power switch S1 defective. J10-12 on Control Panel (ON LINE LMP)* is low? YES NO P1-44 on the Processor CCA (ON LINE LMP)* is low? YES NO U27-6 on the Processor CCA (ON LINE IND)* is low? YES NO J10-33 on the Control Panel (ON/OFF LINE)* goes low when the ON LINE switch is pressed: NO YES P2-47 on the Processor CCA (ON/OFF LINE)* goes low when the ON LINE switch is pressed? NO YES U28-5 on the Processor CCA (ON LINE FLOP) is high? NO YES	Connect power cord to power source Replace F1. Replace S1 ON/LINE indicator defective or +20V supply to indicator lamp is missing. Replace lamp or check power supply. Defective connection between Processor CCA and Control Panel. Repair. I. C. U27 defective. Replace. Defective switch assembly. Replace. Defective connection between the Processor CCA and the Control Panel. Repair. Replace Processor CCA A3. I. C. U28 or associated circuitry defective. Replace. Processor CCA A3 defective. Replace.	-- 5.3.12 5.3.12 -- 5.3.2 5.3.9 5.3.28 -- 5.3.28 -- 5.3.12 5.3.12

TABLE 7-2. FAULT PROBABILITY GUIDE (Contd)

Malfunction Symptom	Probable Cause	Maintenance Action	Ref. Para
Paper does not advance under any condition	Paper feed belt broken? YES NO	Replace paper feed belt.	5. 3. 14
	Tractor drive assembly binding or defective? YES NO	Repair or replace tractor drive assembly as needed.	5. 3. 16
	P1-17 on the Motor Driver CCA (STEP*) goes low on a paper move command or pressing the PAPER STEP switch or TOP OF FORM switch? NO YES	Defective Processor CCA A3 or bad connection from the Processor CCA A3 to the Motor Driver CCA A4. Repair or replace as needed.	5. 3. 12
	P1-47 on the Motor Driver CCA (STEP*) goes to approximately +21V on a paper move command or pressing the PAPER STEP switch or TOP OF FORM switch? NO YES	Fuse A4F1 open, +21V supply missing, or defective circuitry on the Motor Driver CCA A4. Replace or repair as needed.	5. 3. 12 5. 3. 12
	P1-18 on the Motor Driver CCA (01*) goes low on initial power on? NO YES	Defective Processor CCA A3 or bad connection from the Processor CCA to the Motor Driver CCA A4. Repair or replace as needed.	5. 3. 12
	P1-43 on the Motor Driver CCA (PM01) is at approximately -21V? NO YES	Fuse A4F2 open, -21V supply missing, or defective circuitry on the Motor Driver CCA A4. Replace or repair as needed. Replace the Paper Step Motor.	5. 3. 12 5. 3. 12

TABLE 7-2. FAULT PROBABILITY GUIDE (Contd)

Malfunction Symptom	Probable Cause	Maintenance Action	Ref. Para.
Paper does not advance when the PAPER STEP switch is pressed. (Contd)	U8-10 on the Motor Driver CCA is high? NO YES P1-43 on the Motor Driver CCA (PM1) is at approximately -21V? YES NO	Defective I. C. U8	--
In self test mode, paper does not advance after each line of print (over-print)	Processor CCA A3 defective	Replace the Paper Feed Step Motor. Open fuse F2, associated components, or -21V supply voltage. Replace Processor CCA A3	5.3.15 5.3.2
With printer on line, and interface connected, paper advances incorrect number of lines.	a. Interface CCA A2 defective b. Processor CCA A3 defective	Replace Processor CCA A2 Replace CCA A3	5.3.12 5.3.12
Paper does not advance when TOP OF FORM switch is pressed.	Printer in on line mode? YES NO J10-30 on the control panel goes low when the TOP OF FORM switch is pressed. NO YES P2-42 on Processor CCA connector goes low when TOP OF FORM switch is pressed. NO YES	Press ON LINE switch to go off line. TOP OF FORM switch defective - Replace control panel assembly.	--
			5.3.28
		Defective cable connection from the control panel TOP OF FORM switch to the Processor CCA. Defective Processor CCA. Replace.	--
			5.3.12



SECTION VIII

Section 8 has been deleted.

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SECTION IX

LOGIC DIAGRAMS

9.1 INTRODUCTION

This section is provided primarily as an aid to personnel engaged in maintaining or troubleshooting the printer, and in support of circuit descriptions given in the Theory of Operation section of volume I of this manual. It contains detailed information representing the functional logic used in the printer.

9.2 ORGANIZATION

This section is organized into the following parts:

- a. Logic Symbols
- b. Typical IC Devices
- c. Glossary of Mnemonic Terms
- d. List of Diagrams
- e. Signal Origin/Destination

9.3 LOGIC SYMBOLS

The logic symbols used in the logic diagrams conform to MIL-STD-806B. As such, active low signals are denoted by an overbar. Elsewhere in this manual, such as in text, tables, or in block and flow diagrams, the overbar is replaced by an asterisk (*).

A small circle at the input of a logic element indicates that a relatively low level (0V typical) activates that function. On the other hand, the absence of a small circle indicates that a relatively high level (+5V typical) activates the function. Examples of some common functions of AND and OR symbols, and their equivalent truth tables, are shown in figure 9-1.

9.4 TYPICAL IC DEVICES

In addition to the common AND and OR circuits illustrated in figure 9-1, the printer uses a variety of IC devices for logic implementation. A selected number of the more common IC devices used in the printer are described in the following paragraphs. If more information is needed, consult the applicable data books.

9.4.1 Decoder/Demultiplexer (Figure 9-2)

The 74S138 chip decodes a 3-bit binary input into one of eight mutually exclusive outputs. As shown in figure 9-2, there are three enable inputs and three select inputs. Two of the enable inputs, G2A and G2B, are active low, and G1 is active high. All three select inputs are active high. When enabled, one of the eight data output lines, Y0-Y7, is selectively activated (driven low), based on the binary state of the three select input lines.

In the printer, the 74S138 chip is used mainly as a chip select generator. Also used in the printer but not depicted here is the 74154 chip. This chip is an expanded version of the 74S138, with four select input lines and 16 data output lines.

9.4.2 Octal D-Type Flip-Flop (Figure 9-3)

The 74273 chip contains eight individual D-type flip-flops, with common clock and clear signals. When the clock changes from low to high, each flip-flop assumes a state corresponding to the state of its D input, regardless of the state the flip-flop was in before the clock transition. For example, when the D input of a given flip-flop is high at the clock transition time, that flip-flop will set, with its Q output moving (or staying) to the high state.

In the printer, the 74273 chip is used mainly as a latch for storing individual commands from the Processor CCA to the Interface CCA.

9.4.3 Octal Non-Inverting Tri-State Drivers (Figure 9-4)



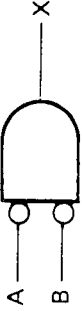





The 74244 chip contains a group of eight non-inverting buffered drivers. The chip is divided into two 4-buffer halves, with each half controlled by a common select signal. Thus, select signal 1G* controls buffers 1A1-1A4/1Y1-1Y4, while select signal 2G* controls buffers 2A1-2A4/2Y1-2Y4. When a select signal is active (low), its four buffers are enabled. When a buffer is enabled, its output, Y, follows its output A. For example, when 1G is low, 1Y1 follows 1A1, 1Y2 follows 1A2, etc. When a select signal is inactive (high), each of its four buffers is driven into the high output impedance state.

In the printer, the 74244 chip is used primarily as a bus driver.

9.4.4 Octal Inverting Tri-State Drivers (Figure 9-5)

The 74240 chip contains a group of eight non-inverting buffered drivers. The chip is divided into two 4-buffer halves, with each half controlled described in paragraph 9.4.3. It differs from the 74244 in that, in addition to buffering, the 74240 also provides logical inversion.

In the printer, the 74240 is used as an inverting bus driver.

LOGIC FUNCTION	AND SYMBOL	OR SYMBOL	INPUTS A B	OUTPUT X
NAND			H H H L L H L L	L H H H
NOR			H H H L L H L L	L L L H
AND			H H H L L H L L	H L L L
OR			H H H L L H L L	H H H L

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Figure 9-1. Common Functions of AND and OR Symbols

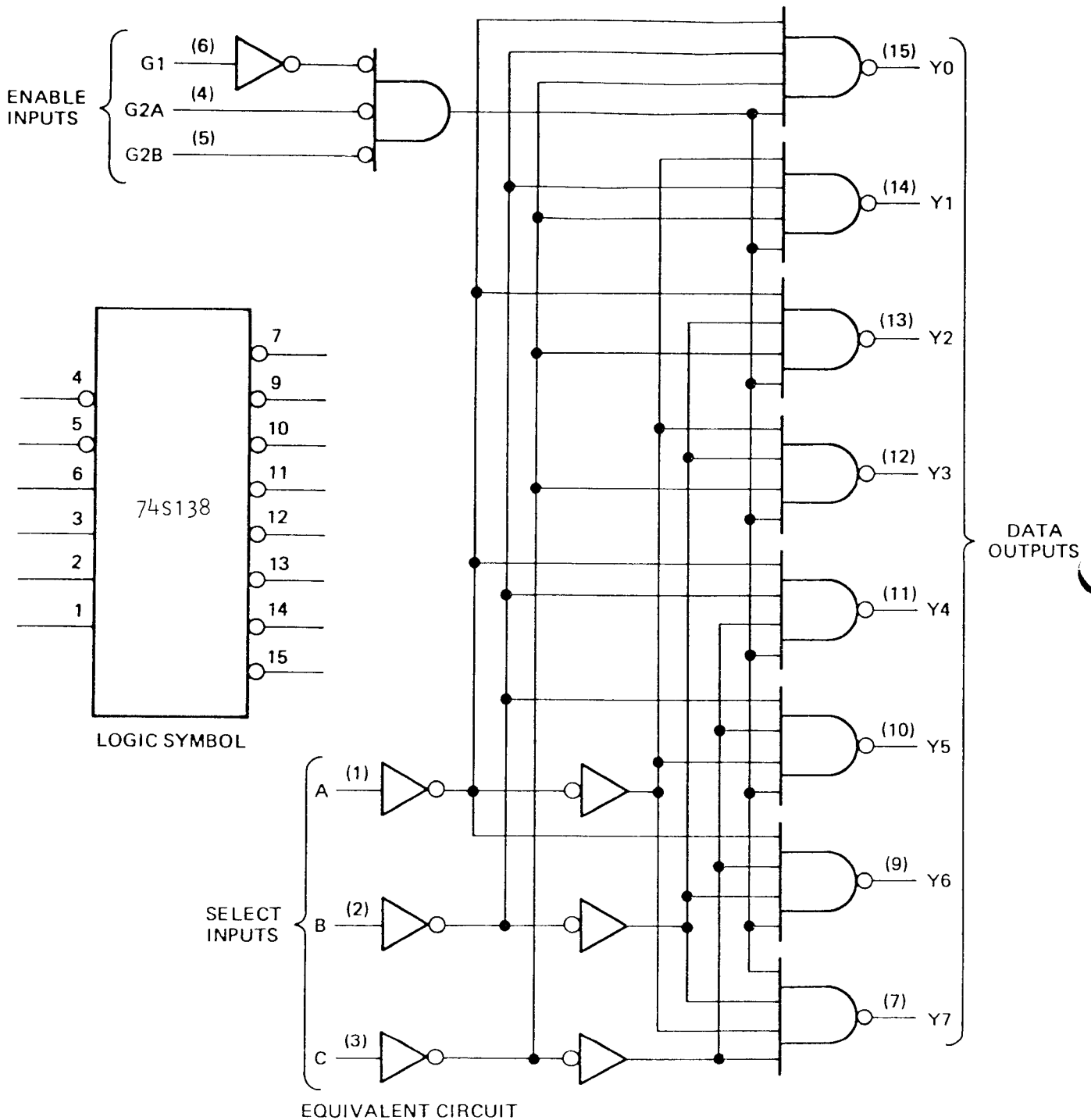


Figure 9-2. Decoder/Demultiplexer Circuit (74138)

FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

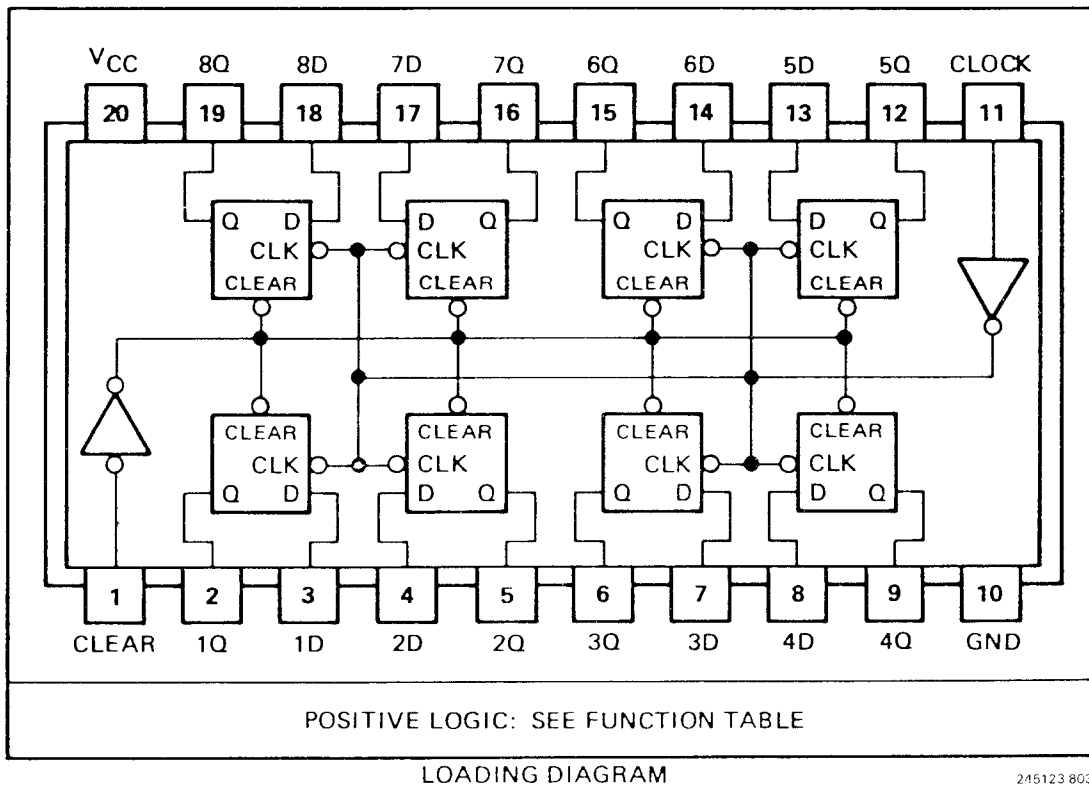
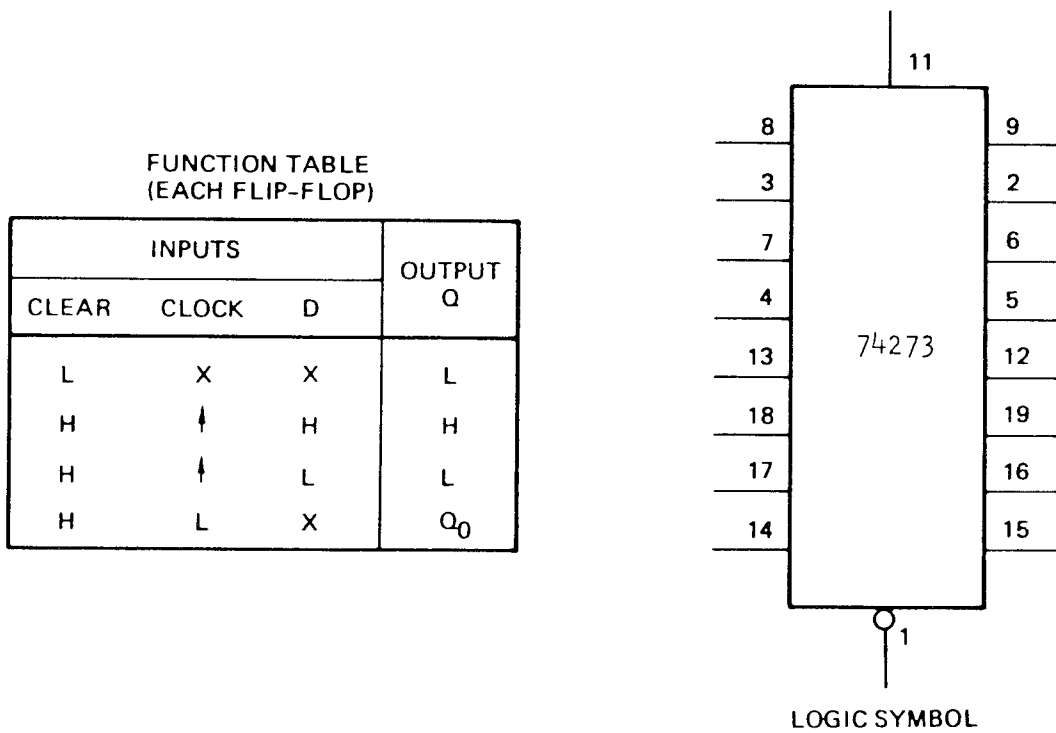
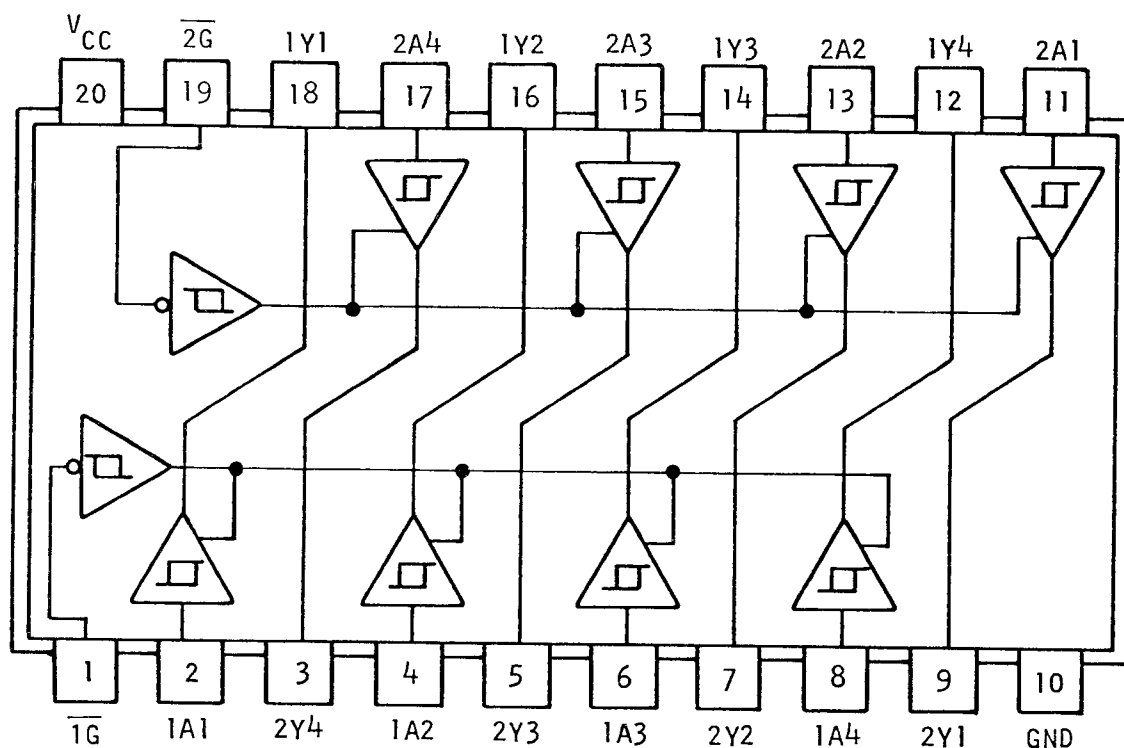


Figure 9-3. Octal D-Type Flip-Flop (74273)



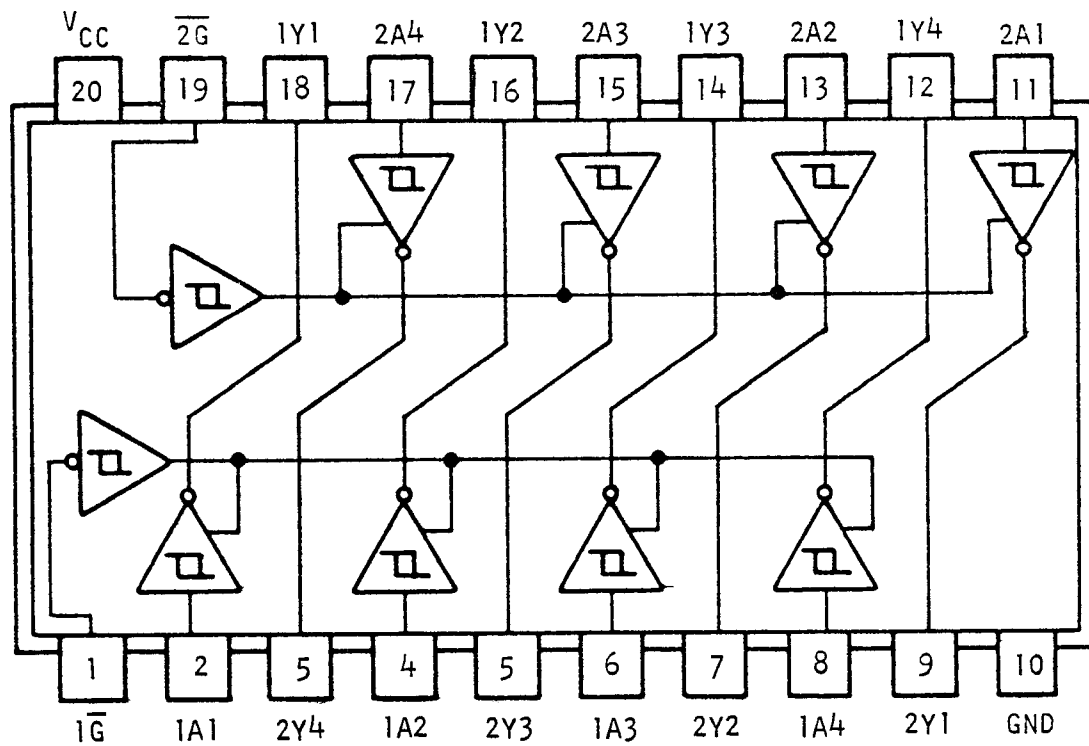
FUNCTION TABLES

1G*	1A1	1Y1
L	L	L
	H	H
	1A2	1Y2
	L	L
	H	H
	1A3	1Y3
	L	L
	H	H
	1A4	1Y4
	L	L
	H	H
H	1Y1 - 1Y4 ALL HIGH IMPEDANCE	

2G*	2A1	2Y1
L	L	L
	H	H
	2A2	2Y2
	L	L
	H	H
	2A3	2Y3
	L	L
	H	H
	2A4	2Y4
	L	L
	H	H
H	2Y1 - 2Y4 ALL HIGH IMPEDANCE	

Figure 9-4. Octal Non-Inverting (74LS244) Tri-State Drivers

LOGIC DIAGRAMS



FUNCTION TABLES

1G*	1A1	1Y1
L	L	H
	H	L
	1A2	1Y2
	L	H
	H	L
	1A3	1Y3
	L	H
	H	L
	1A4	1Y4
	L	H
	H	L
H	1Y1 - 1Y4 ALL HIGH IMPEDANCE	

2G*	2A1	2Y1
L	L	H
	H	L
	2A2	2Y2
	L	H
	H	L
	2A3	2Y3
	L	H
	H	L
	2A4	2Y4
	L	H
	H	L
H	2Y1 - 2Y4 ALL HIGH IMPEDANCE	

Figure 9-5. Octal Inverting (74LS240) Tri-State Drivers

9.5 GLOSSARY OF MNEMONIC TERMS

Table 9-1 lists alphanumerically all logic terms used in the M-200 Printer, defines the meaning of each term, and identifies the source of the term by logic diagram figure number and sheet number. In addition to the standard DPC Parallel Interface CCA, table 9-1 includes all terms found within the optional Serial Interface CCA and DPC Centronics-Compatible Interface CCA; when the same term originates in all the Interface CCAs, all three sources are given. Since the DPC Long-line Parallel Interface CCA is functionally identical to the DPC Short-line Parallel Interface CCA, all references made to the latter also apply to the DPC Long-line Parallel Interface CCA.

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS

Term	Definition	Source	
		Figure	Sheet
ACBIT1-ACBIT9	Address Counter bits of the DPC Parallel Interface CCA.	9-11	3
ACKNLG*	Acknowledge signal supplied by the DPC Centronics-Compatible Interface CCA to the user.	9-14	4
ADR0*-ADR15*	Inverted address bits generated by the Processor CCA	9-15	9
ALARM LMP	Generated by the Processor CCA, this signal turns on the ALARM indicator.	9-15	9
ALCR*	Internal DPC Centronics-Compatible Interface CCA indicating receipt of carriage return code with Auto Line Feed option disabled. When active, causes the Address Counter to skip one count.	9-14	8
A0-A15	Processor CCA address bits	9-15	2
A0-A15	Serial Interface CCA address bits	9-13	2
ATxD+	Positive terminal of active transmit current loop generated by the Serial Interface CCA	9-13	8
ATxD-	Negative counterpart of ATxD+	9-13	8
AUTO LINE*	Option Header signal used to enable the Auto Line Feed option.	9-11	4
		9-13	6
		9-14	5
BCAD*	Internal signal used to clear the Address Counter in the DPC Parallel Interface CCA. Active when the user transmits the BUFFER CLEAR signal.	9-11	3
BOF (Internal)	Status bit supplied by the Processor CCA and decoded in the DPC Parallel Interface CCA. Indicates that the current print line is at the bottom of form.	9-11	9

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
BOF (User)	An amplified version of the BOF (internal) supplied to the user.	9-11	8
BUFFER FULL*	Generated by any Interface CCA and supplied to the Processor CCA as a status bit, this signal indicates completion of the data load cycle.	9-11	5
		9-13	6
		9-14	4
BUSY (Centronics)	DPC Centronics-Compatible Interface status signal supplied to the user. Indicates that the printer is unable to receive data.	9-14	4
BUSY (Serial)	Serial Interface CCA status signal supplied to the user in a RS232C system. Used in conjunction with DTR, it signifies the following: a. BUSY.DTR = Input buffer is 3/4 full. User may continue loading the current line of data and then stop. b. BUSY.DTR* = Printer is unable to receive data.	9-13	8
CBS	Internal current bias supply signal generated within the Wire Driver CCA.	9-17	2
CH1-CH12	Tape Channel signals supplied by the optional TCVFU and routed through any Interface CCA to the Processor CCA.	9-11	4
		9-13	6
		9-14	5
CH13	Line Strobe signal generated by the optional TCVFU and routed through any Interface CCA to the Processor CCA.	9-11	4
		9-13	6
		9-14	5
CK/2	Clock signal used within the DPC Parallel Interface CCA. Equal to 1 mHz, or 1/2 of the OSC2 repetition rate.	9-11	5

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
CLEAR	Derived from a delete code (177 oct) supplied by the user and used to clear the DPC Centronics-Compatible Interface CCA Address Counter.	9-14	6
CLEAR FLOP	Signal generated by the Processor CCA when the CLEAR switch on the Operator Control Panel is pressed. When active, master-clears the printer logic.	9-15	6
CNTDIS*	Signal used to disable DPC Parallel Interface CCA Address Counter upon receipt of a condensed or expanded code.	9-11	6
CODE CONVERTING*	Option Header signal used to enable the code conversion option.	9-11 9-13 9-14	4 6 5
COND	Status bit supplied by the Processor CCA and decoded in the DPC Centronics-Compatible Interface CCA. Active when the 10 CPI switch is set to 16 CPI, and effects condensed printing.	9-14	3
CONDENSED*	Status signal supplied by any Interface CCA to the Processor CCA. Generated when the user transmits a condensed code; also generated in the DPC Centronics-Compatible Interface CCA when the 10 CPI/16 CPI switch is set to 16 CPI.	9-11	6
CONTROL CODE	Internal DPC Centronics-Compatible Interface CCA signal used to terminate the load buffer cycle and generate signal BUFFER FULL. The CONTROL CODE signal is generated under any of the following conditions: a. On receipt of a paper motion control character.	9-14	8

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
CONTROL CODE (Contd)	<ul style="list-style-type: none"> b. On receipt of the DAVFU STOP code. c. When the number of characters received equals the top count. d. With Auto termination enabled, when the number of characters equals 132 or 220 (condensed print). 		
CONTROL CODE*	<p>Internal DPC Parallel Interface CCA signal used to terminate load buffer cycle and generate the BUFFER FULL signal. The CONTROL CODE* signal is generated under any of the following conditions:</p> <ul style="list-style-type: none"> a. On receipt of any paper motion control character. b. On receipt of a DAVFU STOP code. 	9-11	6
CR	Decoded carriage return signal in the DPC Centronics-Compatible Interface CCA.	9-14	8
CRCL*	Generated after a time interval following receipt of CR, is used to clear the BUSY condition in the DPC Centronics-Compatible Interface CCA.	9-14	7
CR/LF	Generated in the DPC Centronics-Compatible Interface CCA on receipt of either a CR or LF paper motion control character.	9-14	8
CS*	Internal DPC Centronics-Compatible Interface CCA signal generated when the Processor CCA intends to read or write into the line buffer.	9-14	9

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
CS1*-CS8*	Family of chip select signals generated in each Interface CCA by decoding the five most significant address bits of the Processor CCA. Not related to CS1*-CS16* of the Processor CCA.	9-11 9-13 9-14	8 3 9
CS1*-CS16*	Family of chip select signals generated from the Processor CCA address bits and used internally within the Processor CCA. Not related to CS1*-CS8* of the Interface CCAs.	9-15	6
CS12*	Logic term generated within the Serial Interface CCA by OR-ing CS1* with CS2*.	9-13	3
D1-D8	Bi-directional Processor CCA data bus, not related to D1-D8 of the Serial Interface CCA.	9-15	2
D1-D8	Main Bi-directional data bus used internally within the Serial Interface CCA. Not related to D1-D8 of the Processor CCA.	9-13	2
DATA01-DATA08	Input data bits supplied by the user to the DPC Parallel Interface CCA.	9-11	6
DATA1-DATA8	Input data bits supplied by the user to the DPC Centronics-Compatible Interface CCA.	9-14	6
DATA STROBE	Strobe signal supplied by the user to the DPC Parallel Interface CCA in response to DEMAND. Validates stability of the input data bits.	9-11	8
DATA STROBE*	Strobe signal supplied by the user to the DPC Centronics-Compatible Interface CCA when the printer is not busy. Validates stability of the input data bits.	9-14	4

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
DAVFU FAULT*	Generated in any Interface CCA and supplied as a status bit (DBUF3) to the Processor CCA under the following conditions. a. When number of DAVFU tape channel characters exceeds 510. b. When number of DAVFU tape channel characters is odd. c. Parity Error (DPC Parallel Interface CCA and Serial Interface CCA only).	9-11	7
		9-13	6
		9-14	6
DAVFU/PRINT*	Generated in any Interface CCA and supplied as a status bit to the Processor CCA (DBUF4), this signal indicates whether the current information supplied by the user is print data (low) or DAVFU data (high).	9-11	3
DAVFU START	Generated in the DPC Parallel Interface CCA and DPC Centronics-Compatible Interface CCA upon receipt of a DAVFU start code.	9-11	6
		9-14	6
DAVFU STOP	Generated in the DPC Parallel Interface CCA and DPC Centronics-Compatible Interface CCA upon receipt of a DAVFU stop code.	9-11	6
		9-14	6
DBI-DB8	Intermediate data bus within any Interface CCA. Channels all data, other than status, between the Interface CCA and the Processor CCA.	9-11	9
		9-13	6
		9-14	3
DBUF1-DBUF8	Inter-CCA bi-directional data bus. Channels all data between the Processor CCA and any Interface CCA and between the Processor CCA and the optional status display. Also used internally within the Processor CCA.	9-11	9
		9-13	6
		9-14	3
		9-15	5

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
DEMAND	Internal signal within the DPC Parallel Interface CCA generated during the load buffer cycle each time DATA STROBE goes low. Pre-requisite for generating DEMAND supplied to the user.	9-11	5
DEMAND	Output signal generated by the DPC Parallel Interface CCA and supplied to the user for requesting data. Raised once per character.	9-11	8
DESELECT	Signal generated within the DPC Centronics-Compatible Interface CCA from the deselect code (023 oct) supplied by the user. When active, places the printer off line.	9-14	8
DET POS	Position Detect signal supplied by the column 1 sensor to the Motor Driver CCA.	9-16	3
DISPLAY LD*	Display indicator enable supplied by the Processor CCA to the optional status display.	9-15	6
DPC/CEN*	Indicates whether or not the printer is configured with a DPC Centronics-Compatible Interface CCA. Supplied as a status bit (DBUF8) to the Processor CCA. 0 = Centronics 1 = DPC Parallel or Serial	9-11	9
		9-13	6
		9-14	3
DSR	Data Set Ready status signal supplied by the user to an RS232-configured Serial Interface CCA. When off (low), indicates that the printer must disregard all other interface signals. Signal may be overridden by a manual switch.	9-13	8
DTR	Data Terminal Ready status signal supplied by an RS232-configured Serial Interface CCA to the user. When high, indicates the following:	9-13	8

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
DTR (Contd)	a. Printer power is on. b. No printer faults exist. c. Printer is on line. d. Input buffer is not full.		
ENC INT REQ*	Interrupt signal generated when the Processor CCA detects an encoder mark.	9-15	6
ENRDR*	Generated by the Processor CCA, is used to enable the optional TCVFU tape reader.	9-15	7
EXPANDED	Generated by any Interface CCA upon detection of an EXPANDED code supplied by the user, and applied as a status bit (DBUF7) to the Processor CCA.	9-11	6
		9-14	6
EXPANDED DIS*	Option Header signal used, when low, to disable the expanded print option.	9-11	4
		9-13	6
		9-14	5
FAULT*	Signal supplied by the DPC Centronics-Compatible Interface CCA to the user indicating one of the following fault conditions:	9-14	4
	a. Printer is out of paper		
	b. Shuttle is not moving		
	c. Printer is deselected		
FF1	Internal signal generated within the DPC Parallel Interface and DPC Centronics-Compatible Interface CCAs. Defines the duration of the load buffer cycle.	9-11	5
		9-14	4
FF2	Internal DATASTROBE signal generated within the DPC Parallel Interface CCA, normally following DATASTROBE. When DATASTROBE	9-11	5

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
FF2 (Contd)	is supplied in a pulsed mode, the duration of FF2 is extended until DEMAND goes low.		
FF9	Parity error detect signal generated each time a parity error is detected. Used to clock PARITY ERROR flip-flop U2.	9-11	2
FLSS1*-FLSS4*	FORMS LENGTH SELECT switch 4-bit BCD output supplied to the Processor CCA.	9-10	2
G*	Composite chip select signal generated within the DPC Centronics-Compatible Interface CCA, and used to enable bi-directional driver U23.	9-14	9
G2A*	Composite logic term generated within the DPC Centronics-Compatible Interface CCA. Equivalent to MEMW* + MEMR*.	9-14	9
GO*/STOP	Shuttle motor control signal generated in the Processor CCA. When low, motor is turned on; when high, motor is turned off.	9-15	7
ICS1*-ICS16*	Chip select signals derived from the Serial Interface CCA address bus.	9-13	3
IMEMR*	Serial Interface CCA, internal memory read enable signal.	9-13	2
IMEMW*	Serial Interface CCA, internal memory write enable signal.	9-13	2
INPUT PRIME*	User-generated signal used to clear the line buffer and interface logic in the DPC Centronics-Compatible Interface CCA.	9-14	6
INTE	Interrupt enable output from the 8080 Processor of the Processor CCA. Not used in the Serial Interface CCA.	9-15	2

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
LD	Fault status signal decoded in the DPC Centronics-Compatible Interface CCA from bit DBUF6 supplied by the Processor CCA. Implies that the shuttle is not moving or the printer is deselected. Used to generate interface signal FAULT*.	9-14	3
LDBUFPULA*, B*	Pulses generated in the DPC Parallel Interface CCA on the low-to-high transition of the LOAD BUFFER signal. Used to initialize the interface logic and set flip-flop FF1.	9-11	5
LD BUFFER PL*	Same as LDBUFPULA*, B*. Generated in the DPC Centronics-Compatible Interface CCA.	9-14	4
LOAD BUFFER	Communication signal supplied by the Processor CCA on bit DBUF1, and decoded in any Interface CCA. Initiates the data load cycle.	9-11 9-13 9-14	9 6 3
LSB ADD BUS	Least significant bit of the DPC Centronics-Compatible Interface CCA address counter.	9-14	2
MEMR	Memory read enable signal generated in the Processor CCA.	9-15	2
MEMW	Memory write enable signal generated in the Processor CCA.	9-15	2
MEMR/W	Internal signal in the DPC Parallel Interface CCA, equivalent to MEMR+MEMW. Used to enable the chip select logic. Same as G2A* in the DPC Centronics-Compatible Interface CCA.	9-11	9
NDB1-NDB8	Internal data bus in the DPC Centronics-Compatible Interface CCA. Channels ASCII-coded user data.	9-14	6

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
OFF LINE ACK	On/Off line acknowledge signal generated in the DPC Centronics-Compatible Interface CCA and supplied on bit DBUF2 to the Processor CCA.	9-14	3
ON LINE	Status signal indicating that the printer is on line. Generated in the Processor CCA as status bit DBUF3 and decoded in any Interface CCA.	9-11	9
		9-13	6
		9-14	3
ON LINE	Status signal supplied by the DPC Parallel Interface CCA to the user.	9-11	8
ON LINE AK*	On/Off line acknowledge signal supplied by the DPC Parallel Interface CCA to the Processor CCA on bit DBUF2.	9-11	9
ON LINE FLOP	Signal stored in the on line flip-flop of the Processor CCA. Stores on/off line condition of the printer.	9-15	6
ON LINE LMP*	Signal generated in the Processor CCA and used to turn on the ON LINE indicator on the Operator Control Panel.	9-15	9
ON LINE USER	Intermediate signal in the DPC Parallel Interface CCA. Used to generate the ON LINE signal supplied to the user.	9-11	5
ON/OFF LINE*	Output of the ON LINE switch on the Operator Control Panel. Used to toggle ON LINE FF in the Processor CCA.	9-10	2
OSC2	2-mHz clock signal generated by the Processor CCA.	9-15	2
OSC18	18-mHz clock signal generated by the Processor CCA.	9-15	2

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
OSCFF	Internal clock signal generated in the DPC Parallel Interface CCA. Equivalent to OSC2+FF2.	9-11	2
OSCXT	100-kHz reference clock supplied by the DPC Centronics-Compatible Interface CCA to the user.	9-14	4
PAPER MOVING	Status signal supplied by the Processor CCA to the DPC Parallel Interface CCA on bit DBUF6, and thence to the user.	9-11	9
PARITY BIT	User-supplied input to the DPC Parallel Interface CCA. When the parity option is enabled, this signal codes the odd/even bit content of the input character.	9-11	8
PARITY EN*	Option header output signal. When low, enables the parity option.	9-11	4
		9-13	6
		9-14	5
PARITY ERROR	Generated in the DPC Parallel Interface CCA when a parity error is detected. Once generated, PARITY ERROR remains active for the duration of the data load cycle, and is reported as a DAVFU FAULT status bit on DBUF3 to the Processor CCA.	9-11	2
PARITY EVEN	Option header output signal used in conjunction with PARITY EN* to specify type of parity in the DPC Parallel Interface CCA: High = Even Parity Low = Odd Parity	9-11	4
PAPER INST	User-supplied input signal to the Interface CCAs. Indicates that the input data is either a VFU type paper instruction or a DAVFU START or DAVFU STOP code.	9-11	8
		9-14	6

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
PBTCNT	Indicates that the DPC Parallel Interface CCA has received the maximum number of print characters and disables the address counter until receipt of a paper motion control character.	9-11	7
PE	Paper empty status bit supplied by the Processor CCA on DBUF8 to the DPC Centronics-Compatible Interface CCA, and thence to the user. Not used in the DPC Parallel Interface CCA.	9-14	3
PERF SKIP1*, PERF SKIP2*	Two-bit perforation skip code supplied by the Option Header. Specifies the number of perforation skip lines per table 6-1.	9-11	4
		9-13	6
		9-14	5
PHASE 1*, PHASE 2*, PHASE 3*	Stepping motor control signals generated in the Processor CCA. Each signal controls a group of motor drive circuits associated with one of the three phase windings.	9-15	7
PL/DA TOP CNT	DAVFU top count signal generated in the DPC Parallel Interface CCA. Equivalent to signal 255 in the DPC Centronics-Compatible Interface CCA.	9-11	7
PS	Power protection signal. When power is first turned on, disables the motor and wire driver circuits until the +5V supply has come up to a safe level.	9-16	3
PS1*, PS2*	Inverted versions of PS.	9-17	2
RCLRFF*	Processor CCA signal used to reset the CLEAR flip-flop.	9-15	7
READY	Status signal supplied by the Processor CCA to any Interface CCA on DBUF2. Indicates that the printer can be placed on line.	9-11	9
		9-13	6
		9-14	3

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
READY	Status signal supplied by the DPC Parallel Interface CCA to the user. Amplified version of the Processor-supplied READY signal.	9-11	8
REC LINE SIG DET	User-generated RS232 signal supplied to the Serial Interface CCA. Indicates that the data communication equipment is receiving a signal which meets its suitability criteria.	9-13	8
RESETLF*, RESETRT*	Processor CCA signals used to reset the left and right direction flip-flops, respectively.	9-15	7
RESET*	Amplified version of POWER RESET* generated in the DPC Centronics-Compatible Interface CCA. Used to clear the BUSY flip-flop.	9-14	9
RIGHT*/LEFT	Shuttle motor direction signal supplied by the Processor CCA to the Motor Driver CCA. Right when low; left when high.	9-15	7
RMTR*	Ribbon motor control signal supplied by the Processor CCA to the Motor Driver CCA. When low, motor is turned on; when high, motor is turned off.	9-15	7
RTFF	Right dot column pulse generated in the Processor CCA. Low-to-high transition indicates the presence of a dot column encoder mark. High state indicates that the shuttle is moving from left to right.	9-15	6
RTS	Request to send output signal supplied by an RS232-configured Serial Interface CCA to the user. Always held in the low, off position since the printer operates only in the receive mode.	9-13	8

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
RxD	Received data input supplied by the user to an RS232-configured Serial Interface CCA. Contains the serial data stream.	9-13	8
RxD+, RxD-	Receive current loop terminals supplied by the user to the Serial Interface CCA.	9-13	8
SEL/DES	Decoded signal generated in the DPC Centronics-Compatible Interface CCA indicating that the input character supplied by the user is either a SELECT or DESELECT code.	9-14	6
SELECT	Decoded signal generated in the DPC Centronics-Compatible Interface CCA indicating that the input character supplied by the user is a SELECT code.	9-14	8
SELECT	Status signal generated in the DPC Centronics-Compatible Interface CCA upon receipt of a SELECT code, provided that the printer is in the READY state. Applied to the Processor CCA on DBUF5.	9-14	3
SELF TEST*	Switch-selected signal obtained from the Operator Control Panel. When low, places the printer in the self-test mode.	9-10	2
SCVP	SKIP COUNT*/VALID PRINT signal generated in the DPC Centronics-Compatible Interface CCA. When low, indicates that the character received is not a print or paper motion character, and inhibits the address counter.	9-14	7
SLCT	Equivalent to SELECT, supplied by the DPC Centronics-Compatible Interface CCA to the user.	9-14	4

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
SLT	Select flip flop signal in the DPC Centronics-Compatible Interface CCA. Set upon receipt of SELECT code from the user.	9-14	4
STBINST*	Stored condition of DATASTB generated in the DPC Parallel Interface CCA. Extends the duration of the strobe until DEMAND goes low.	9-11	7
STEP*	Stepping motor control signal generated in the Processor CCA. When low, enables the circuits that control the common side of the stepping motor.	9-15	7
TB8	Logic term that controls bit 8 of the character stored in the DPC Parallel Interface CCA line buffer. When the user supplies 8 data bits per character, TB8 follows bit 8 of the user data. When the user supplies 7 data bits per character, TB8 is always high (logical "1").	9-11	2
TCVFU*	Option header output signal. When low, enables the TCVFU option.	9-11 9-13 9-14	4 6 5
TOF (Internal)	Status signal supplied by the Processor CCA on DBUF4 to the DPC Parallel and Serial Interface CCAs. When active, indicates that paper is at the top of form position.	9-11 9-13	9 6
TOF (User)	An amplified version of the TOF (Internal) supplied to the user.	9-11	8
TOFSW*	TOP OF FORM switch output signal. When switch is pressed, the signal goes low (active), causing paper to move to the top of the next form.	9-10	2

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
TPI	Qualified version of paper instruction signal PI, generated in both the DPC Parallel and DPC Centronics -Compatible Interface CCAs. Follows PI supplied by the user when either DAVFU or TCVFU option has been enabled.	9-11 9-14	2 6
TRRQ*	TCVFU read-request signal generated by the optional TCVFU when the operator presses the read switch. Signal is routed through the applicable Interface CCA to the Processor CCA.	9-11 9-13 9-14	4 5 6
TxD	Generated in the USART chip of the Serial Interface CCA, this signal enables the active current loop ATxD+, ATxD-.	9-13	7
TxD+, TxD-	Passive output current loop terminals of the Serial Interface CCA. Loop is closed when the printer is not busy.	9-13	8
USER DEM	Logic term developed in the DPC Parallel Interface CCA from the internal DEMAND signal and used to generate DEMAND supplied to the user. Allows the printer to communicate with the user in both the pulsed and handshake modes.	9-11	7
VFC	Generated in the DPC Centronics-Compatible Interface CCA upon receipt of a PI-coded paper motion control character.	9-14	6
WR*	Write enable term generated in the DPC Centronics-Compatible Interface CCA. Allows user or Processor CCA data to be written into the line buffer.	9-14	9

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
WRITE*	Write enable term generated in the DPC Parallel Interface CCA. Allows user data to be written into the line buffer.	9-11	5
1L*-7L*	Left wire register bits, generated in the Processor CCA.	9-15	8
1L0-7L0	Left wire driver bits, negative terminals.	9-17	3
1L1-7L1	Left wire driver bits, positive terminals.	9-17	3
1R*-7R*	Right Wire Register bits, generated in the Processor CCA.	9-15	8
1R0-7R0	Right wire driver bits, negative terminals.	9-12 9-12	2 3
1R1-7R1	Right wire driver bits, positive terminals.	9-17	2
6/8* LPI	Vertical line pitch select signal controlled by the optional LPI select switch on the operator control panel and applied to the Processor CCA. When high, vertical line pitch is 6 LPI; when low, vertical line pitch is at 8 LPI.	9-10	2
7*/8 BIT	Option header output signal that specifies the number of bits per character supplied by the user. When low, number of bits is 7; when high, number of bits is 8.	9-11 9-13 9-14	4 6 5
10/16* PITCH	Horizontal line pitch select signal controlled by the optional LPI switch on the Operator Control Panel and applied to the Processor CCA. When high, horizontal line pitch is 10/inch; when low, horizontal line pitch is 16/inch.	9-10	2

TABLE 9-1. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Definition	Source	
		Figure	Sheet
10*/16 SHTL	Generated in the Processor CCA, this signal specifies the speed of the shuttle motor. When low, shuttle moves at 34 ips; when high, shuttle moves at 20.4 ips.	9-15	7
11/12* FORM	Option Header output signal that specifies 11" or 12" form length. When high, form length is 11 inches; when low, form length is 12 inches. If the printer is equipped with the optional FORM LGTH switch, form length is determined by that switch setting regardless of the value of signal 11/12* FORM.	9-11	4
		9-13	6
132/220	Top Count signal generated in the DPC Centronics-Compatible Interface CCA when the character count equals either 132 (normal or expanded print) or 220 (condensed print). If auto print is enabled, this signal causes the DPC Centronics-Compatible Interface CCA to stop loading data and generate a BUFFER FULL signal.	9-14	2
222	Signal generated in the DPC Centronics-Compatible Interface CCA indicating that the number of print characters received from the user is 222, the absolute maximum. Characters in addition to this number are not registered until the user transmits a paper motion control character. 222 is the equivalent to PBTCNT in the DPC Parallel Interface CCA.	9-14	2
255	Signal generated in the DPC Centronics-Compatible Interface CCA indicating that the number of DAVFU characters (not counting START) is 510, the absolute maximum. If the next character is not a DAVFU STOP code, a DAVFU FAULT condition exists. See PL/DA TOP CNT.	9-14	2

9.6 LIST OF DIAGRAMS

Table 9-2 lists by figure number, the complement of power distribution, power supply, power regulation, and logic diagrams contained in this section of the manual.

TABLE 9-2. LIST OF DIAGRAMS

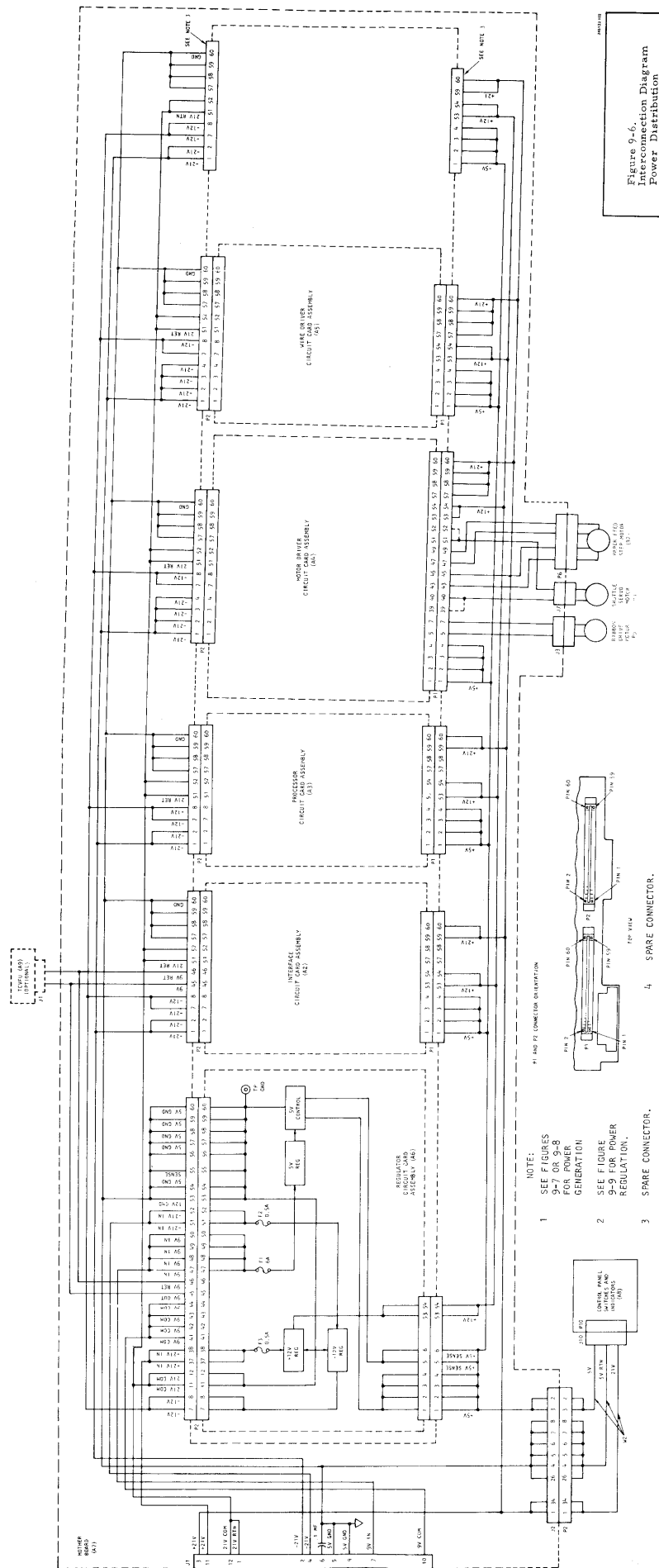
Figure No.	Title	Page	Number of Sheets
9-6	Interconnection Diagram, Power Distribution	9-30	1
9-7	Schematic Diagram, Power Supply, Standard	9-32	3
9-8	Schematic Diagram, Power Supply, Universal	9-35	5
9-9	Schematic Diagram, Regulator CCA	9-40	2
9-10	Schematic Diagram, Control Panel	9-42	2
9-11	Logic Diagram, DPC Short Line Parallel Interface CCA	9-43	9
9-12	Logic Diagram, DPC Long Line Parallel Interface CCA	9-52	9
9-13	Logic Diagram, Serial Interface CCA	9-61	8
9-14	Logic Diagram, DPC Centronics-Compatible Interface CCA	9-69	9
9-15	Logic Diagram, Processor CCA	9-78	9
9-16	Schematic Diagram, Motor Driver CCA	9-83	4
9-17	Schematic Diagram, Wire Driver CCA	9-87	3
9-18	Logic Diagram, Tape Controlled Vertical Format Unit	9-90	2
9-19	Mother Board (Wire List)	9-92	3

9.7 SIGNAL ORIGIN/DESTINATION

On each logic diagram sheet, input and output signals are cross-referenced by origin and destination, respectively. Cross-referencing between sheets of the same figure is denoted by an alphanumeric code. The first digit (or first two digits) of the code refers to the sheet number, and the other two digits direct the reader to an alphanumeric coordinate within the referenced sheet. Signals originating in or destined for another figure are denoted by a figure number, and, where applicable, also by the sheet number.

Example: On sheet 6 of figure 9-15, logic term ON LINE FLIP-FLOP is denoted by the three-digit code 7C8. The digit "7" directs the reader to sheet 7 of figure 9-15, and the digits "C8" direct the reader to coordinate C8 of sheet 7.

LOGIC DIAGRAMS

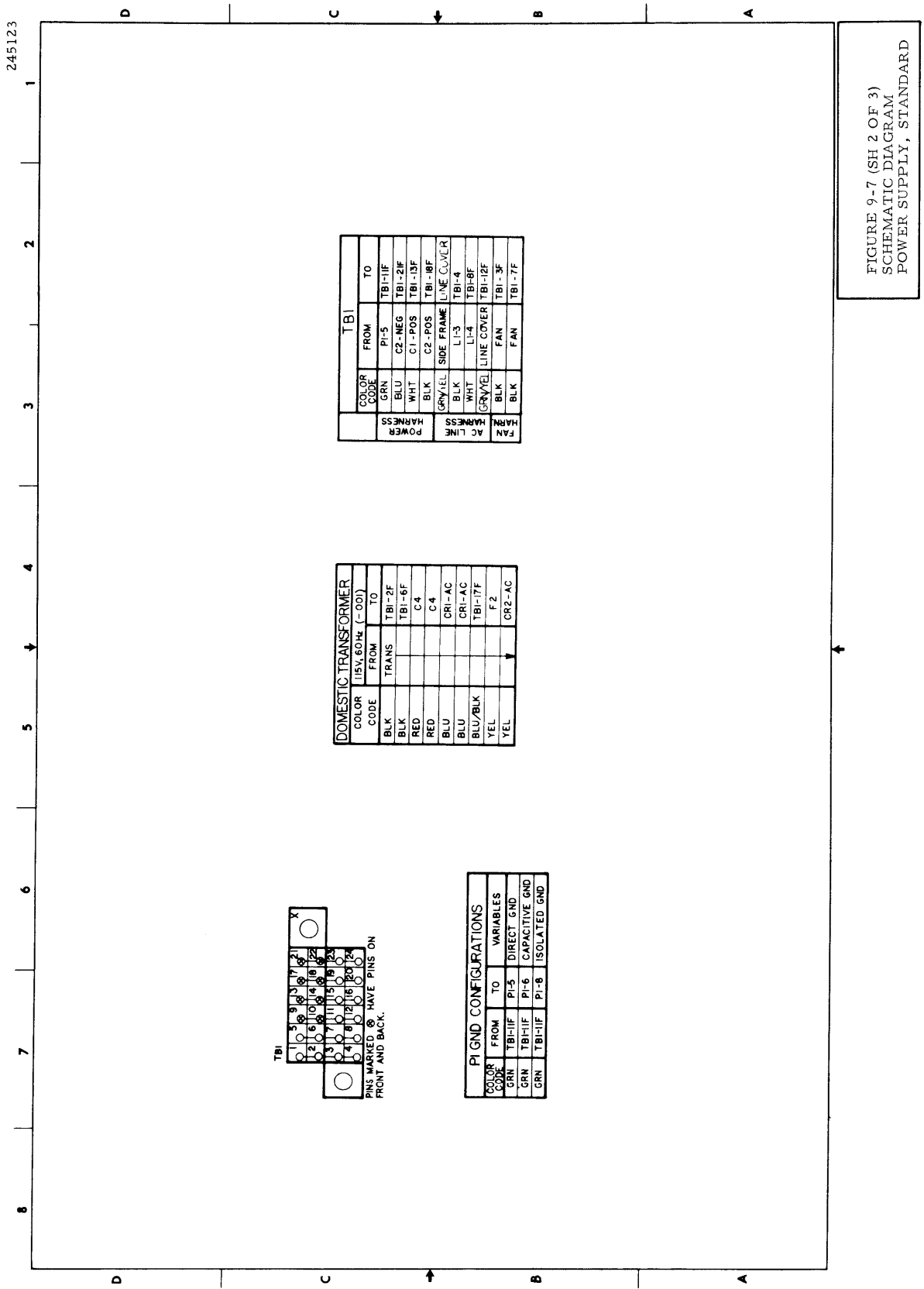


4. REFERENCE SCHEMATIC DIAGRAM 245870, REV. A.
3. TERMINAL BLOCK REFERENCE DESIGNATIONS: PIN NO. FOLLOWED BY FRONT (F) OR BACK (B). E.G. 22B IS PIN NO. 22 ON BACK (B) OF TERMINAL BLOCK.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, +75%, -10%, 30 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 20W.

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 9-7 (SH 1 OF 3)
SCHEMATIC DIAGRAM
POWER SUPPLY, STANDARD

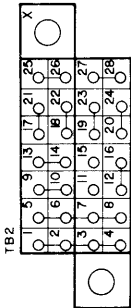
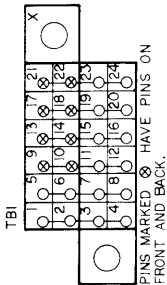
245123





245123

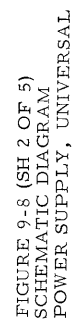
	TBI		
	COLOR CODE	FROM	TO
POWER HARNESS	GRN	PI-5	TBI-1IF
	BLU	C2-NEG	TBI-2IF
	WHT	CI-POS	TBI-13F
	BLK	C2-POS	TBI-18F
AC LINE HARNESS	GRN/YEL	SIDE FRAME	LINE COVER
	BLK	LI-3	TBI-4
	WHT	LI-4	TBI-8F
FAN HARNESS	GRN/YEL	LINE COVER	TBI-12F
	BLK	FAN	TB2-1
	BLK	FAN	TB2-5



	PI GND CONFIGURATION		
	COLOR CODE	FROM	TO
GRN	TBI-1IF	PI-5	DIRECT GND
GRN	TBI-1IF	PI-6	CAPACITIVE GND
GRN	TBI-1IF	PI-8	ISOLATED GND

8. 220/50 Hz CONFIGURATION SHOWN ON SHEET 5.
7. 115/50 Hz CONFIGURATION SHOWN ON SHEET 4.
6. 220/60 Hz CONFIGURATION SHOWN ON SHEET 3.
5. 115/60 Hz CONFIGURATION SHOWN ON SHEET 2.
4. REFERENCE SCHEMATIC DIAGRAM 245871, REV. A.
3. TERMINAL BLOCK REFERENCE DESIGNATIONS: PIN NO. FOLLOWED BY FRONT (F) OR BACK (B), E. G. 22B IS PIN NO. 22 ON BACK (B) OF TERMINAL BLOCK.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 75%, -10%, 30 VOLT.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 20W
- NOTES (UNLESS OTHERWISE SPECIFIED)

FIGURE 9-8 (SH 1 OF 5)
SCHEMATIC DIAGRAM
POWER SUPPLY, UNIVERSAL



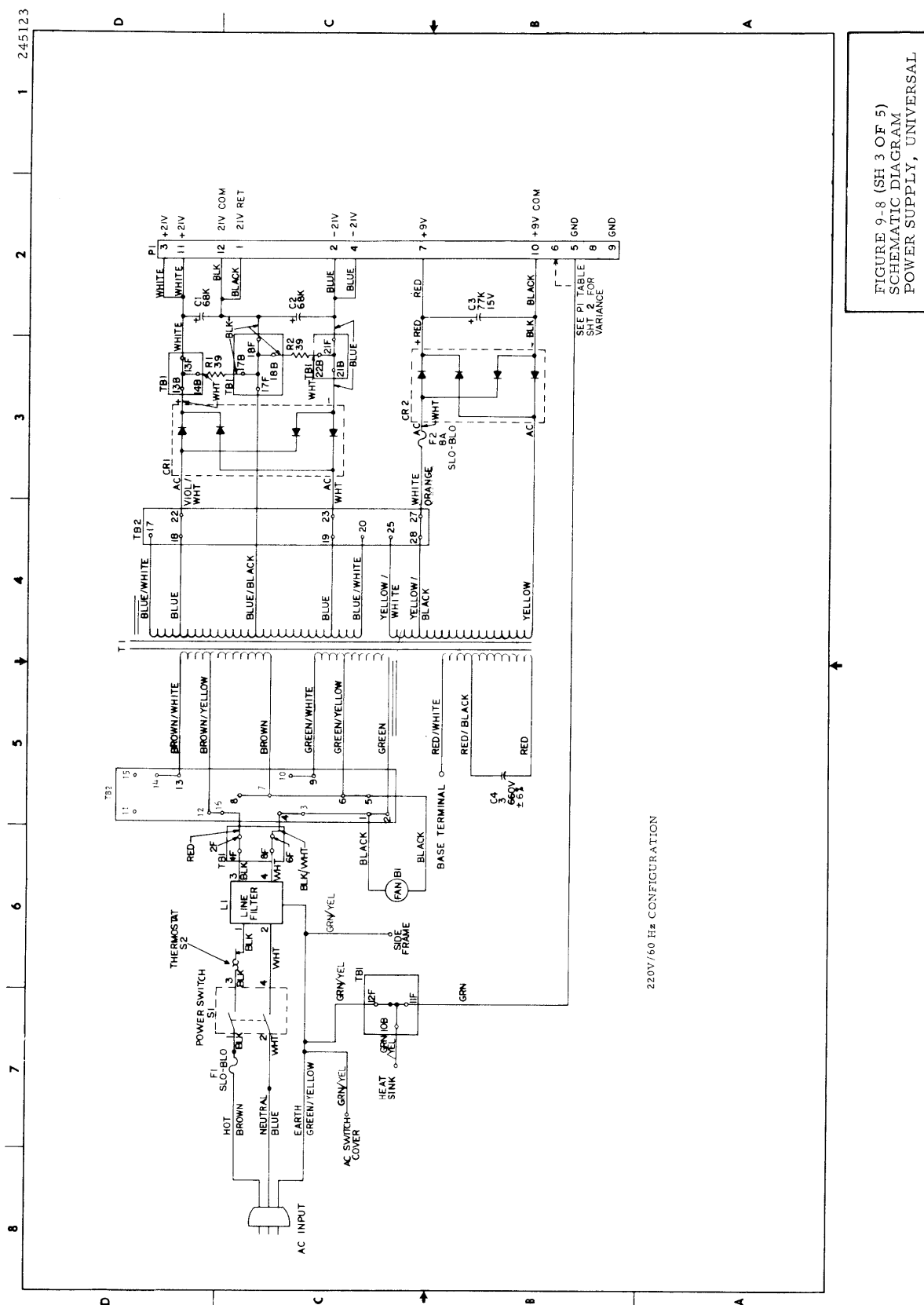


FIGURE 9-8 (SH 3 OF 5)
SCHEMATIC DIAGRAM
POWER SUPPLY, UNIVERSAL



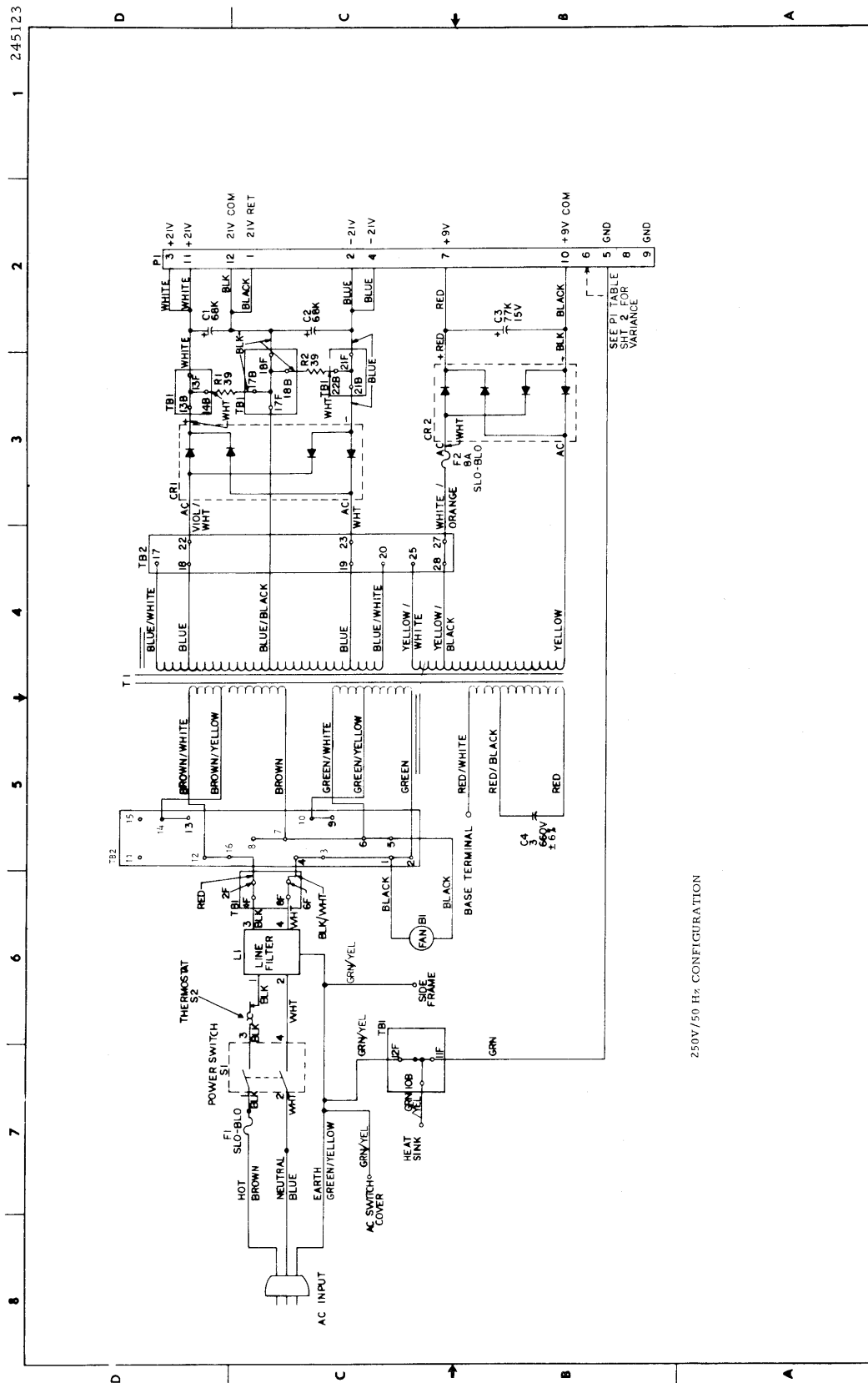
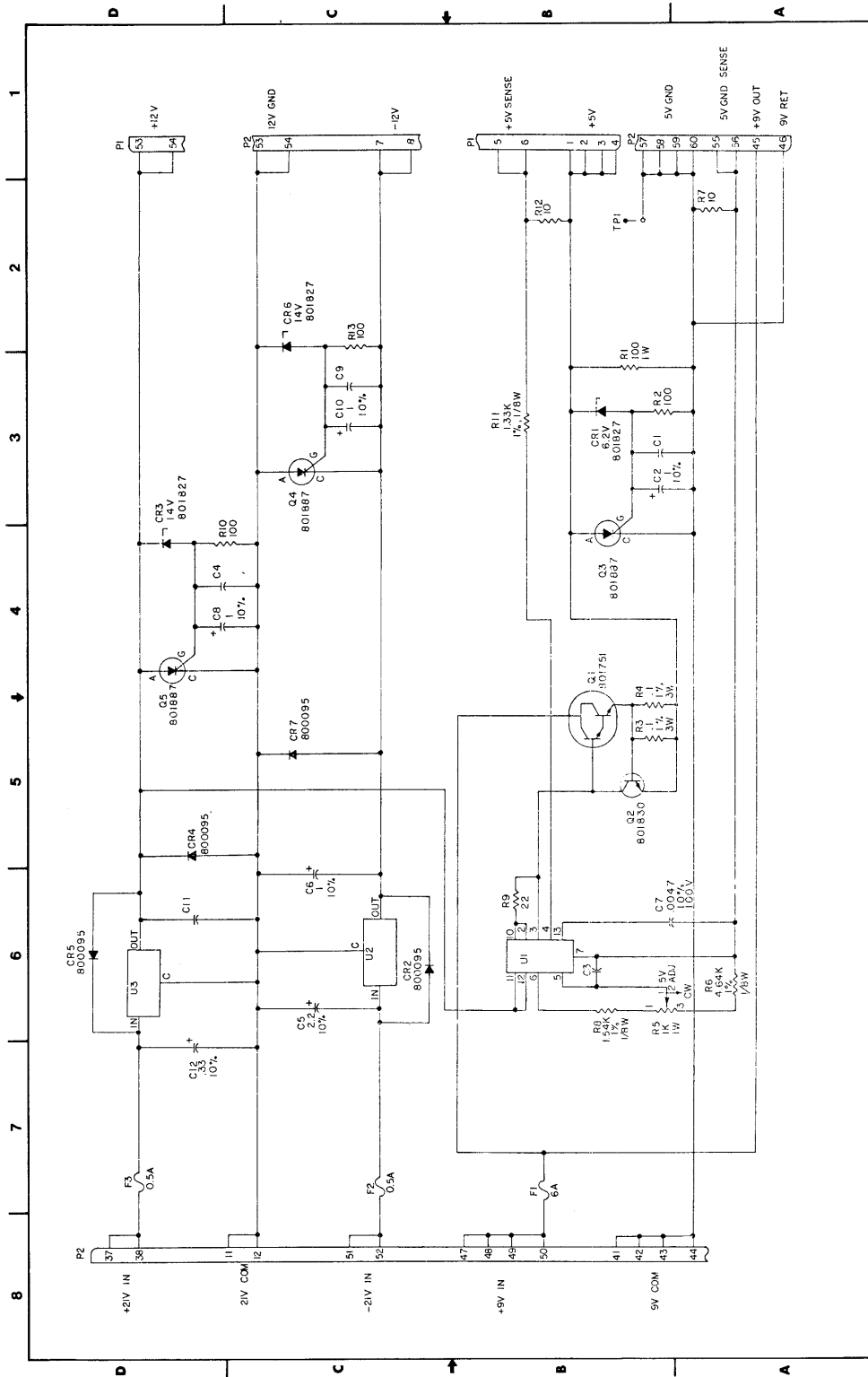


FIGURE 9-8 (SH 5 OF 5)
SCHEMATIC DIAGRAM
POWER SUPPLY, UNIVERSAL

NOTES(UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTANCE VALUES ARE IN OHMS 5%,1/4W
2. ALL CAPACITANCE VALUES ARE IN UF, +80%,-20%,50V.
3. ALL CAPACITORS ARE .1UF
4. INTEGRATED CIRCUITS ARE:
 801179 (723) :U1
 801205(7912) :U2
 801204(7812) :U3

MODEL M200
 FIGURE 9-9 (SH 1 OF 2)
 SCHEMATIC DIAGRAM
 REGULATOR CCA



MODEL M200
FIGURE 9-9 (SH 2 OF 2)
SCHEMATIC DIAGRAM
REGULATOR CCA

4. REFERENCE SCHEMATIC DIAGRAM 245869, REV A.
- ③ OPTIONAL ITEMS: NOT ON -001 ASSEMBLY.
2. SIGNAL MNEMONICS WHICH CONTAIN A BAR (—) ARE ACTIVE IN THE
1. INTEGRATED CIRCUITS ARE:
(GENERIC PART NUMBERS ARE PROVIDED FOR "REFERENCE ONLY")
801996-001 T1L311 U1,2

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 9-10 (SH 1 OF 2)
SCHEMATIC DIAGRAM
CONTROL PANEL

245123

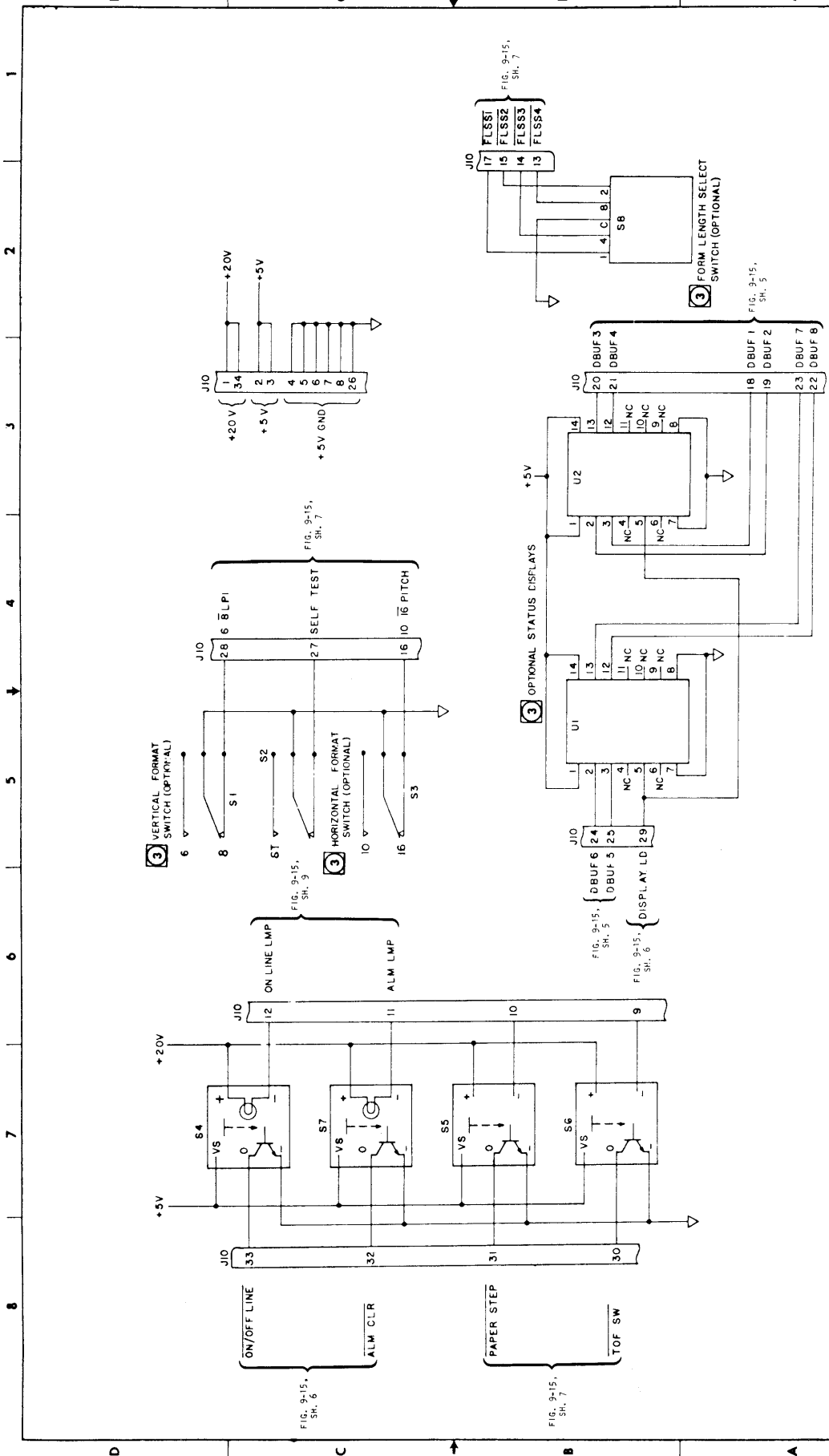
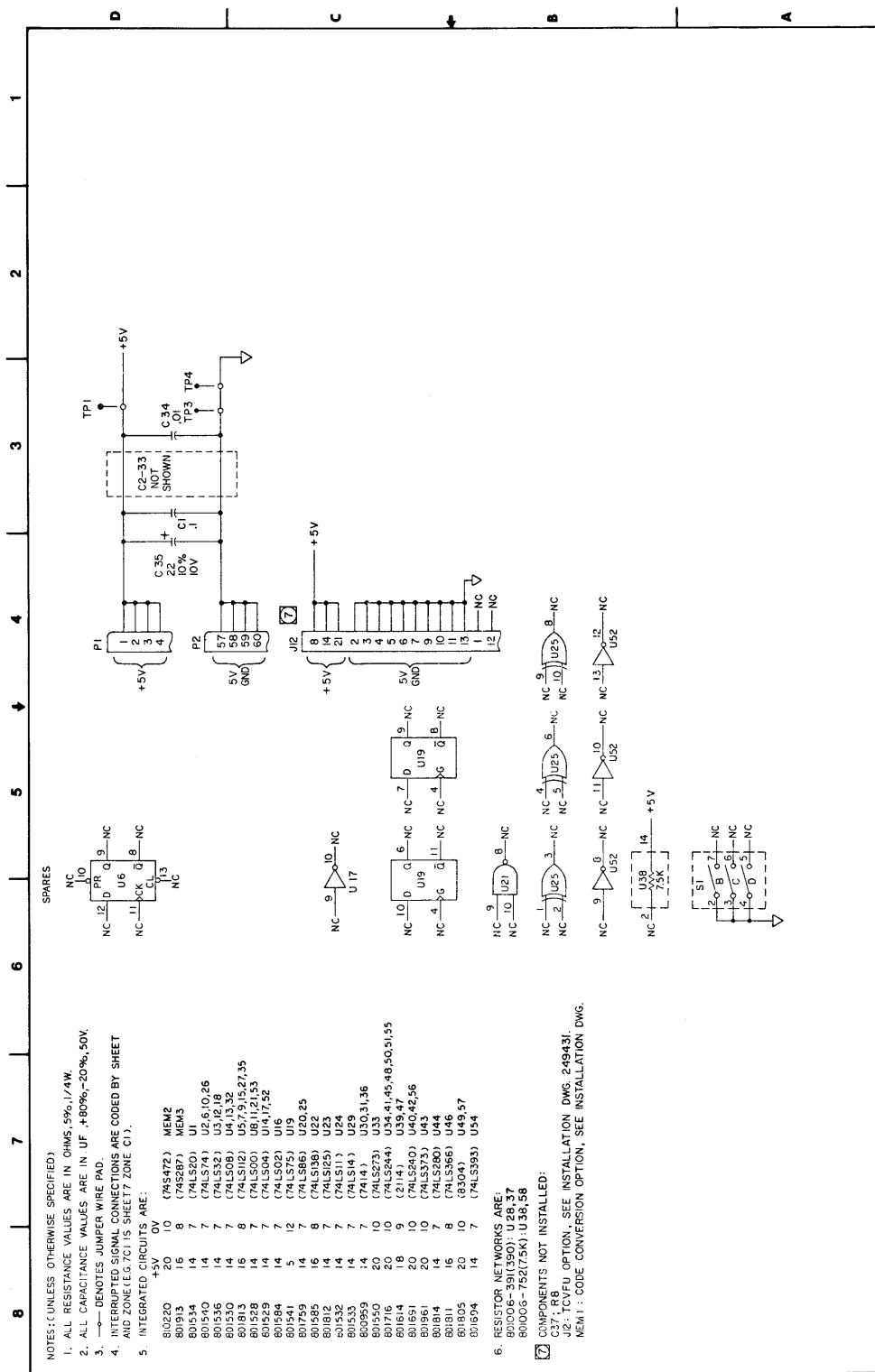


FIGURE 9-10 (SH 2 OF 2)
SCHEMATIC DIAGRAM
CONTROL PANEL

MODEL M200
FIGURE 9-11 (SH 1 OF 9)
LOGIC DIAGRAM
DPC SHORT-LINE PARALLEL
INTERFACE CCA



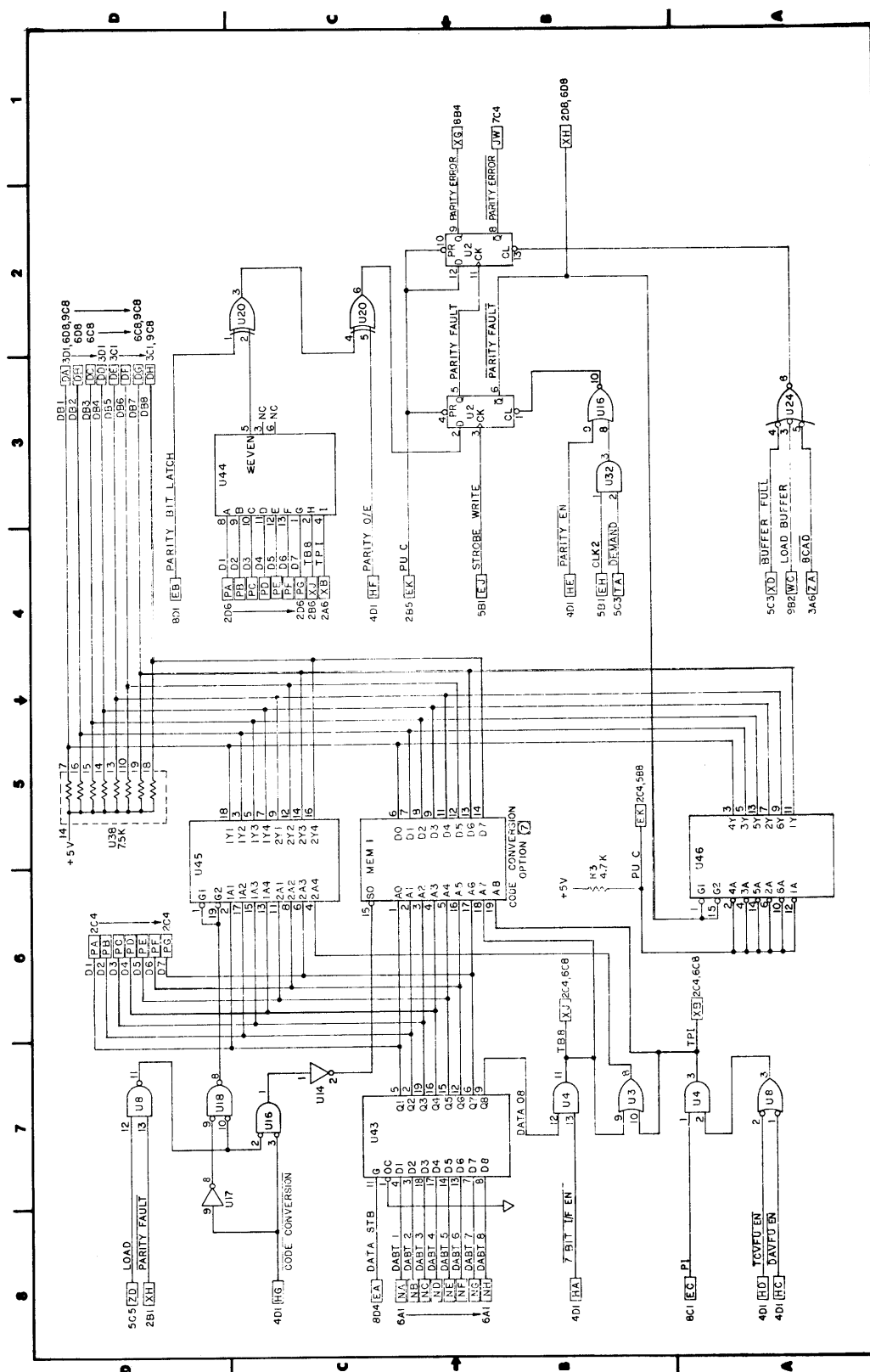
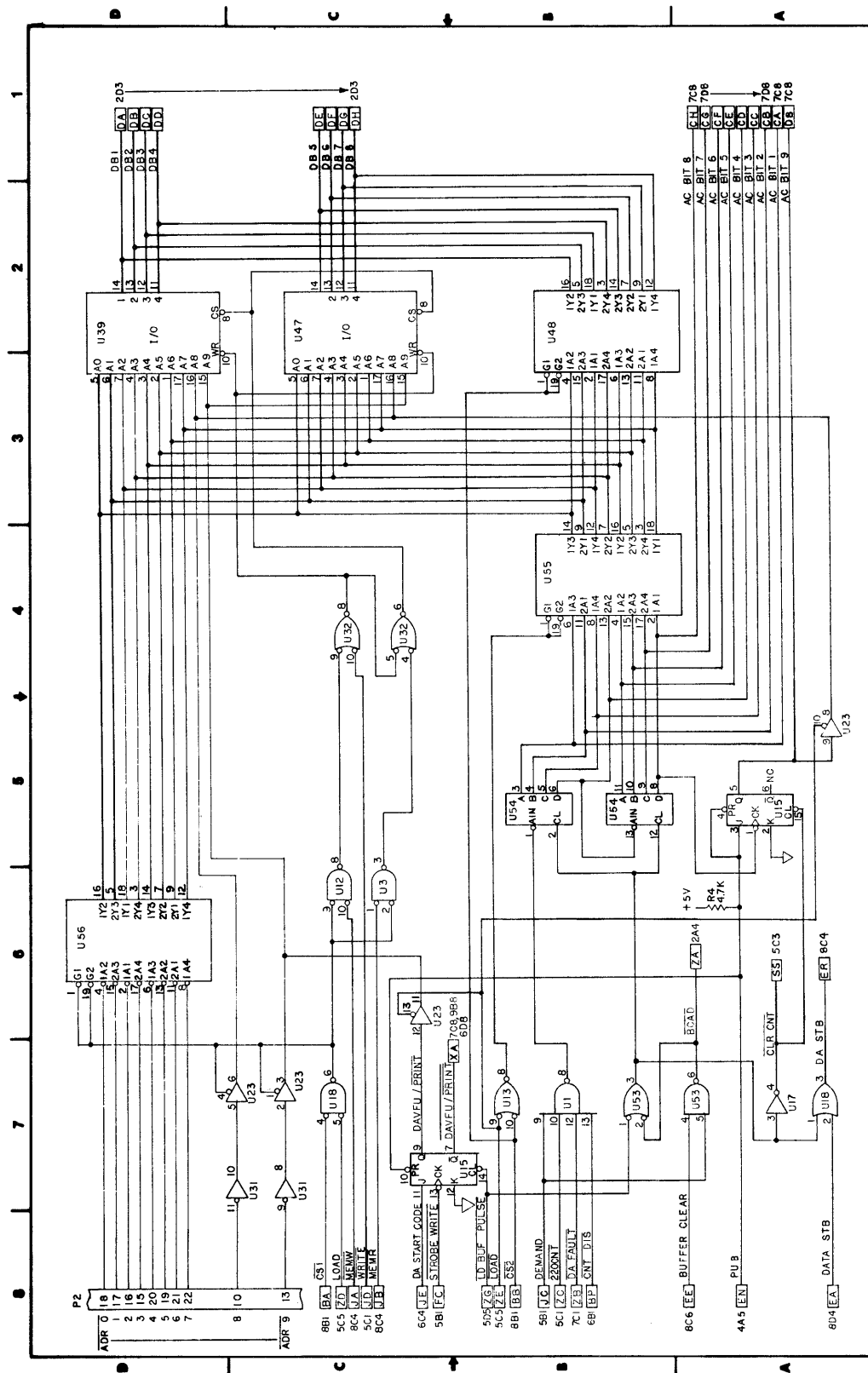
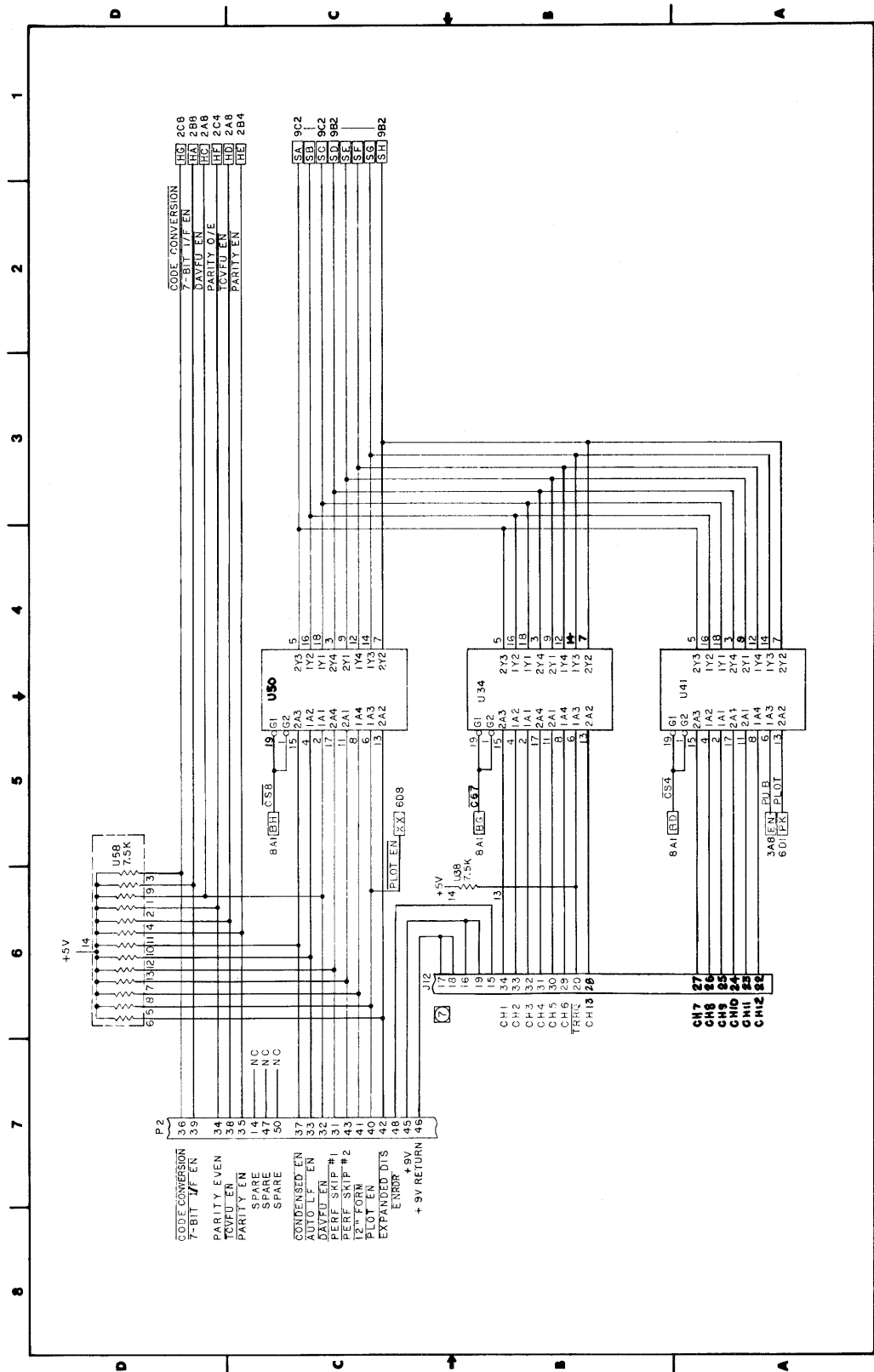


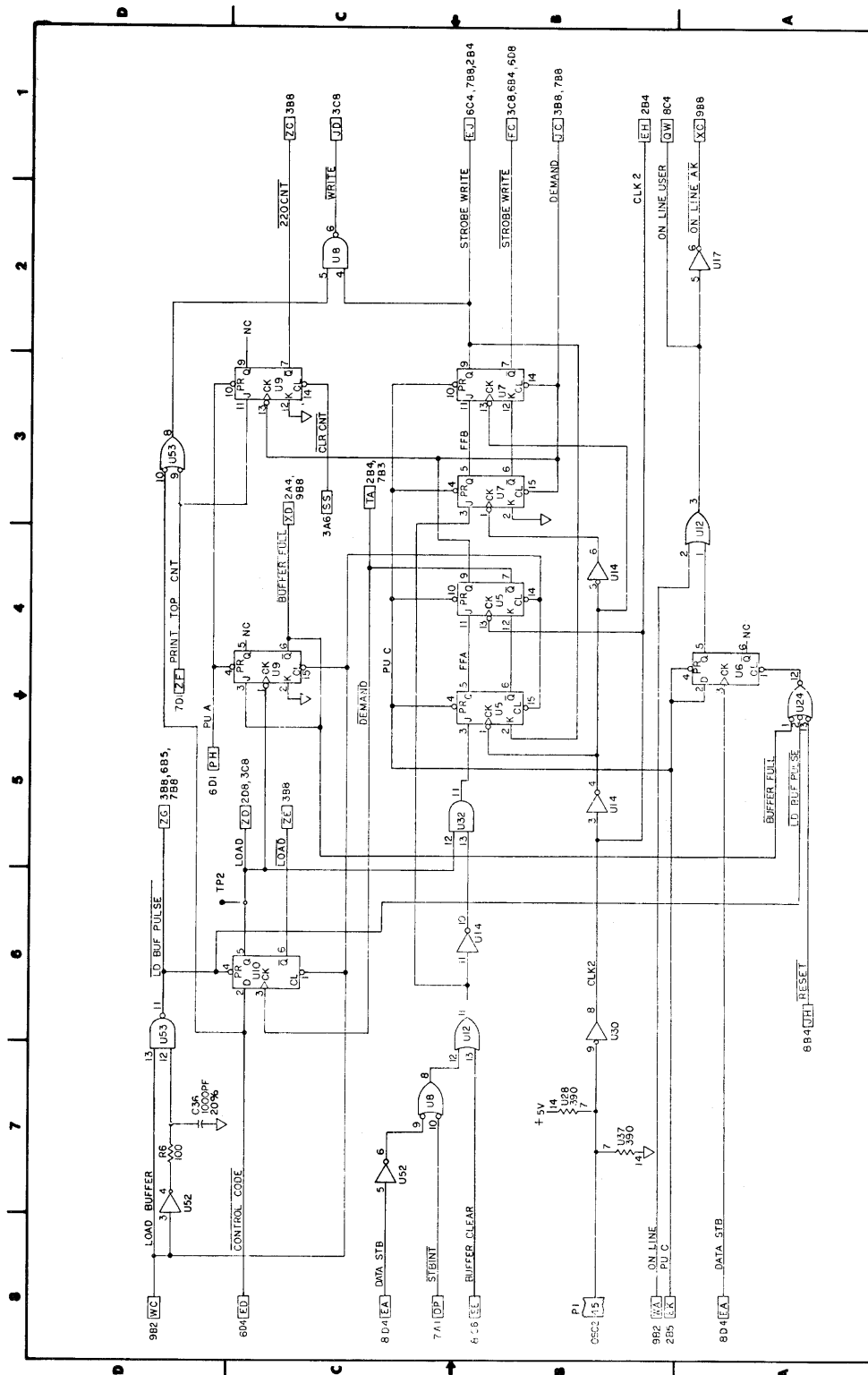
FIGURE 9-11 (SH 2 OF 9)
LOGIC DIAGRAM
DPC SHORT-LINE PARALLEL
INTERFACE CCA

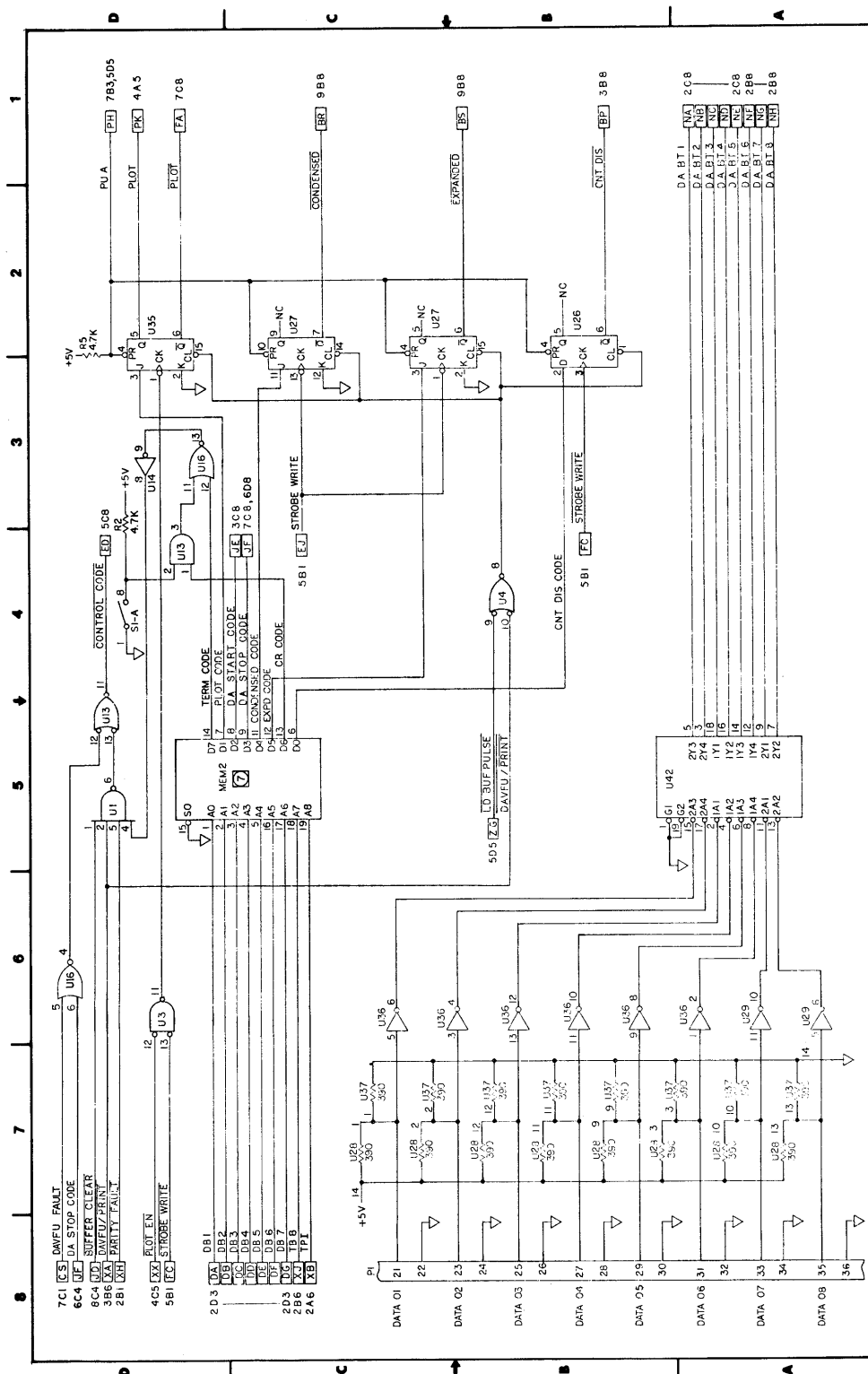


MODEL M200
FIGURE 9-11 (SH 3 OF 9)
LOGIC DIAGRAM
DPC SHORT-LINE PARALLEL
INTERFACE CCA

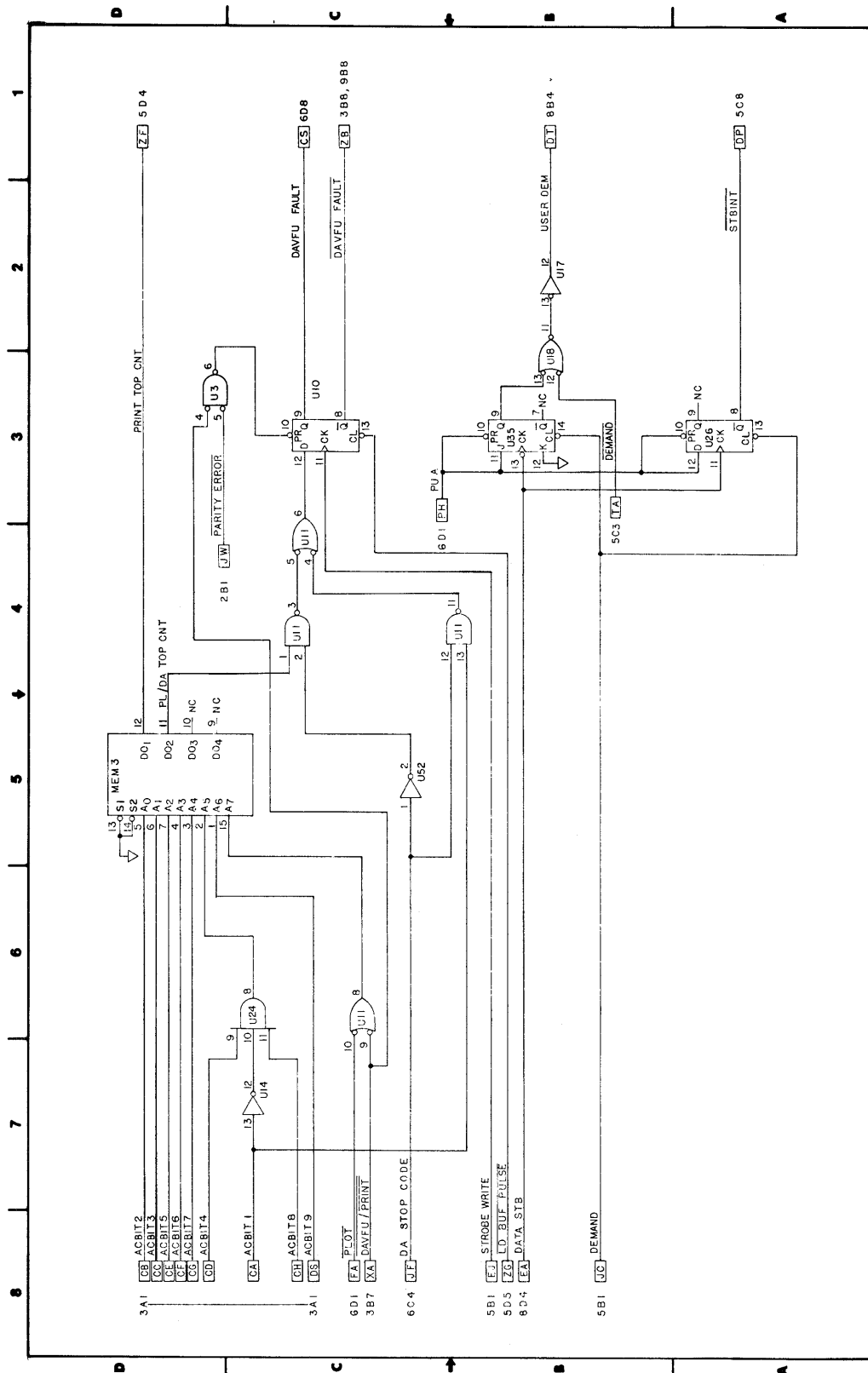


MODEL M200
FIGURE 9-11 (SH 4 OF 9)
LOGIC DIAGRAM
DPC SHORT LINE
PARALLEL INTERFACE CCA

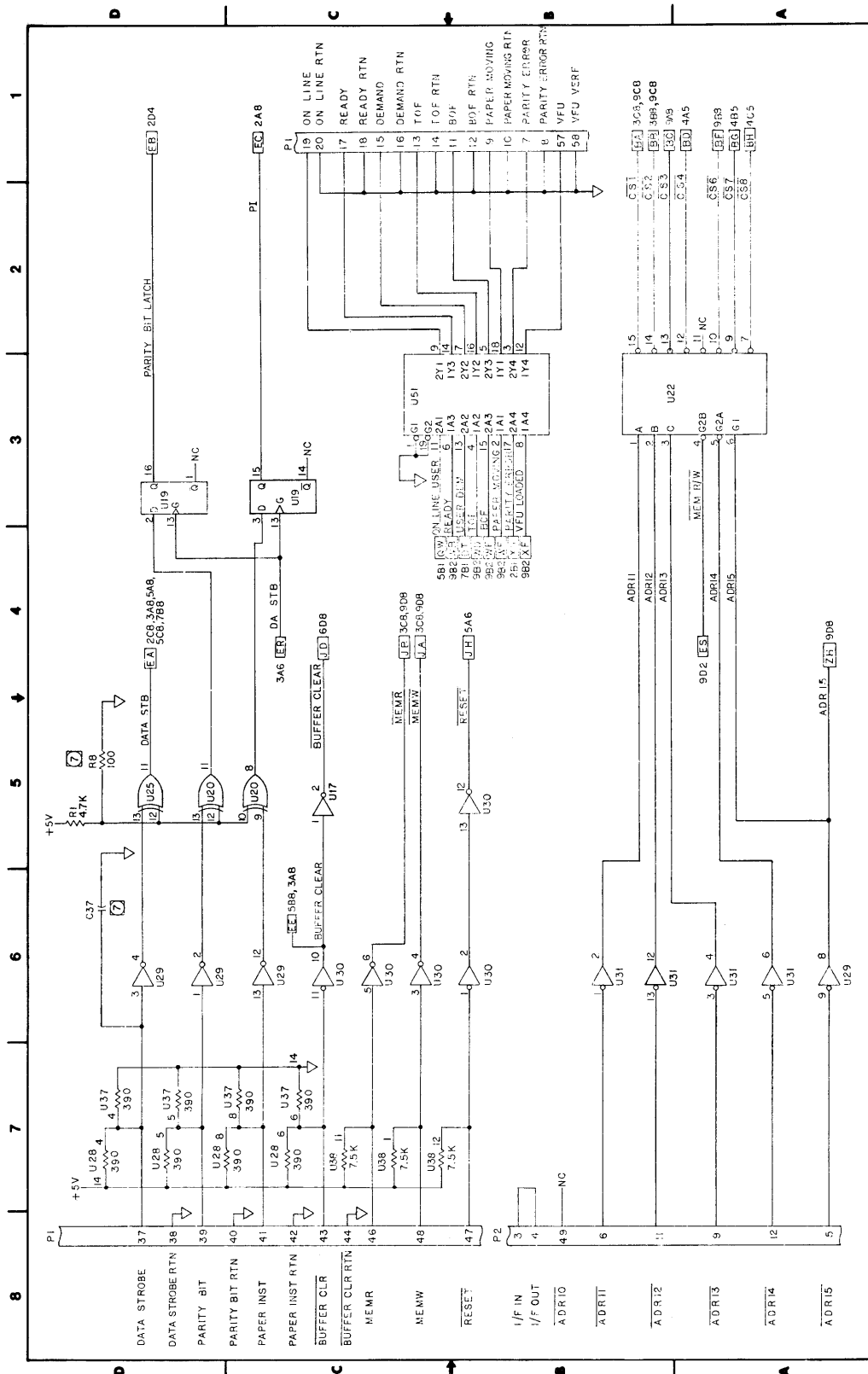




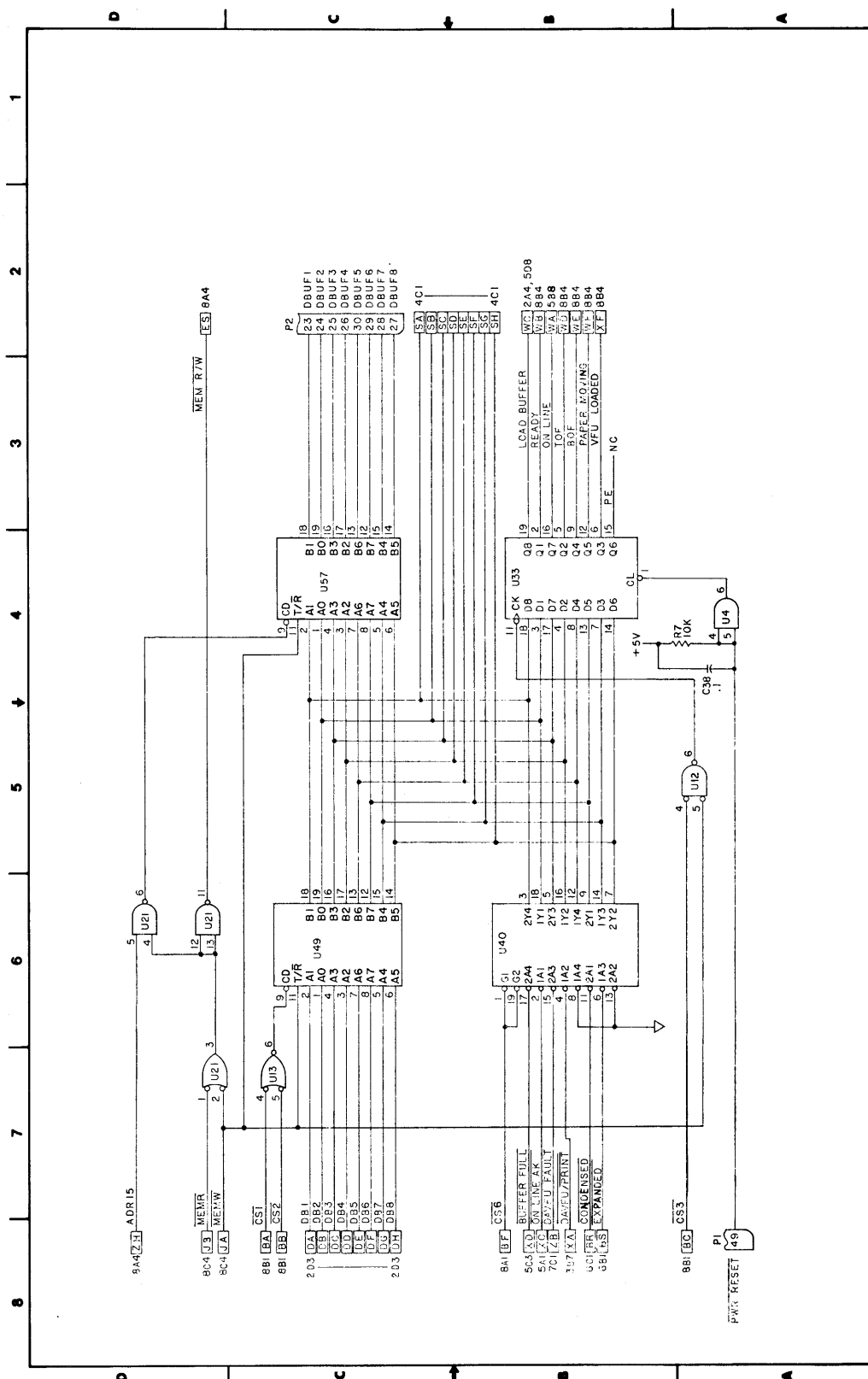
MODEL M200
FIGURE 9-11 (SH 6 OF 9)
LOGIC DIAGRAM
DPC SHORT-LINE PARALLEL
INTERFACE CCA

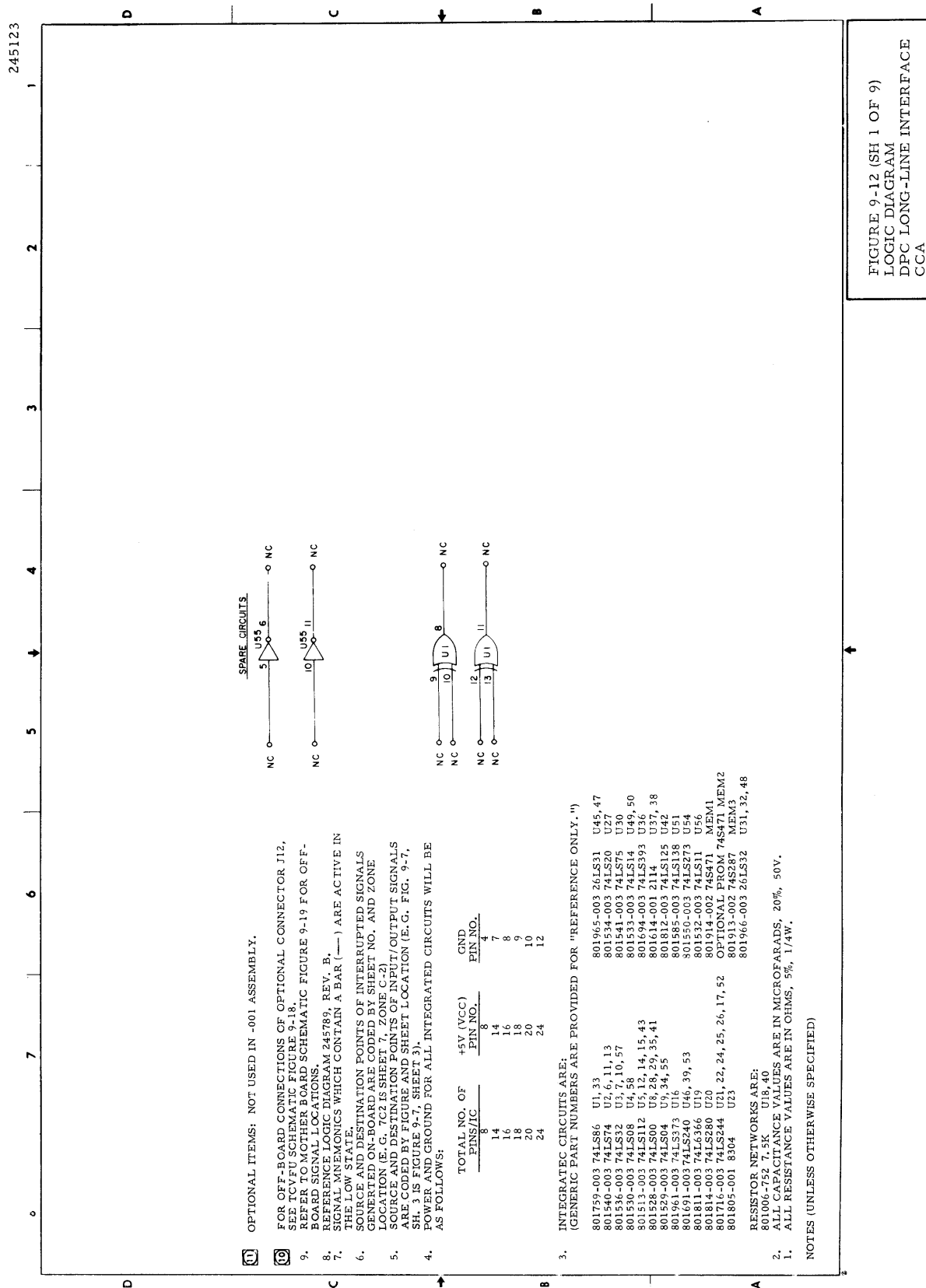


MODEL M200
FIGURE 9-11 (SH 7 OF 9)
LOGIC DIAGRAM
DPC SHORT-LINE PARALLEL
INTERFACE CCA



MODEL M200
FIGURE 9-11 (SH 8 OF 9)
LOGIC DIAGRAM
DPC SHORT-LINE PARALLEL
INTERFACE CCA





245123

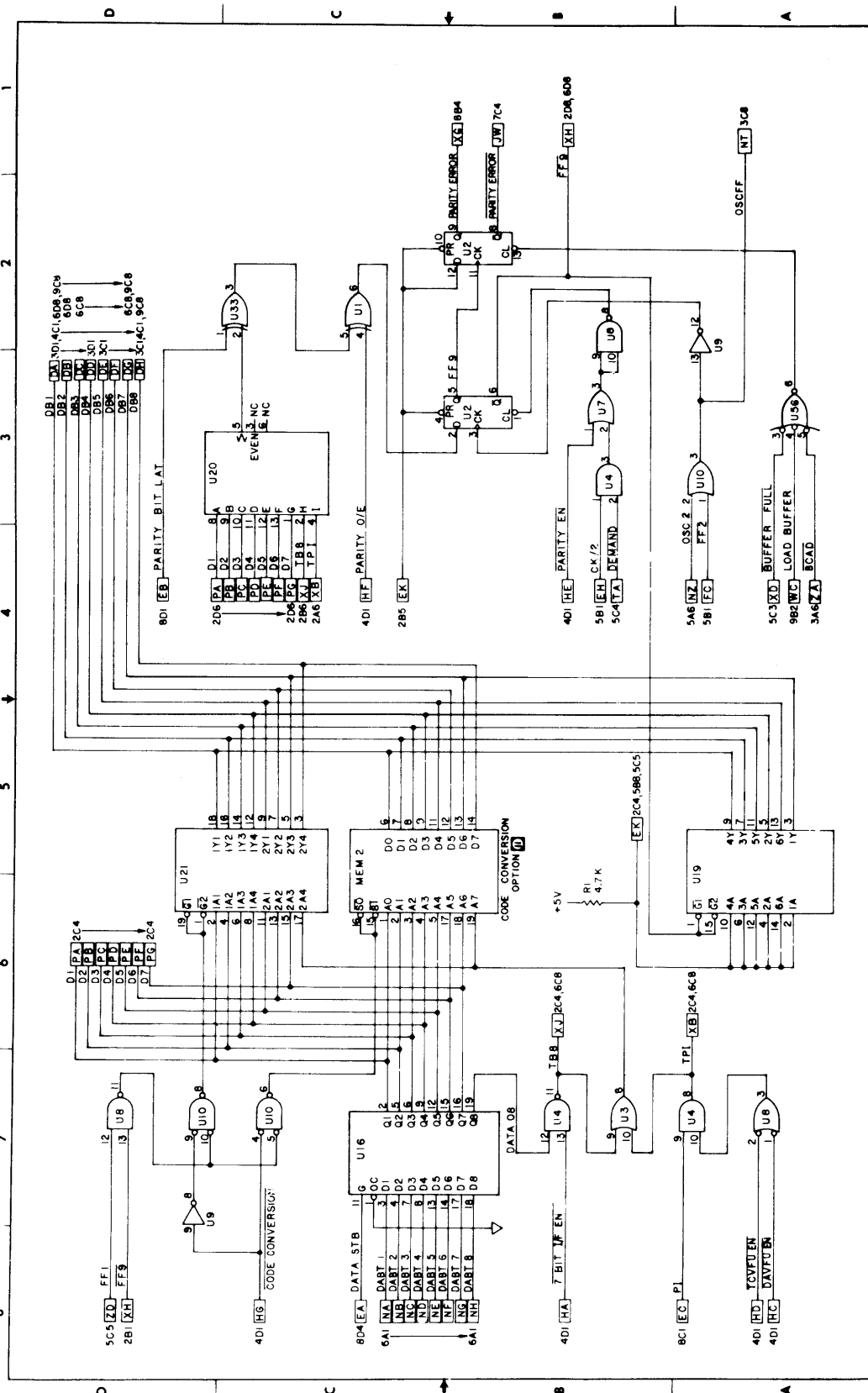


FIGURE 9-12 (SH 2 OF 9)
LOGIC DIAGRAM
DPC LONG-LINE INTERFACE
CCA



245123

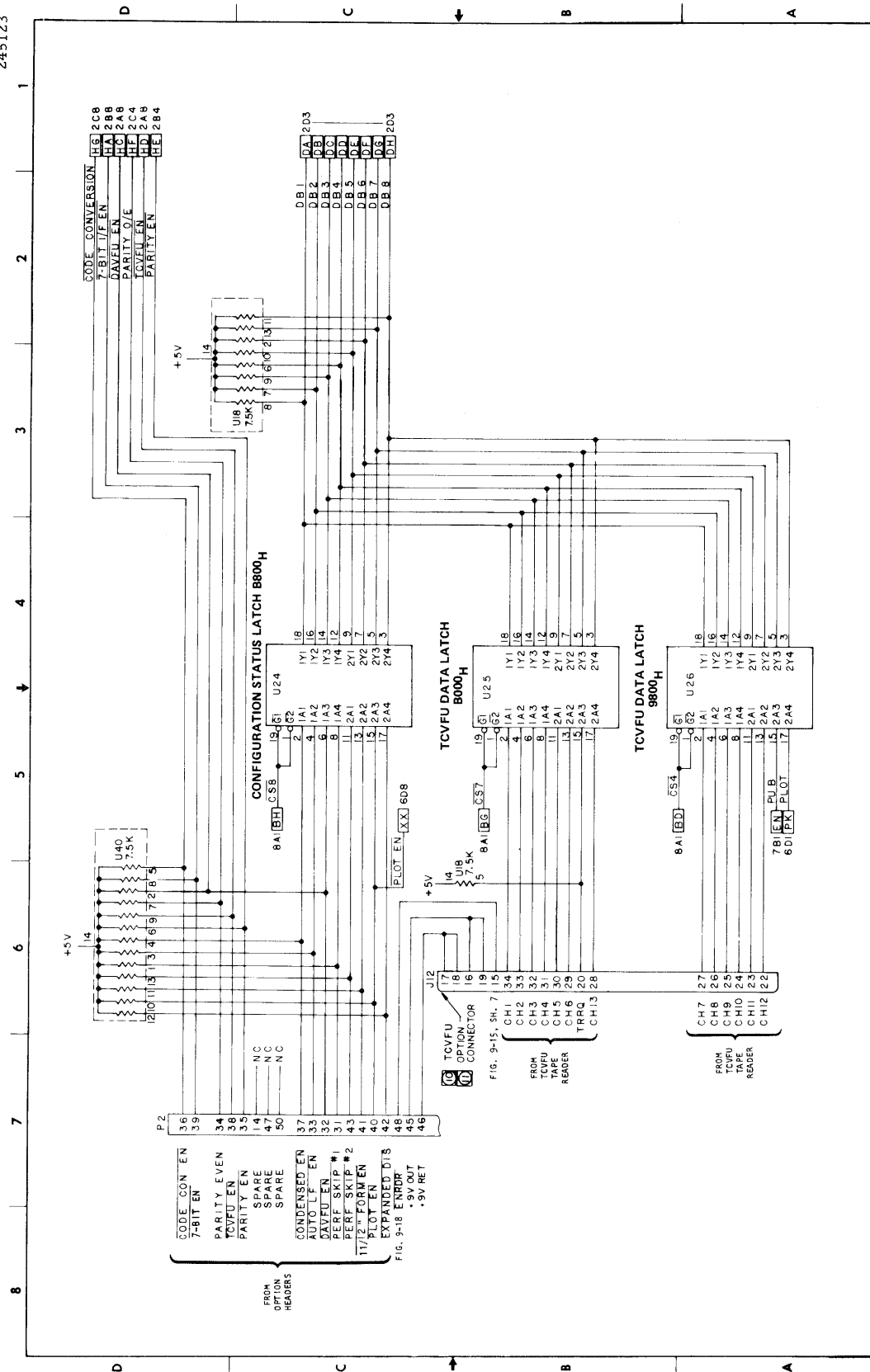


FIGURE 9-12 (SH 4 OF 9)
LOGIC DIAGRAM
DPC LONG-LINE INTERFACE
CCA



4643 PRINTER SERVICE

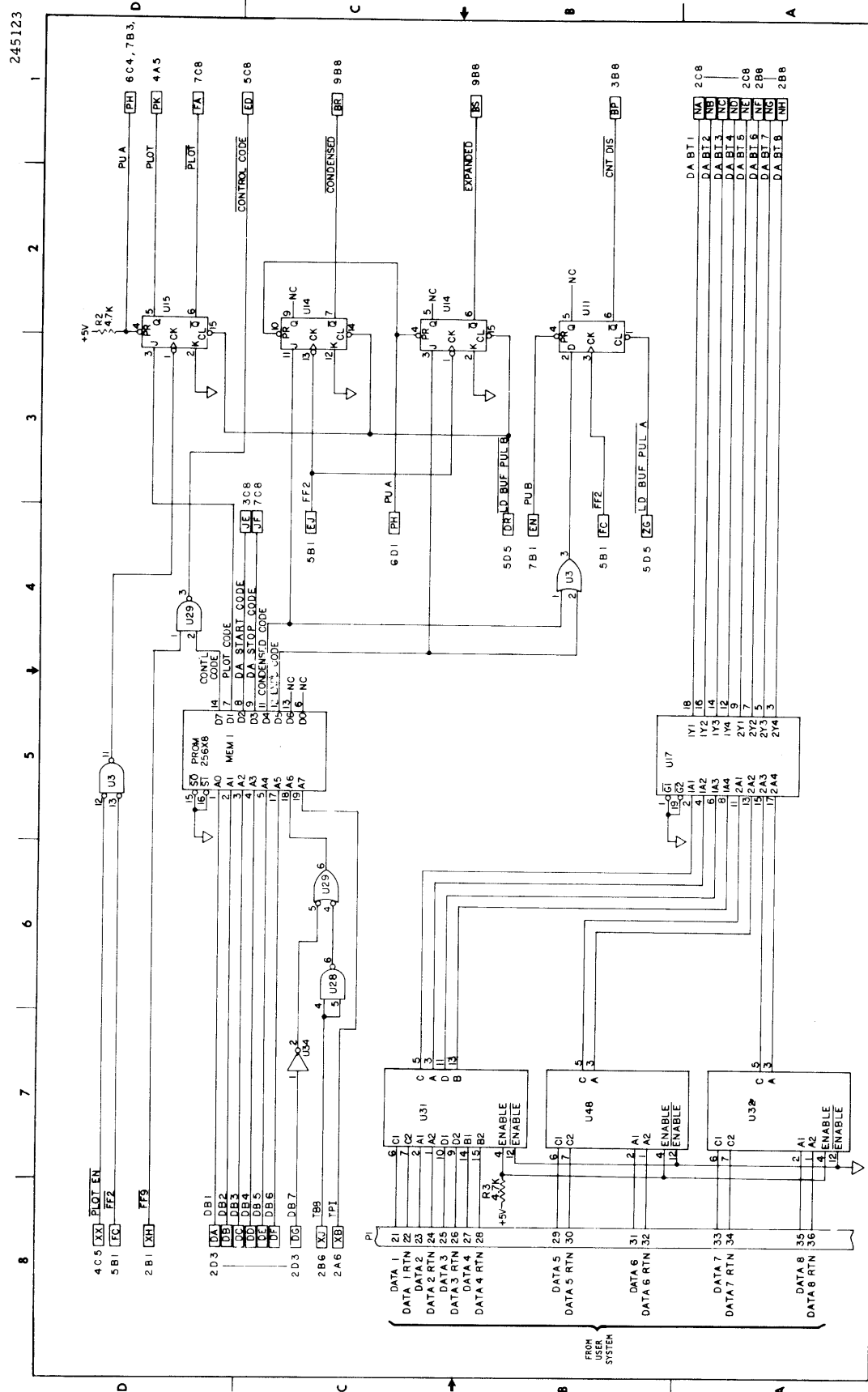


FIGURE 9-12 (SH 6 OF 9)
LOGIC DIAGRAM
DPC LONG-LINE INTERFACE
CCA

245123

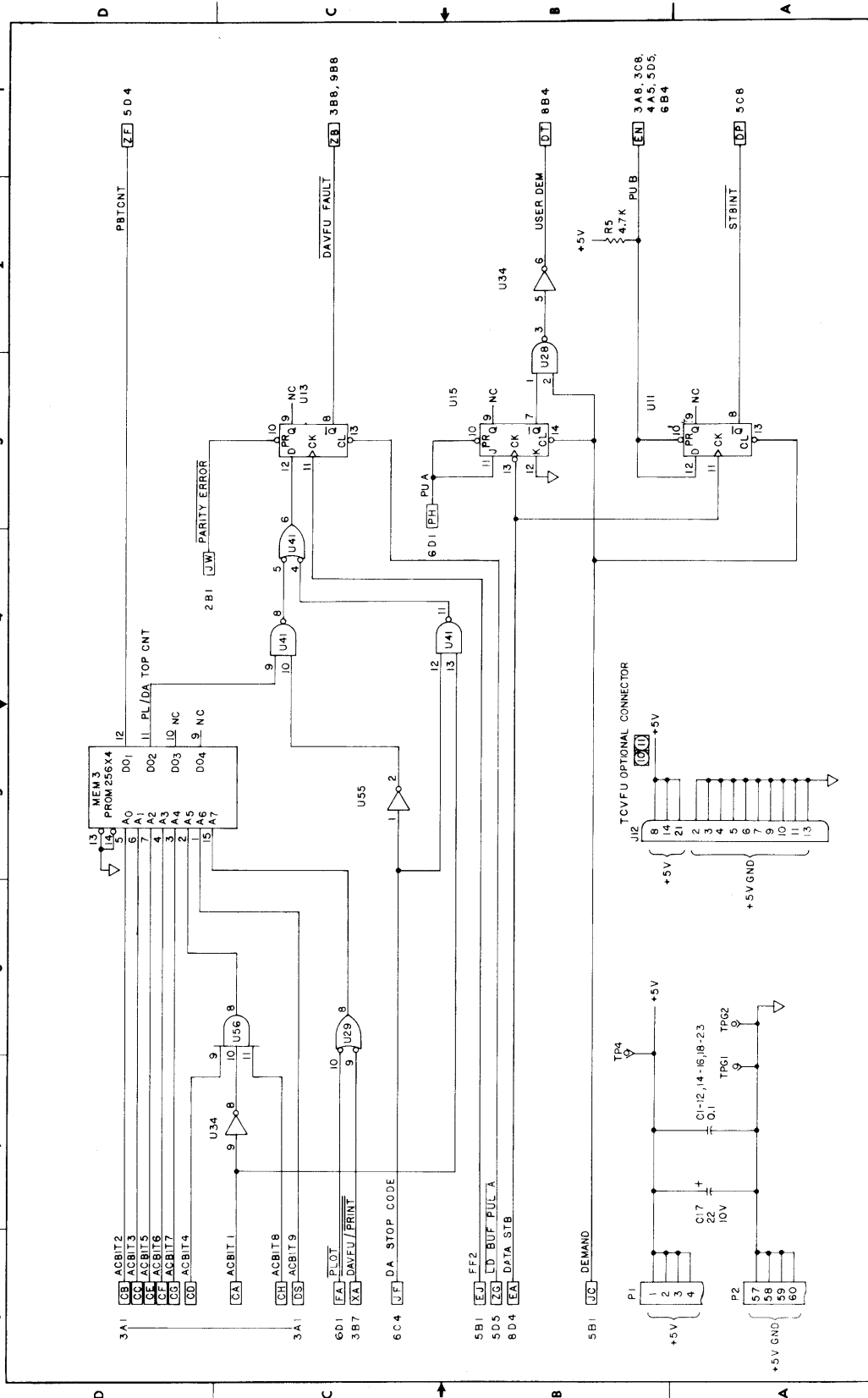


FIGURE 9-12 (SH 7 OF 9)
LOGIC DIAGRAM
DPC LONG-LINE INTERFACE
CCA

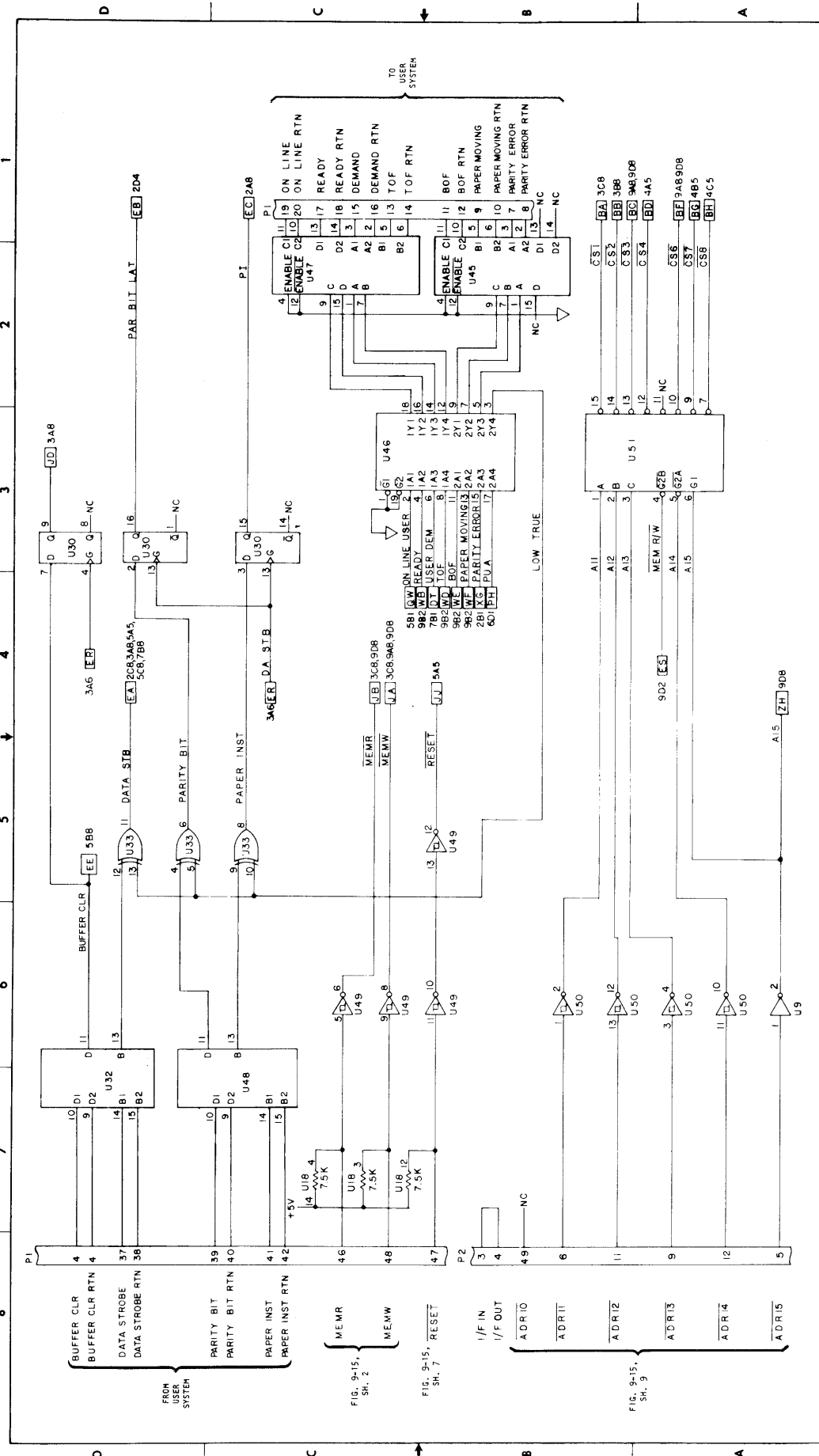
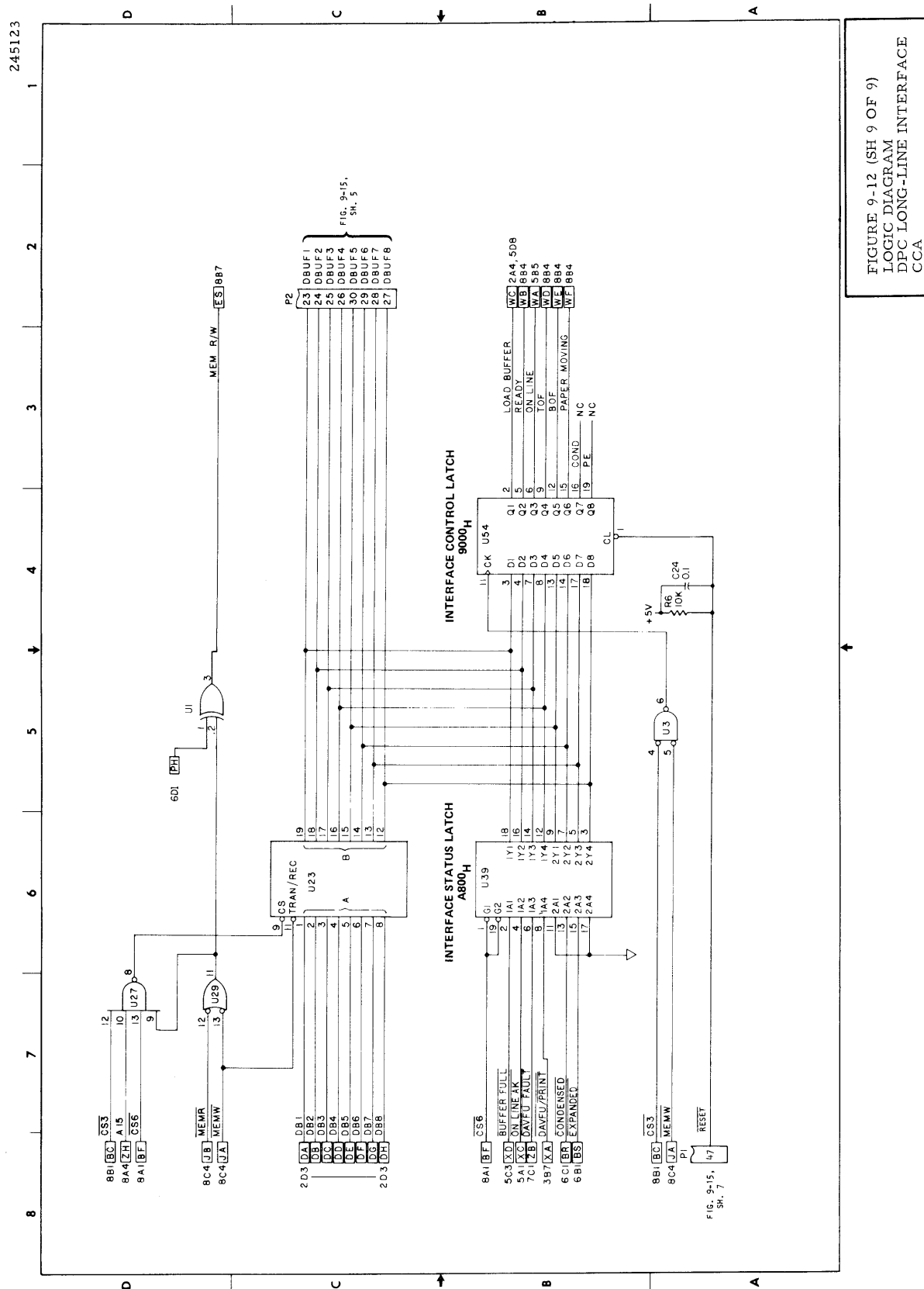
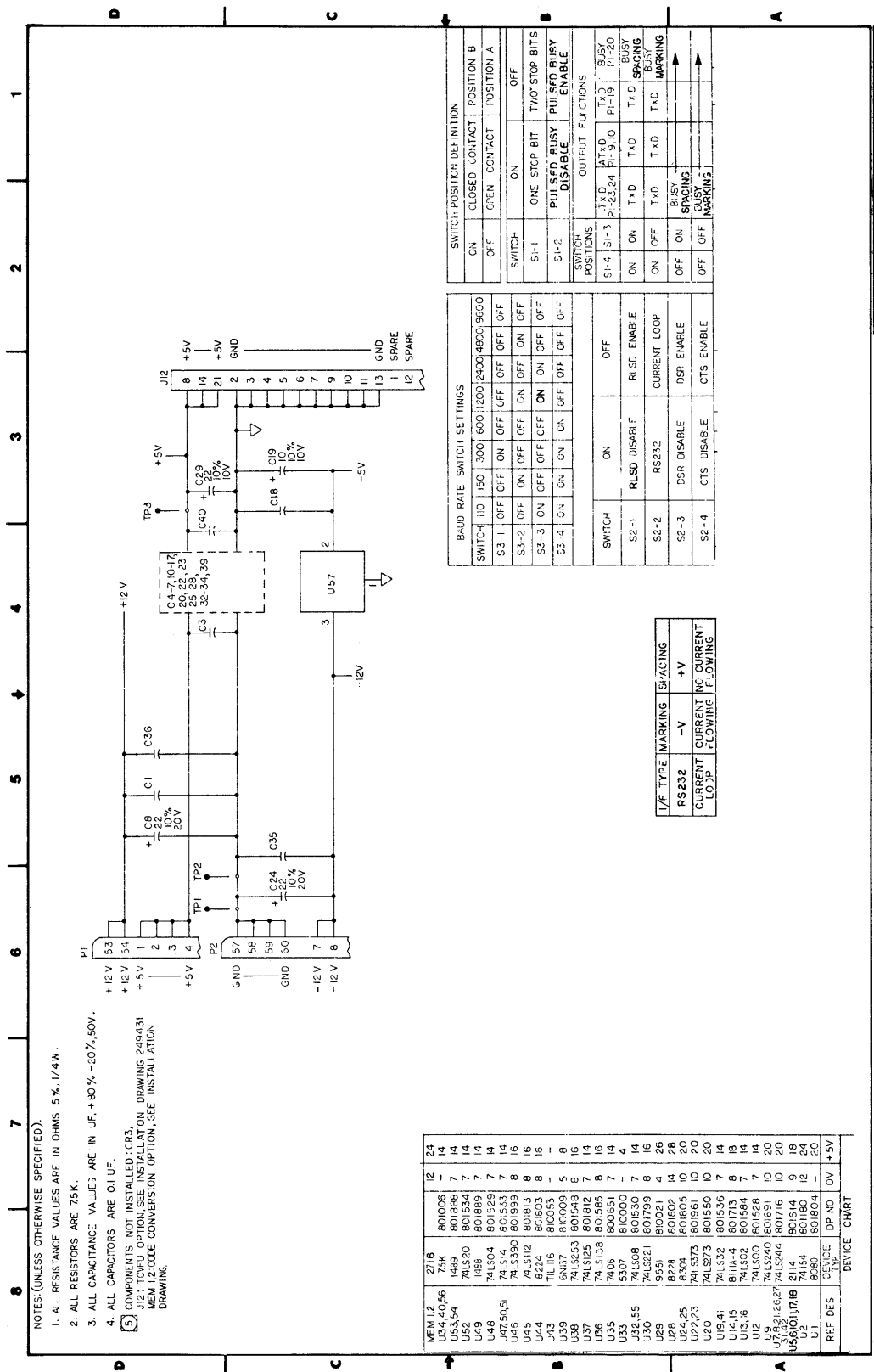


FIGURE 9-12 (SH 8 OF 9)
LOGIC DIAGRAM
DPC LONG-LINE INTERFACE
CCA





MODEL M200
FIGURE 9-13 (SH 1 OF 8)
LOGIC DIAGRAM
SERIAL INTERFACE CCA

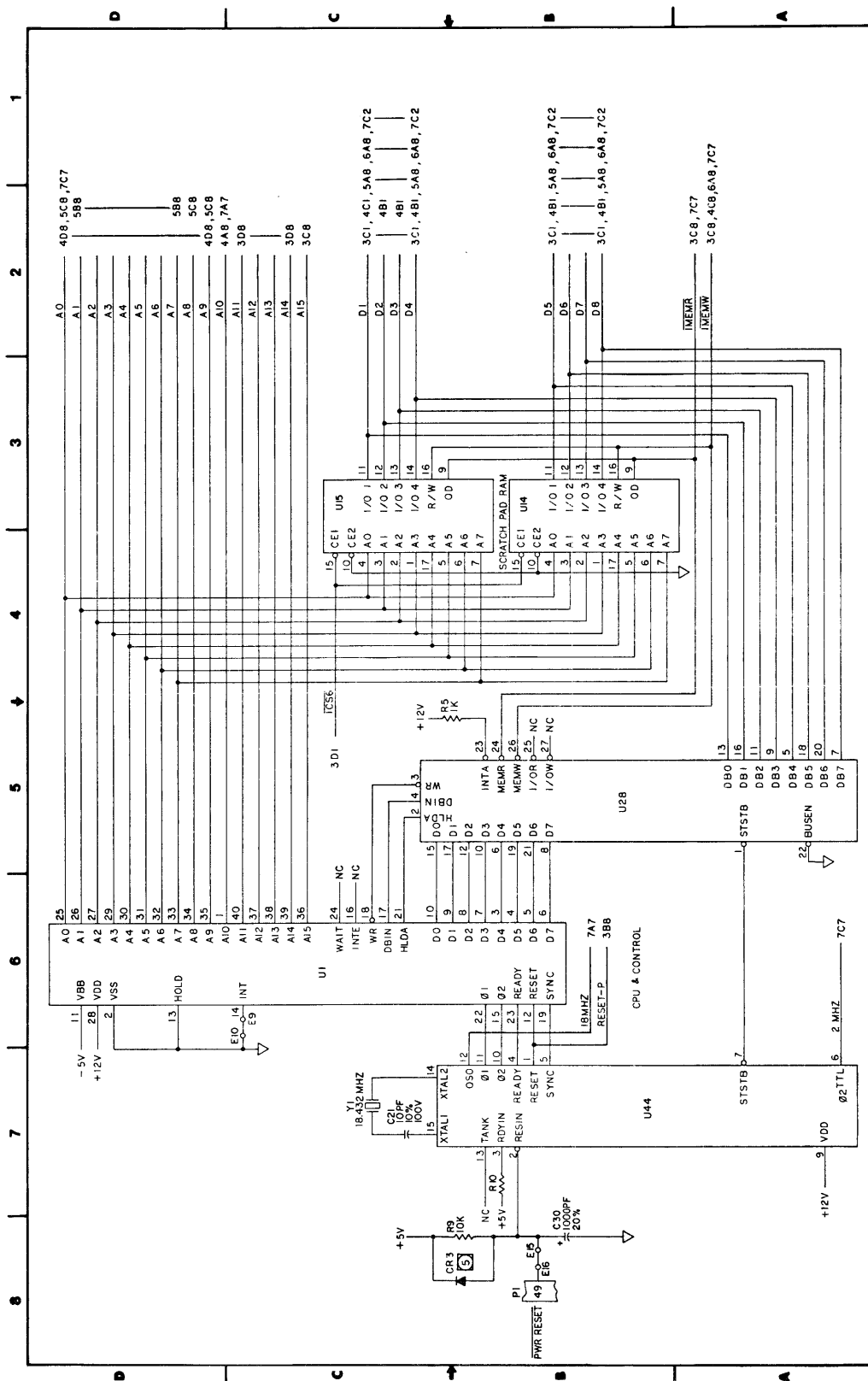
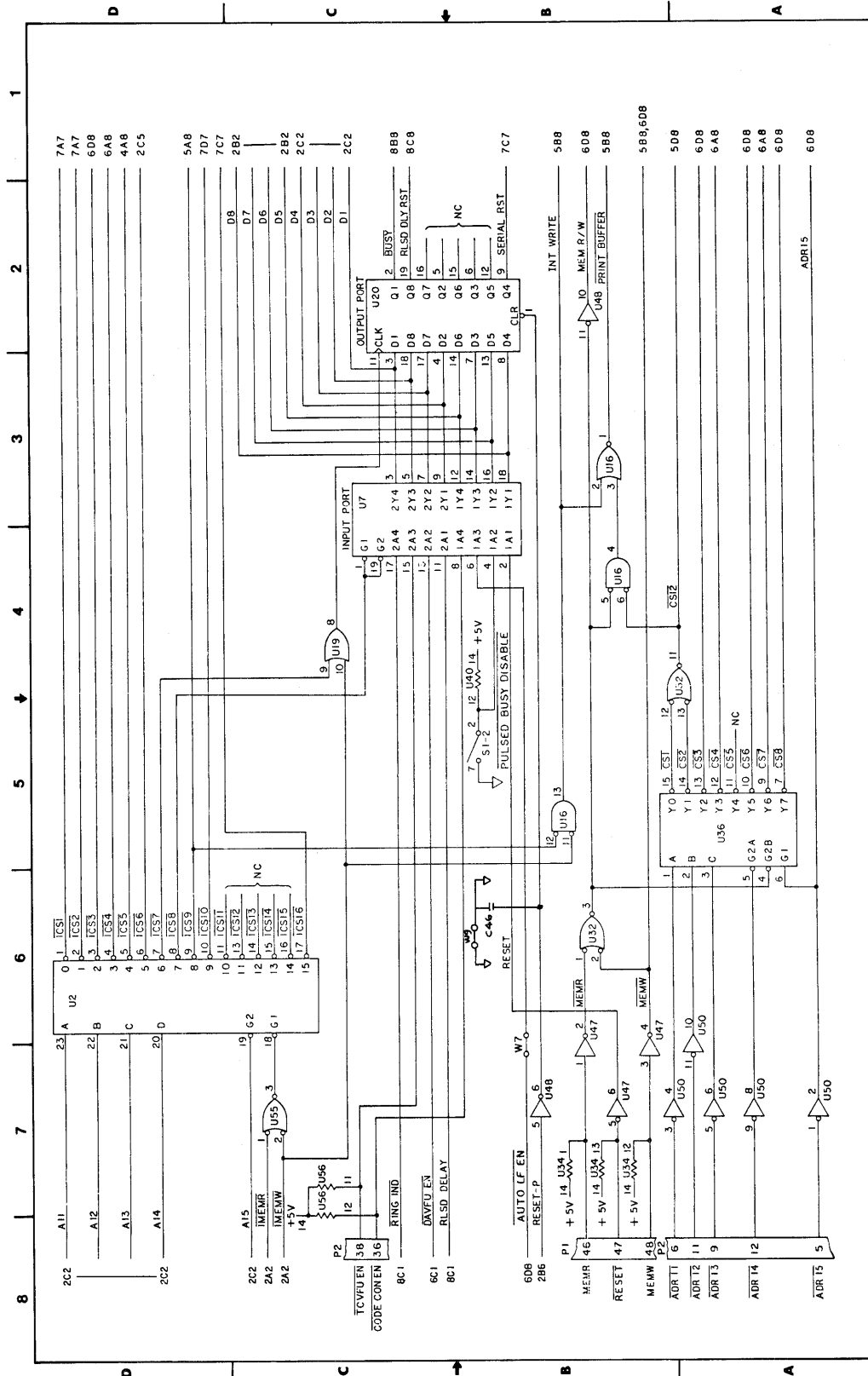
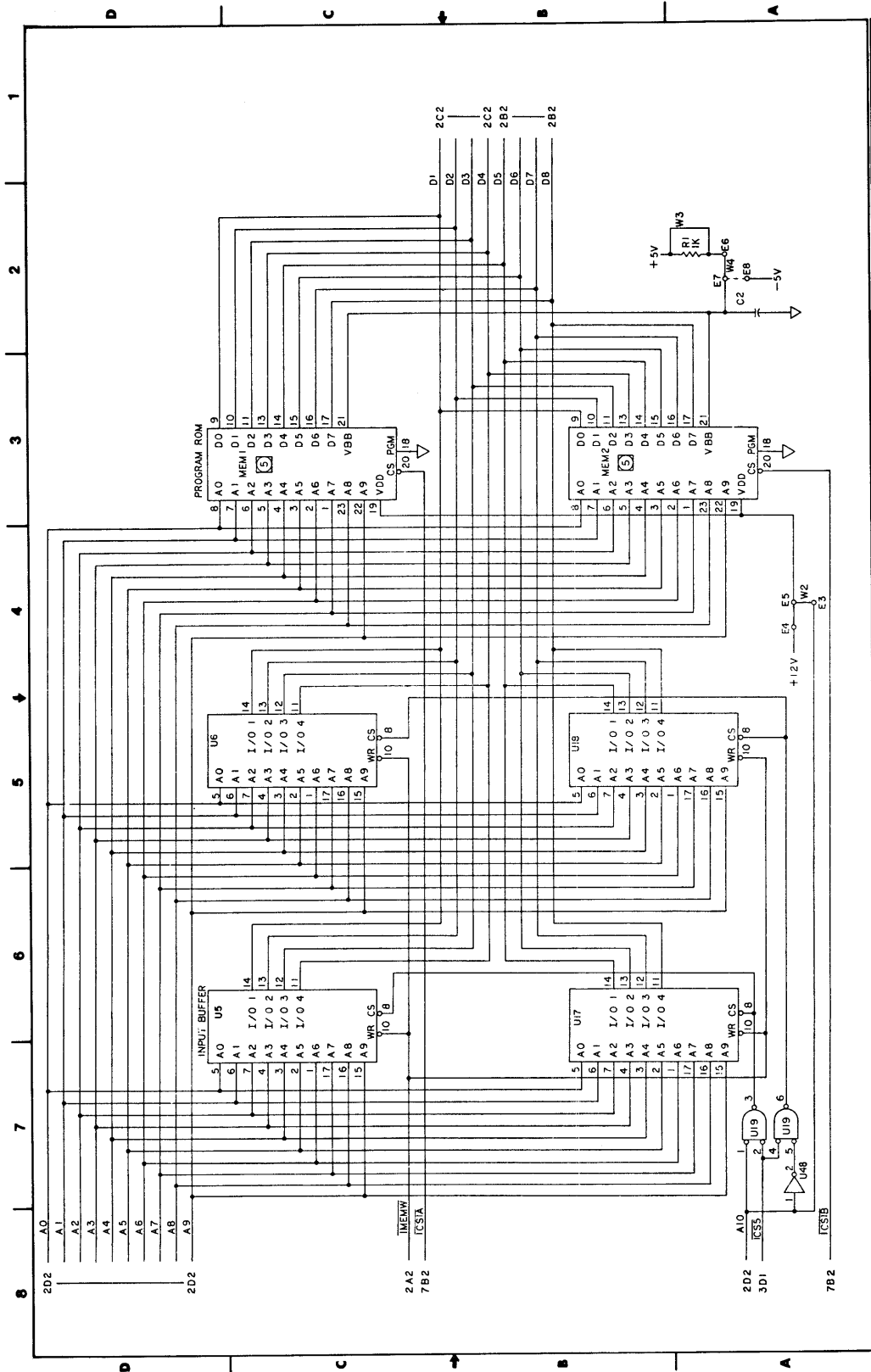


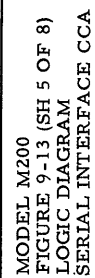
FIGURE 9-13 (SH 2 OF 8)
LOGIC DIAGRAM
SERIAL INTERFACE CCA

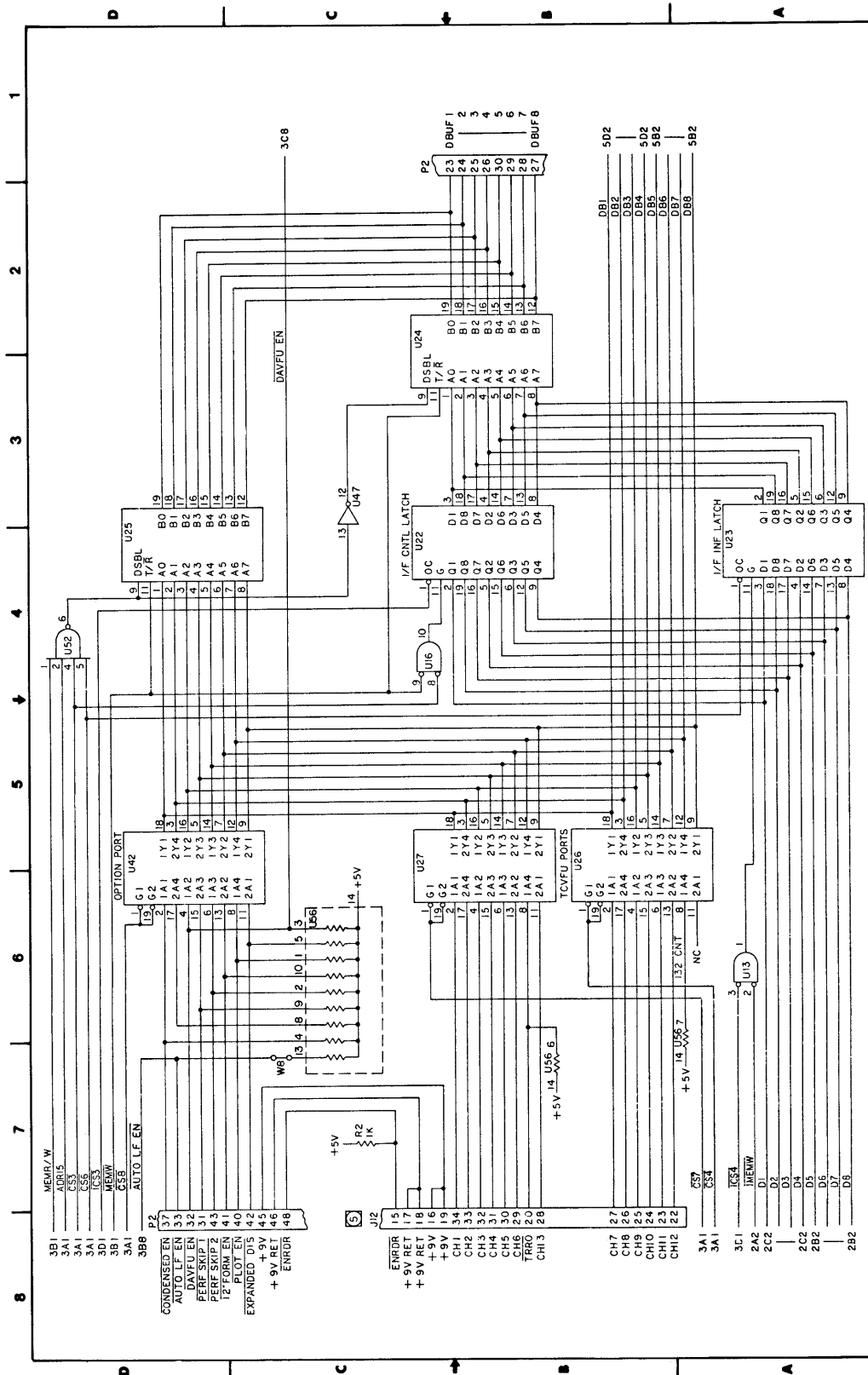


MODEL M200
FIGURE 9-13 (SH 3 OF 8)
LOGIC DIAGRAM
SERIAL INTERFACE CCA

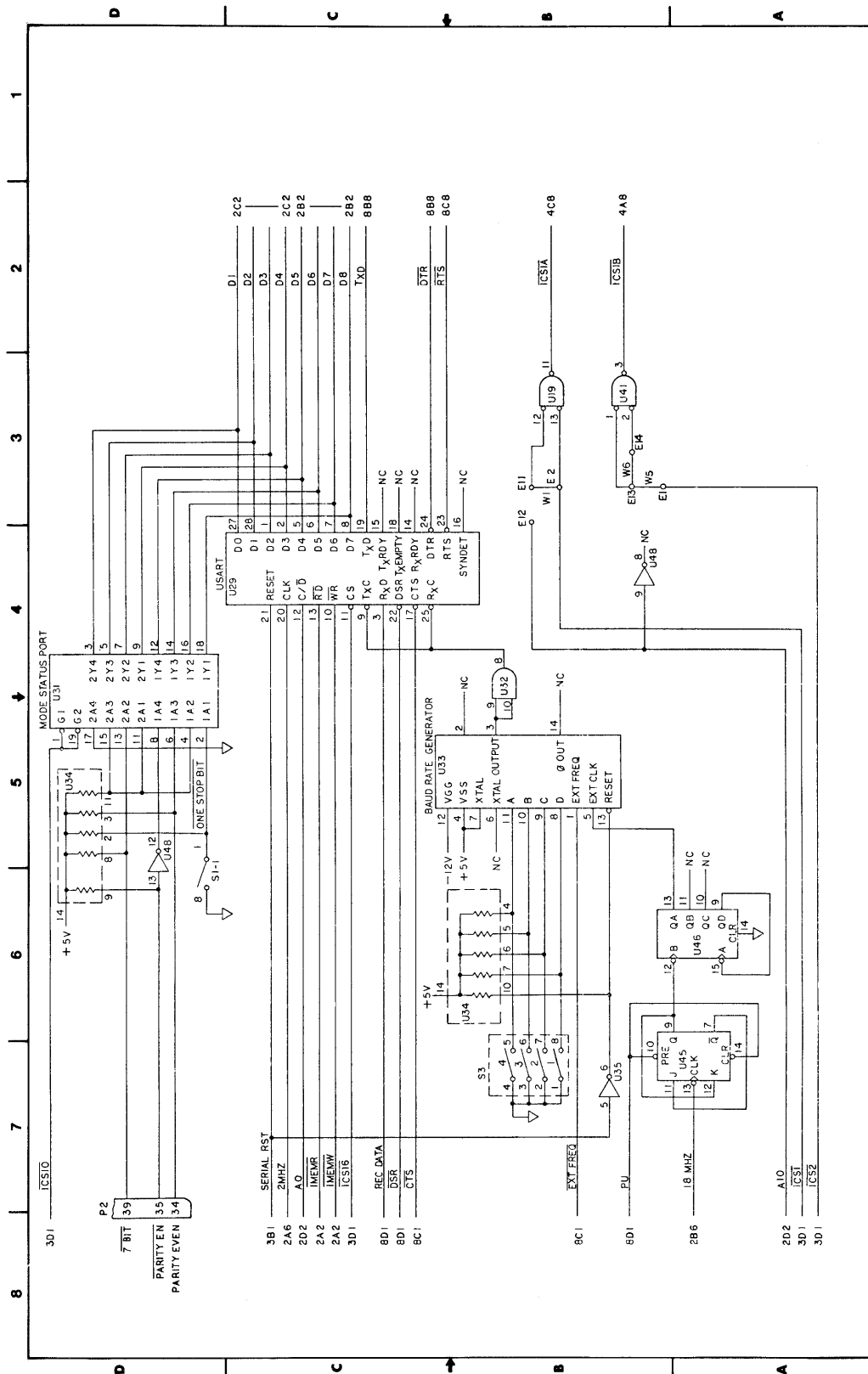


MODEL M200
FIGURE 9-13 (SH 4 OF 8)
LOGIC DIAGRAM
SERIAL INTERFACE CCA

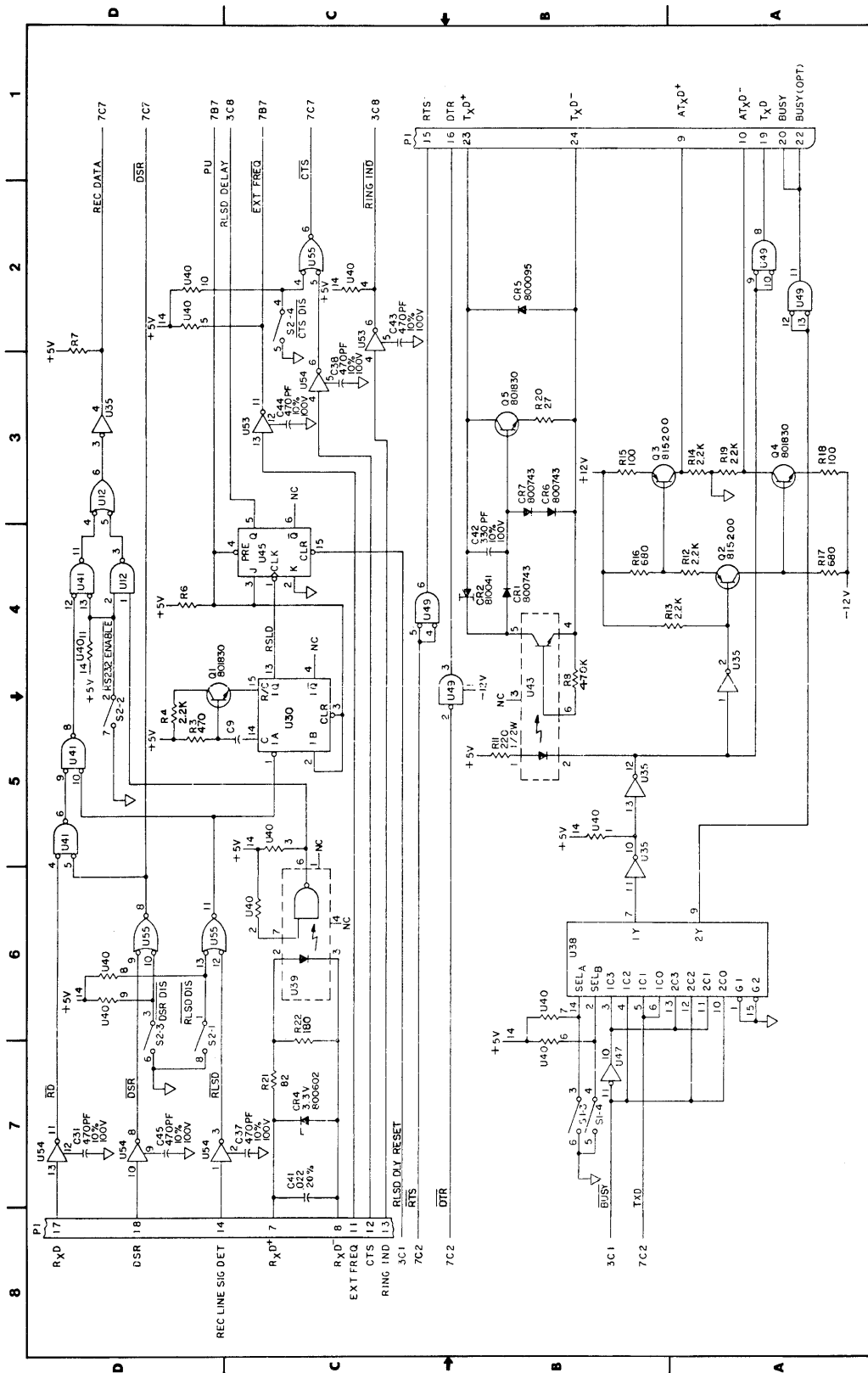




MODEL M200
FIGURE 9-13 (SH 6 OF 8)
LOGIC DIAGRAM
SERIAL INTERFACE CCA

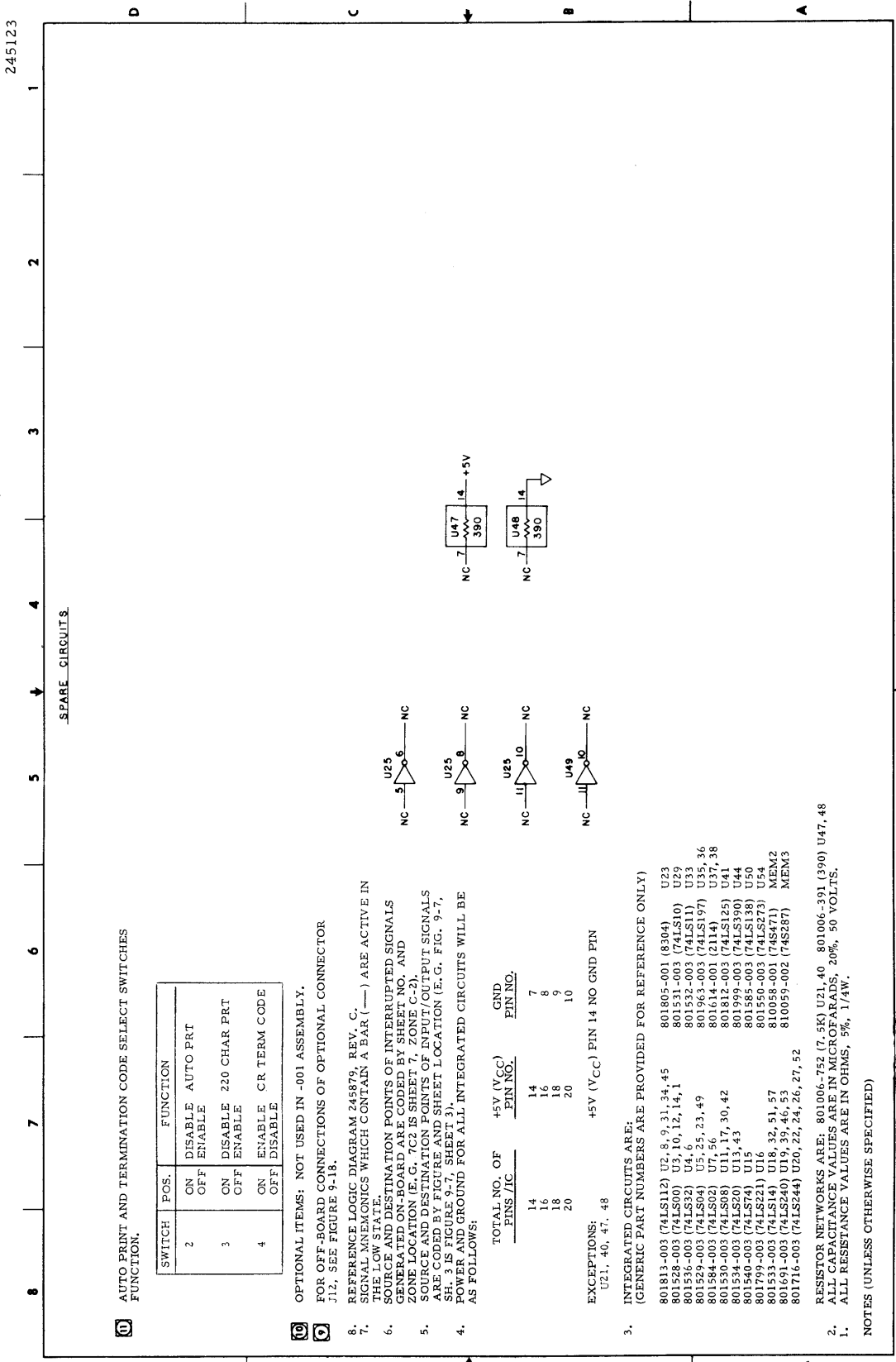


MODEL M200
FIGURE 9-13 (SH 7 OF 8)
LOGIC DIAGRAM
SERIAL INTERFACE CCA



MODEL M200
FIGURE 9-13 (SH 8 OF 8)
LOGIC DIAGRAM
SERIAL INTERFACE CCA

FIGURE 9-14 (SH 1 OF 9)
LOGIC DIAGRAM
DPC CENTRONICS-COMPATIBLE
INTERFACE CCA



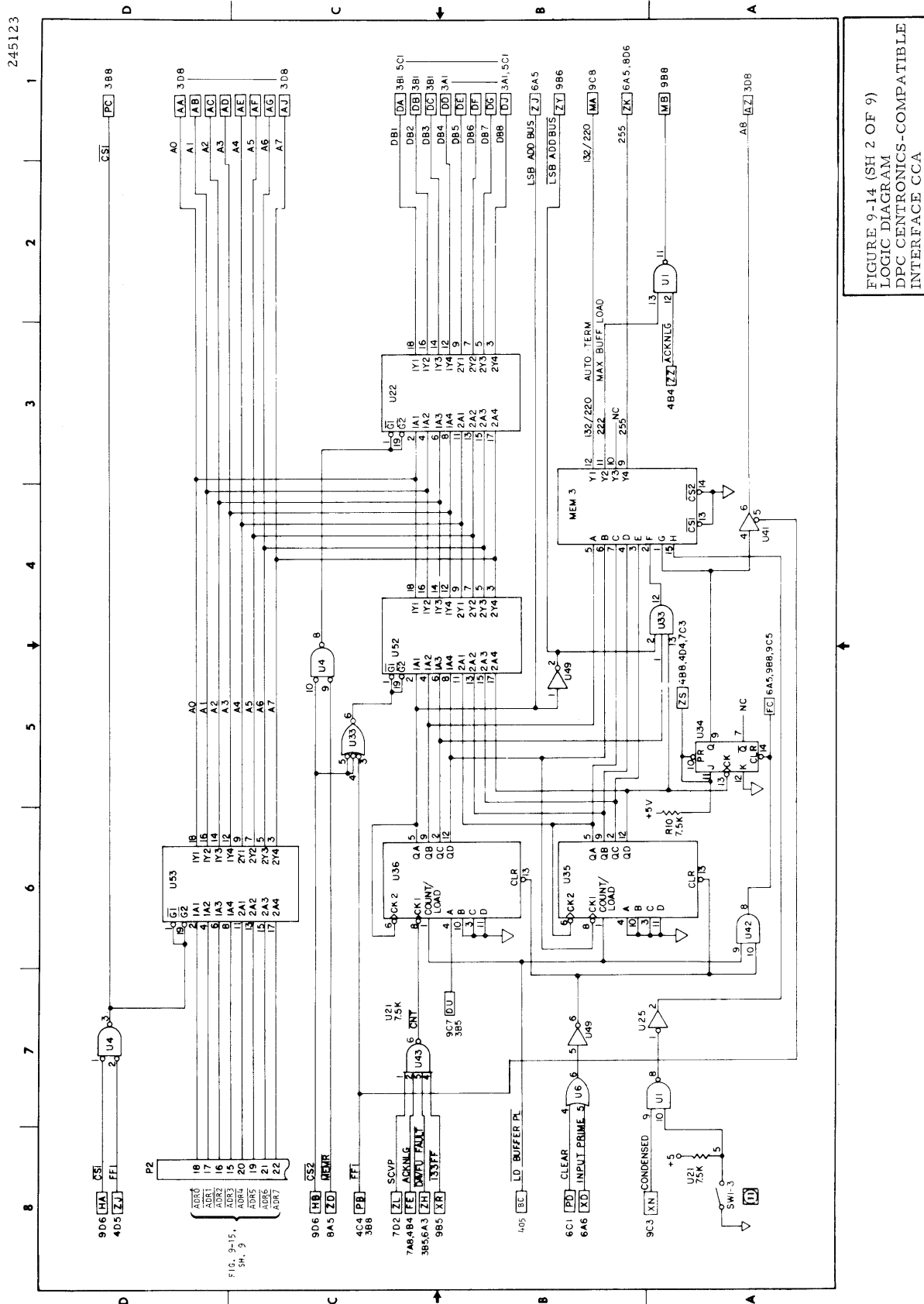


FIGURE 9-14 (SH 2 OF 9)
LOGIC DIAGRAM
DPC CENTRONICS-COMPATIBLE
INTERFACE CCA

245123

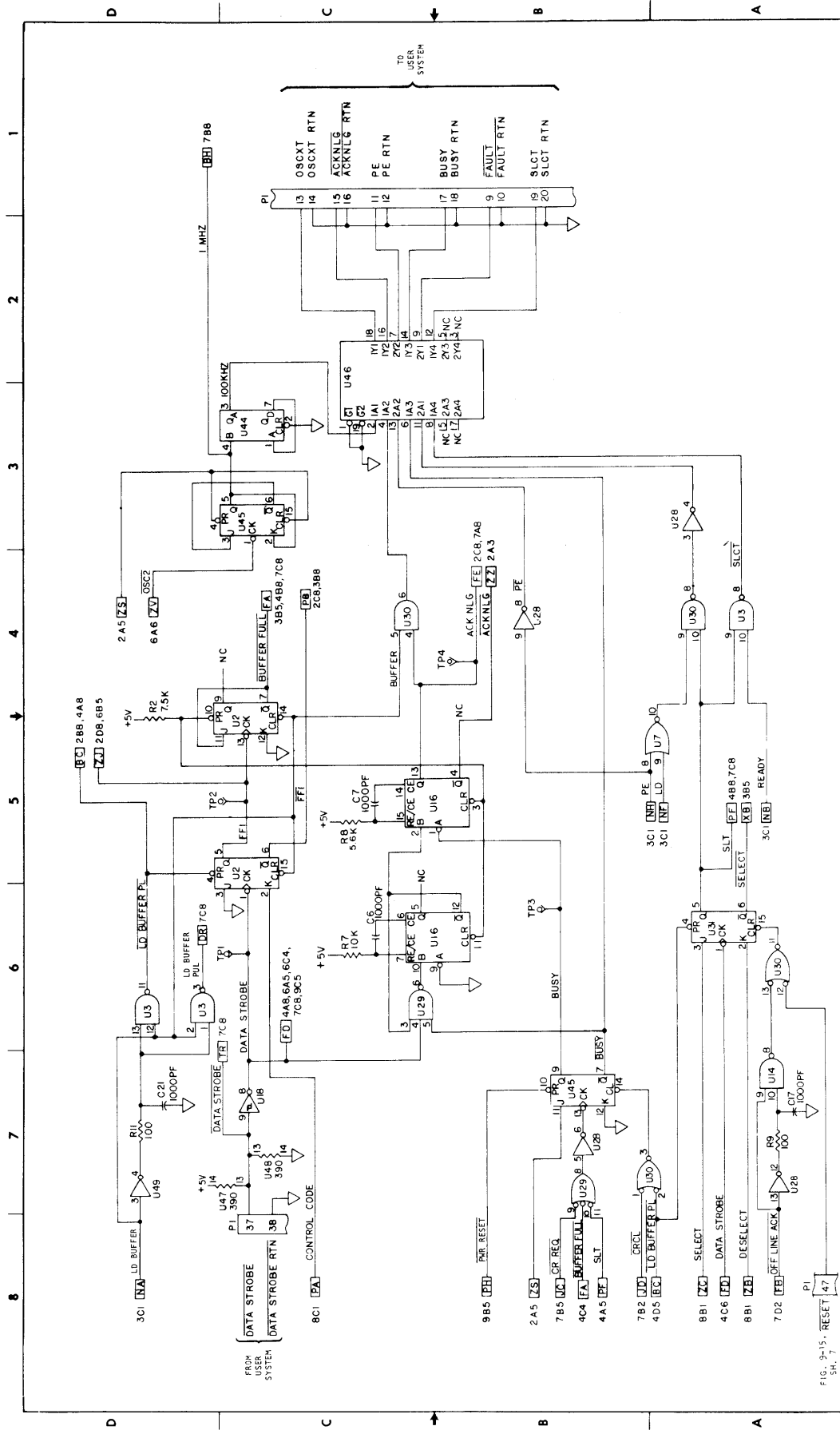


FIG. 9-15, RESET 47

FIGURE 9-14 (SH 4 OF 9)
LOGIC DIAGRAM
DPIC CENTRONICS-COMPATIBLE
INTERFACE CCA

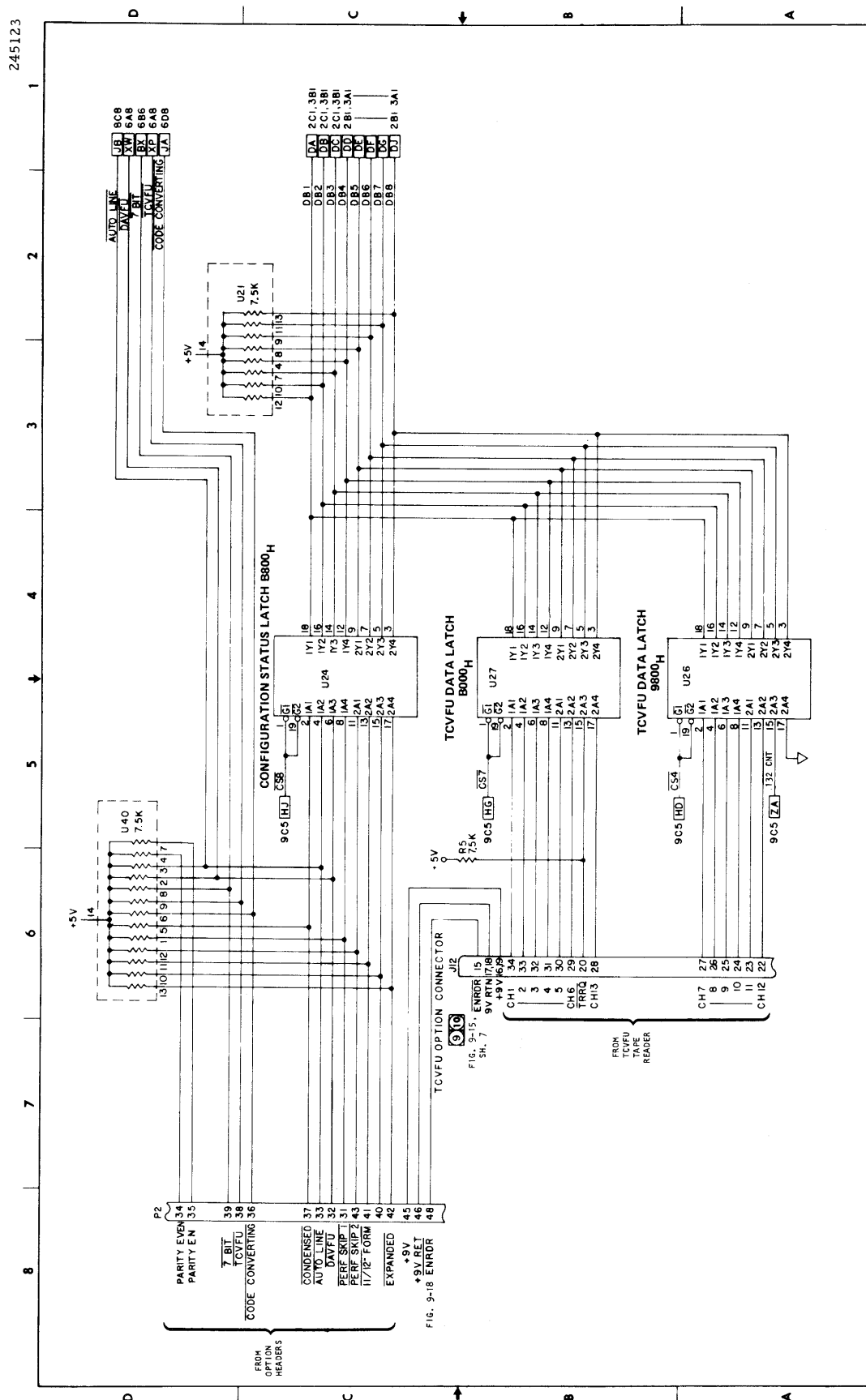


FIGURE 9-14 (SH 5 OF 9)
LOGIC DIAGRAM
DPC CENTRONICS-COMPATIBLE
INTERFACE CCA

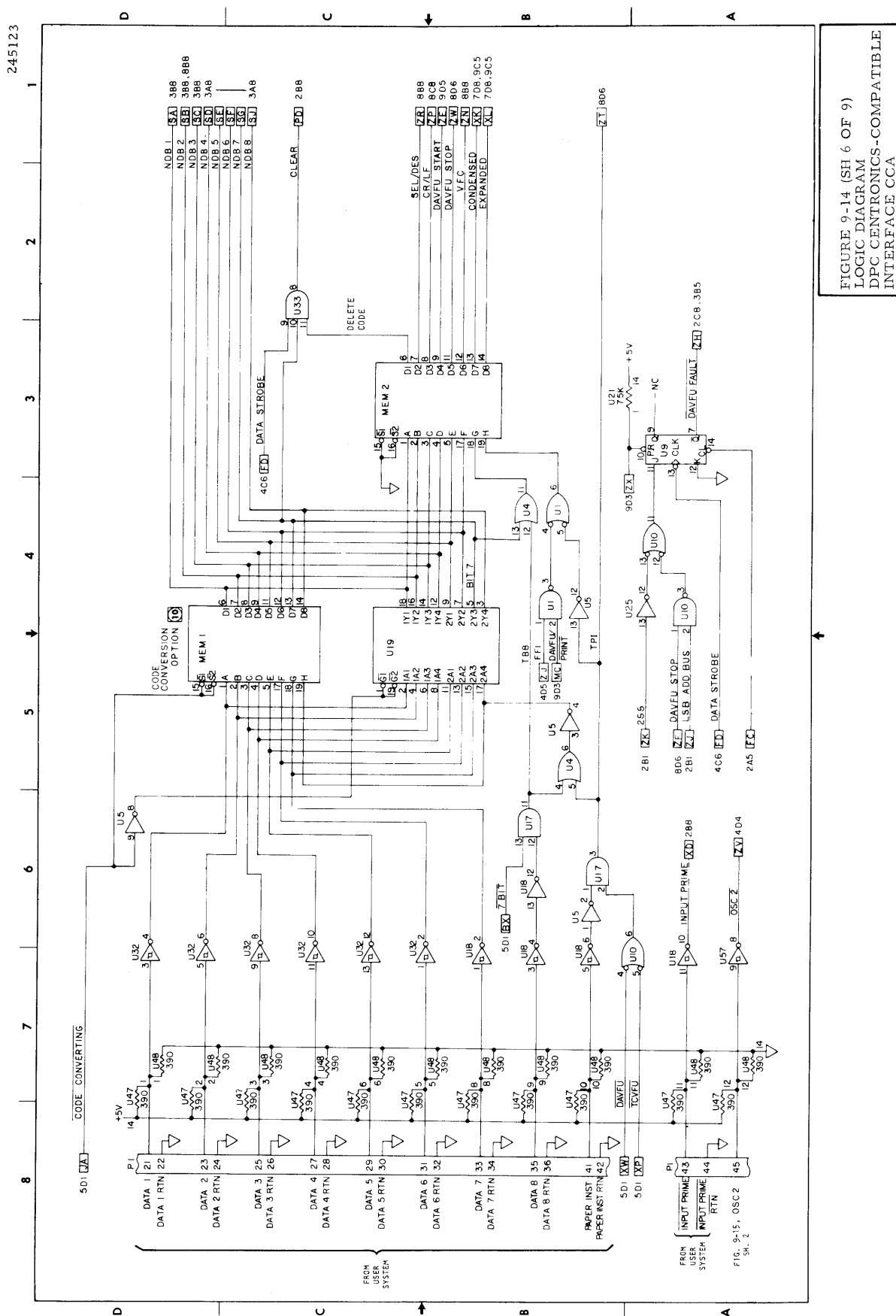


FIGURE 9-14 (SH 6 OF 9)
LOGIC DIAGRAM
DPC CENTRONICS-COMPATIBLE
INTERFACE CCA

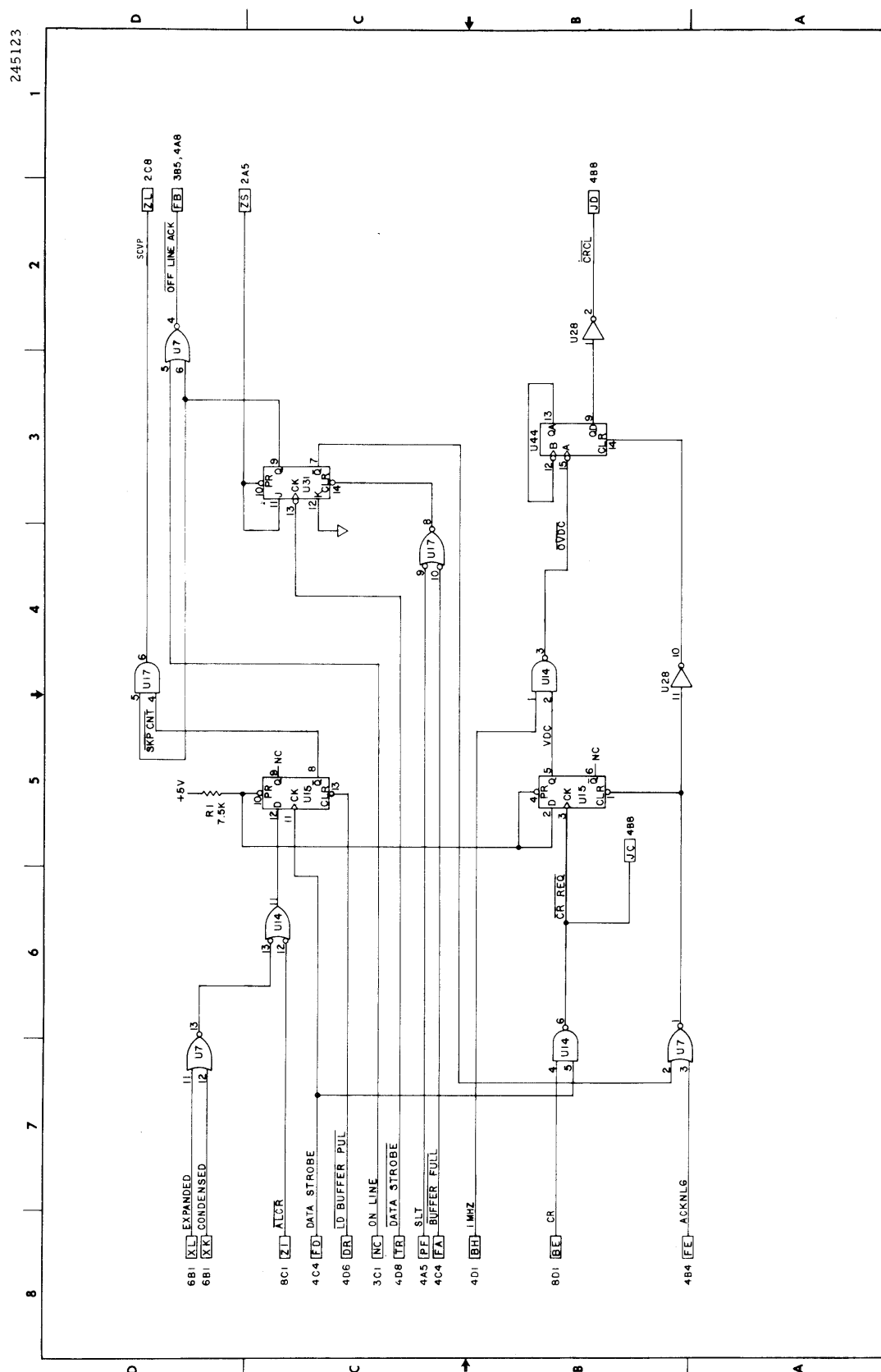


FIGURE 9-14 (SH 7 OF 9)
LOGIC DIAGRAM
DPC CENTRONICS-COMPATIBLE
INTERFACE CCA

245123

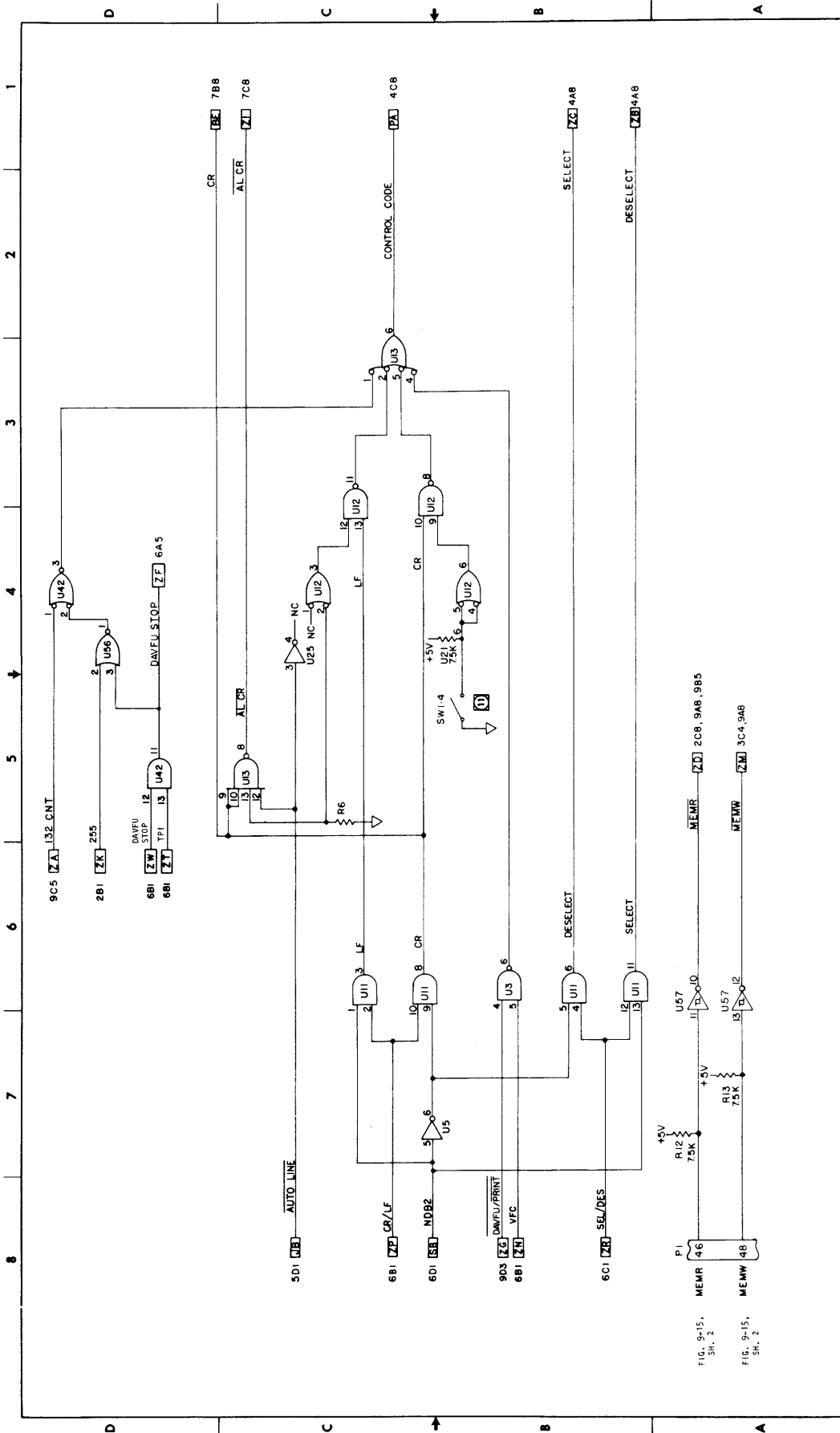


FIGURE 9-14 (SH 8 OF 9)
LOGIC DIAGRAM
DPC CENTRONICS-COMPATIBLE
INTERFACE CCA

245123

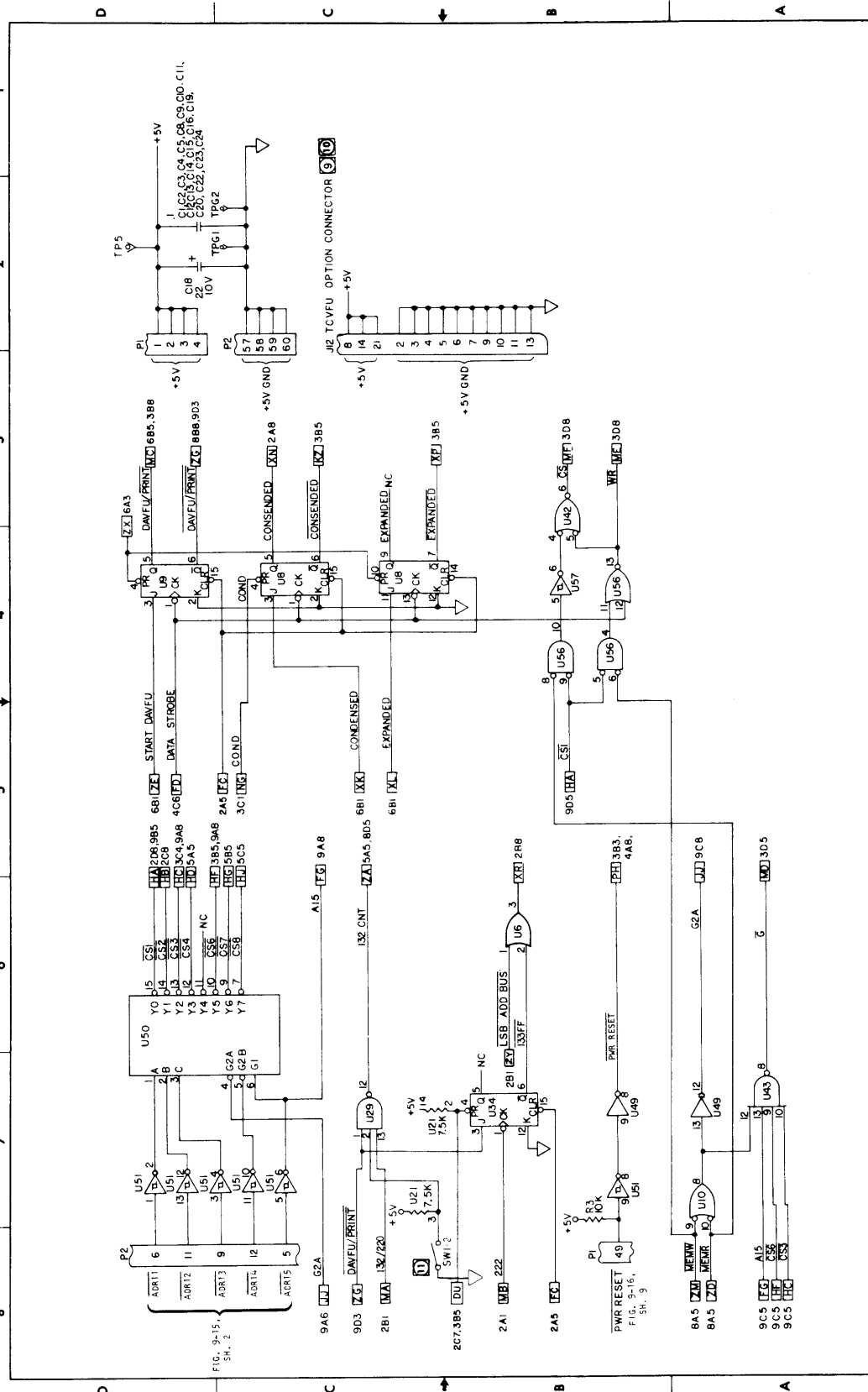
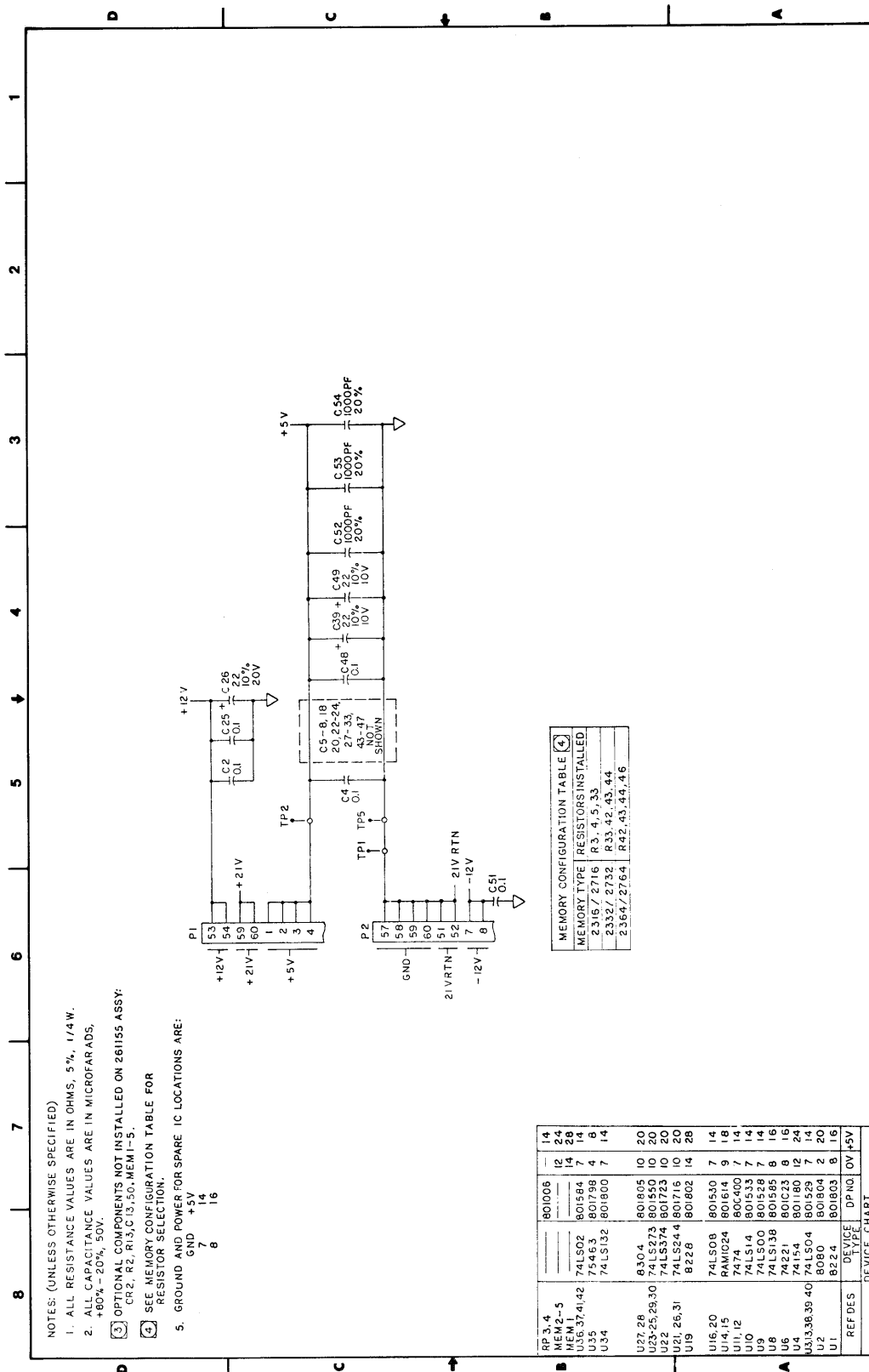
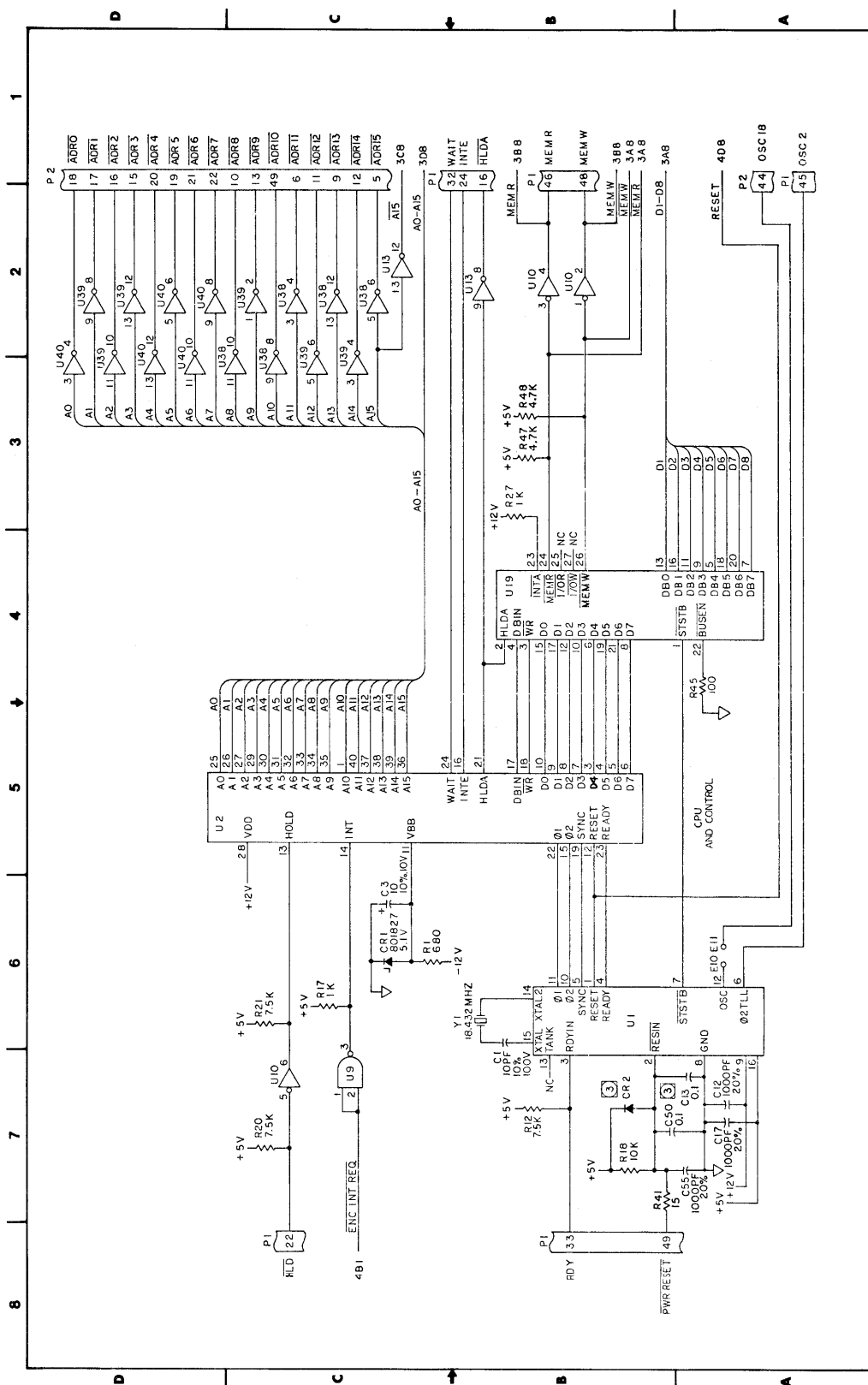


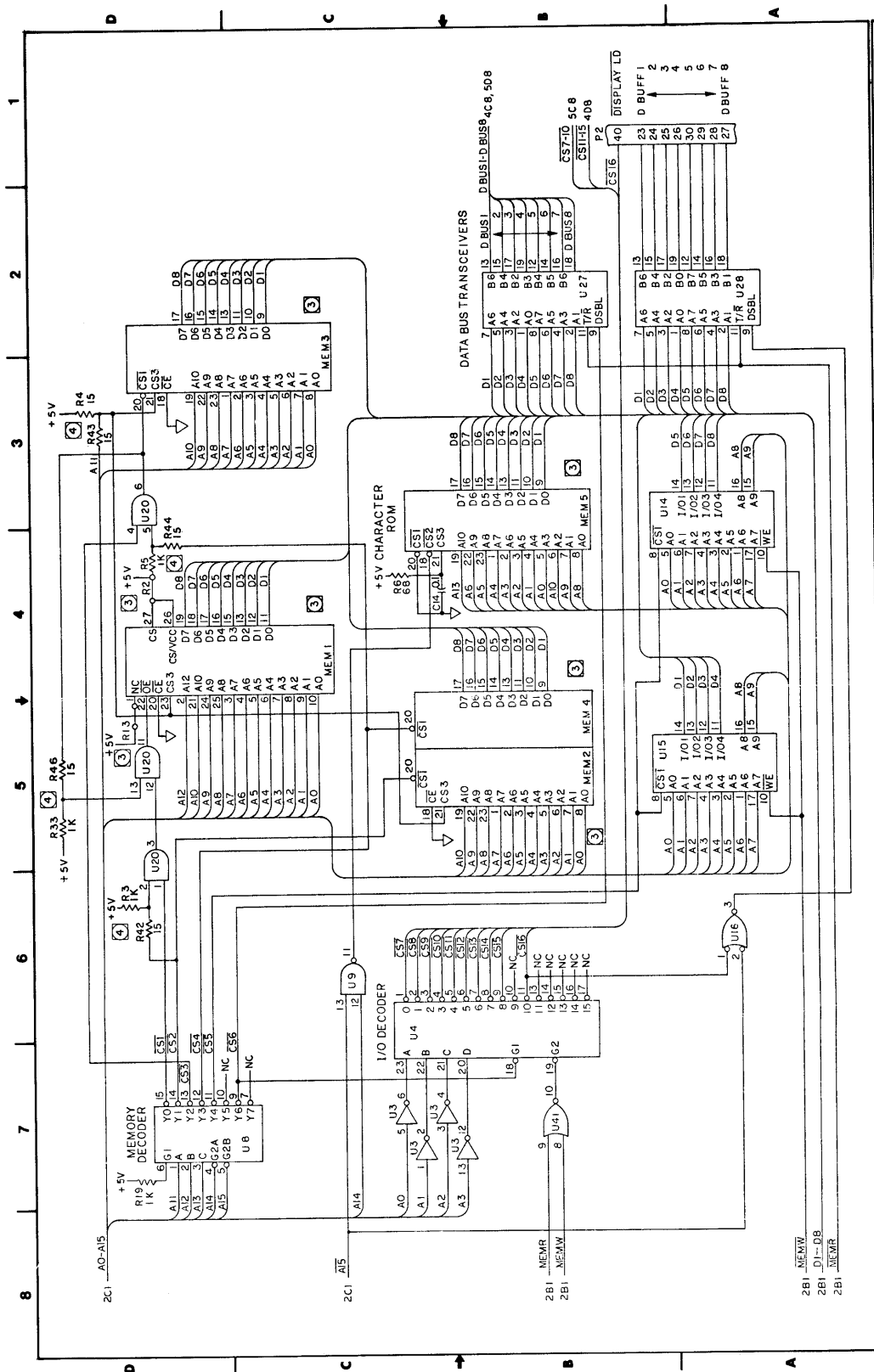
FIGURE 9-14 (SH 9 OF 9)
LOGIC DIAGRAM
DPC CENTRONICS-COMPATIBLE
INTERFACE CCA



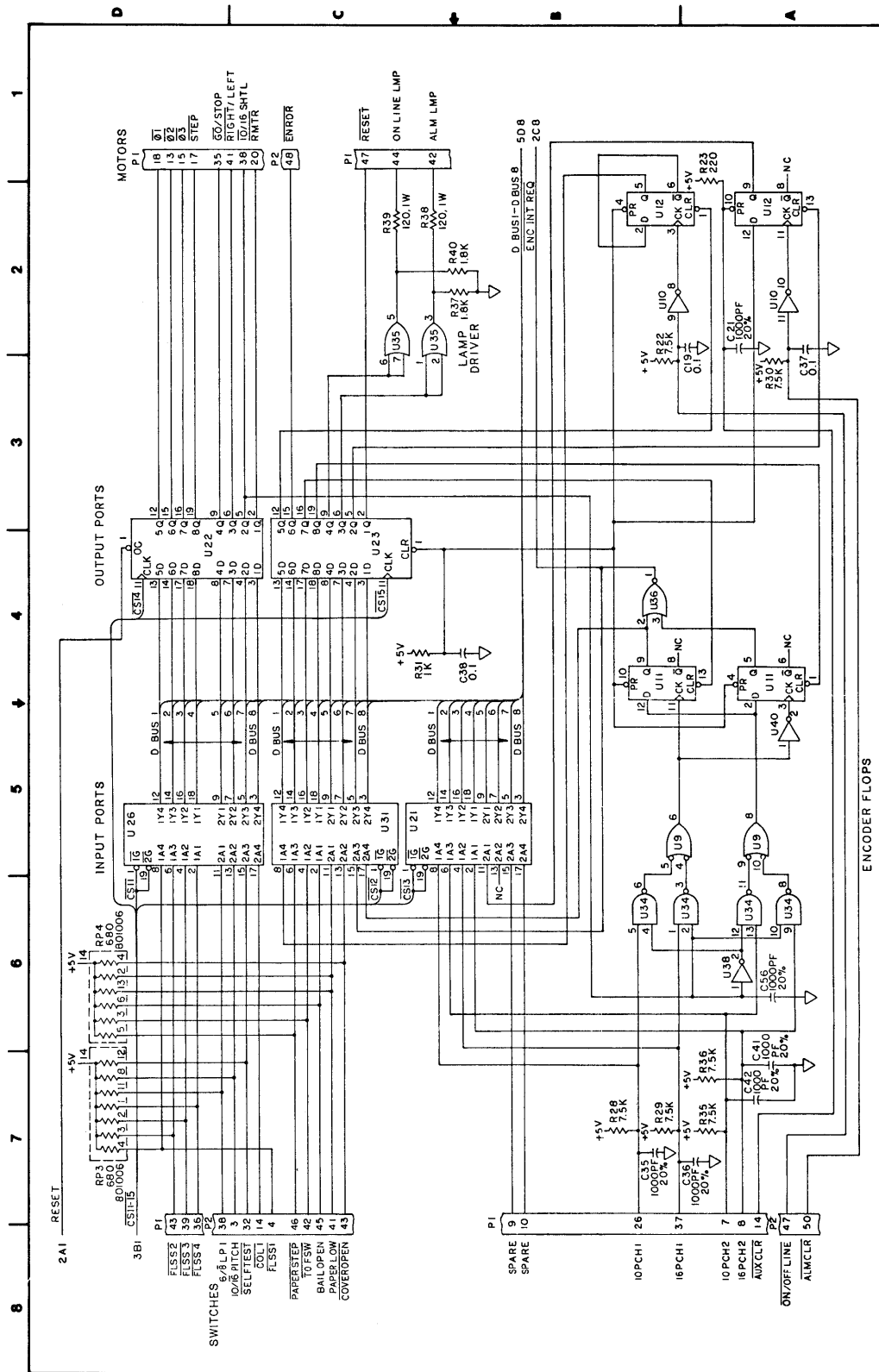
MODEL M200
FIGURE 9-15 (SH 1 OF 5)
LOGIC DIAGRAM
PROCESSOR CCA



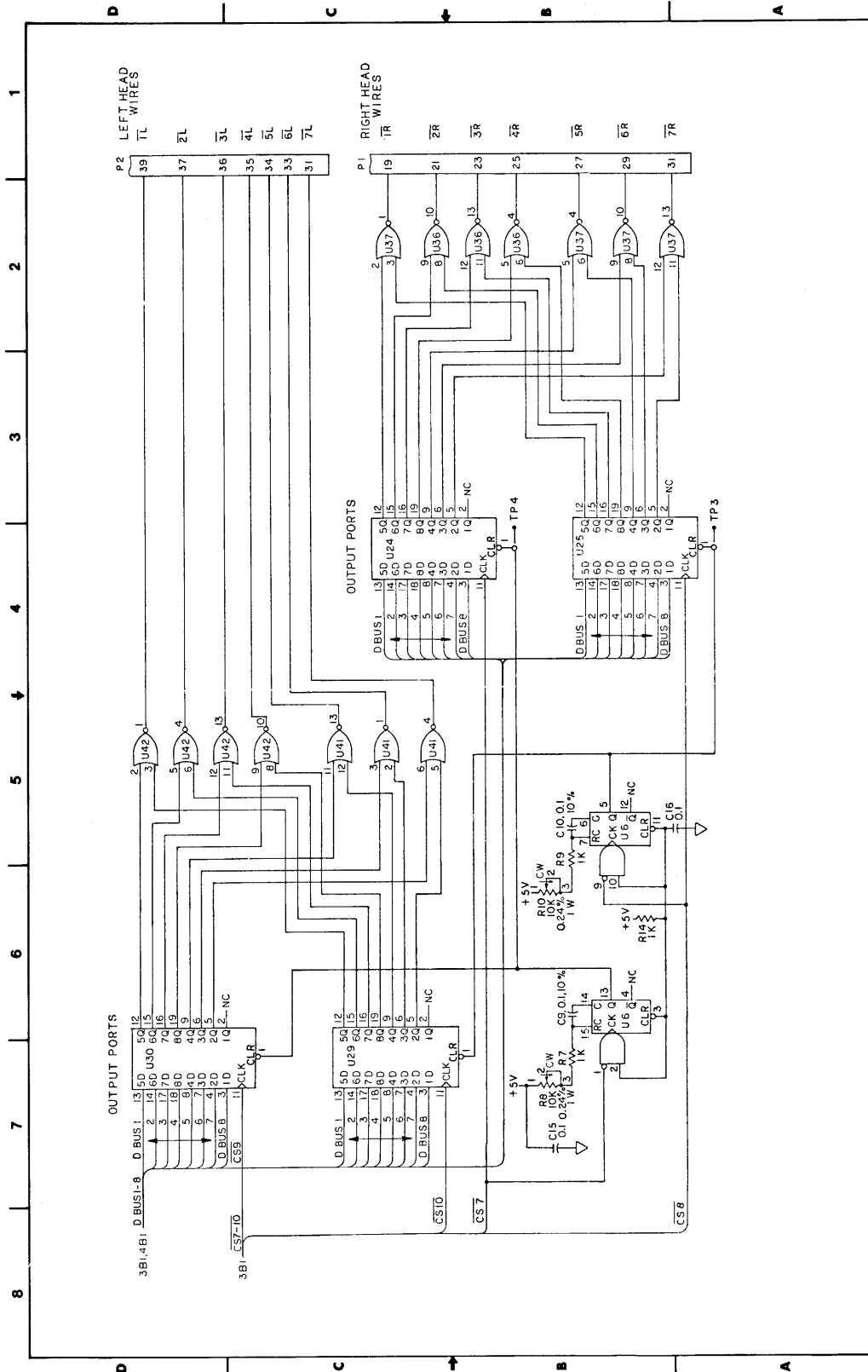
MODEL M200
FIGURE 9-15 (SH 2 OF 5)
LOGIC DIAGRAM
PROCESSOR CCA



MODEL M200
FIGURE 9-15 (SH 3 OF 5)
LOGIC DIAGRAM
PROCESSOR CCA

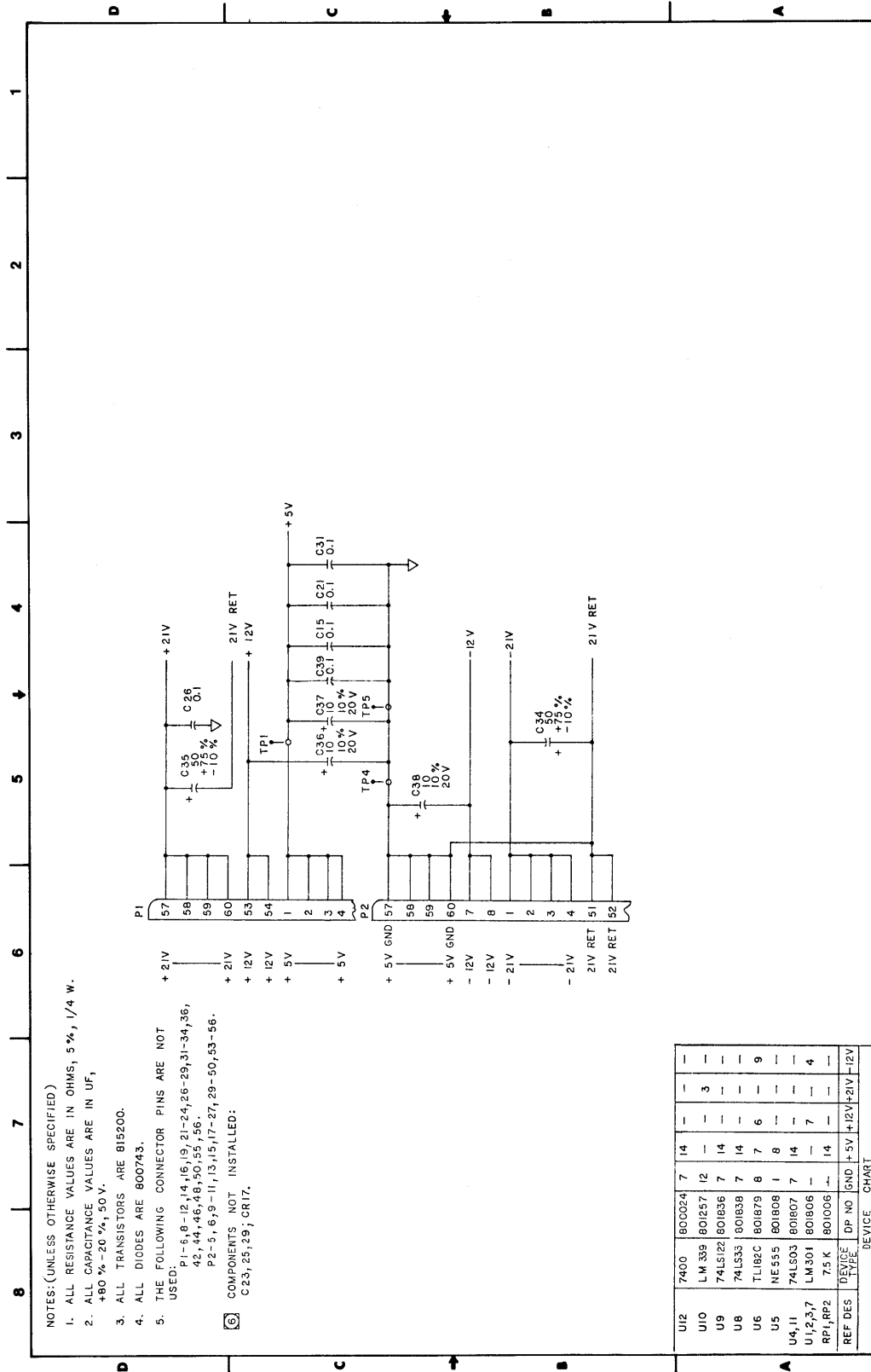


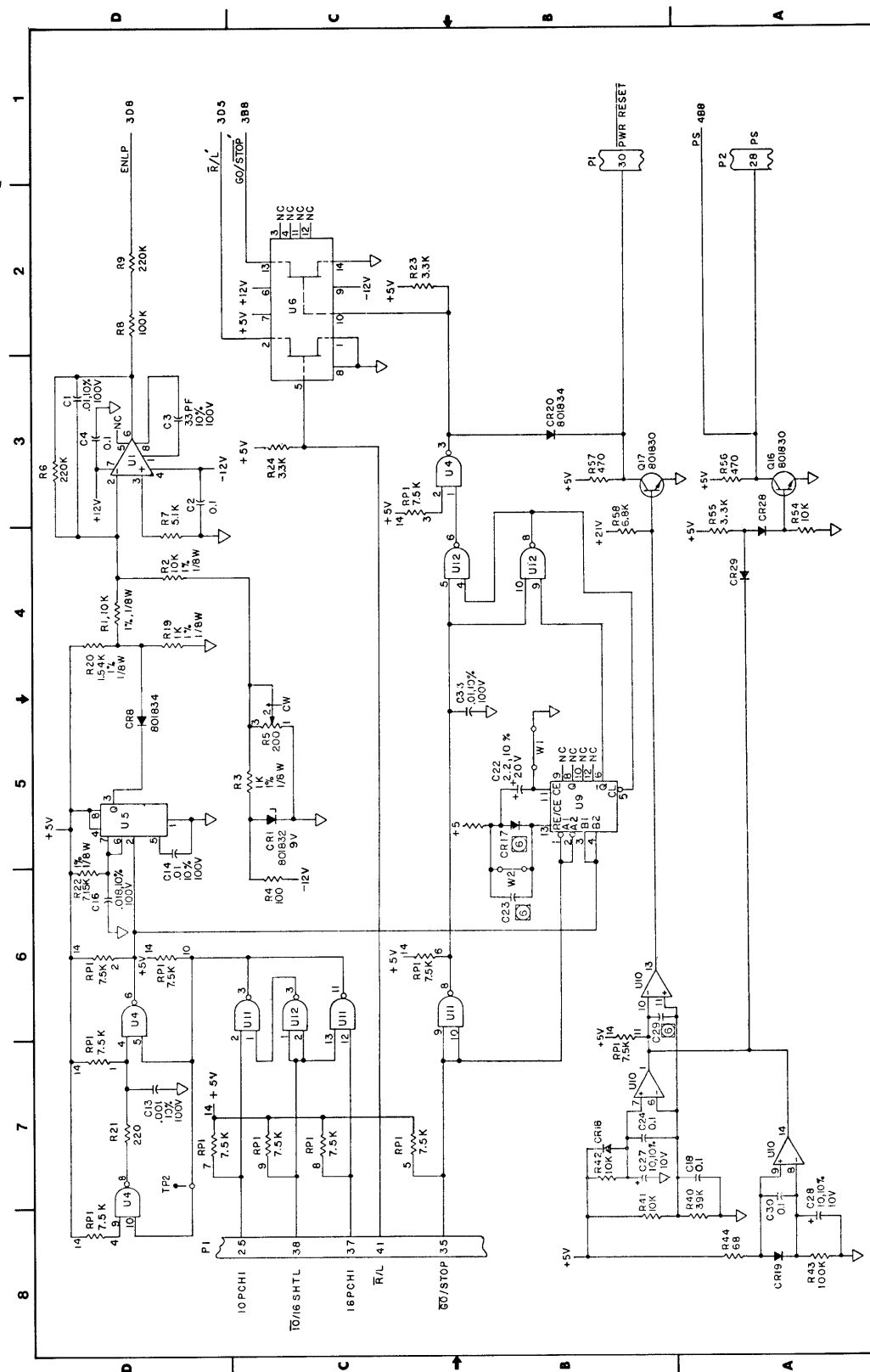
MODEL M200
FIGURE 9-15 (SH 4 OF 5)
LOGIC DIAGRAM
PROCESSOR CCA



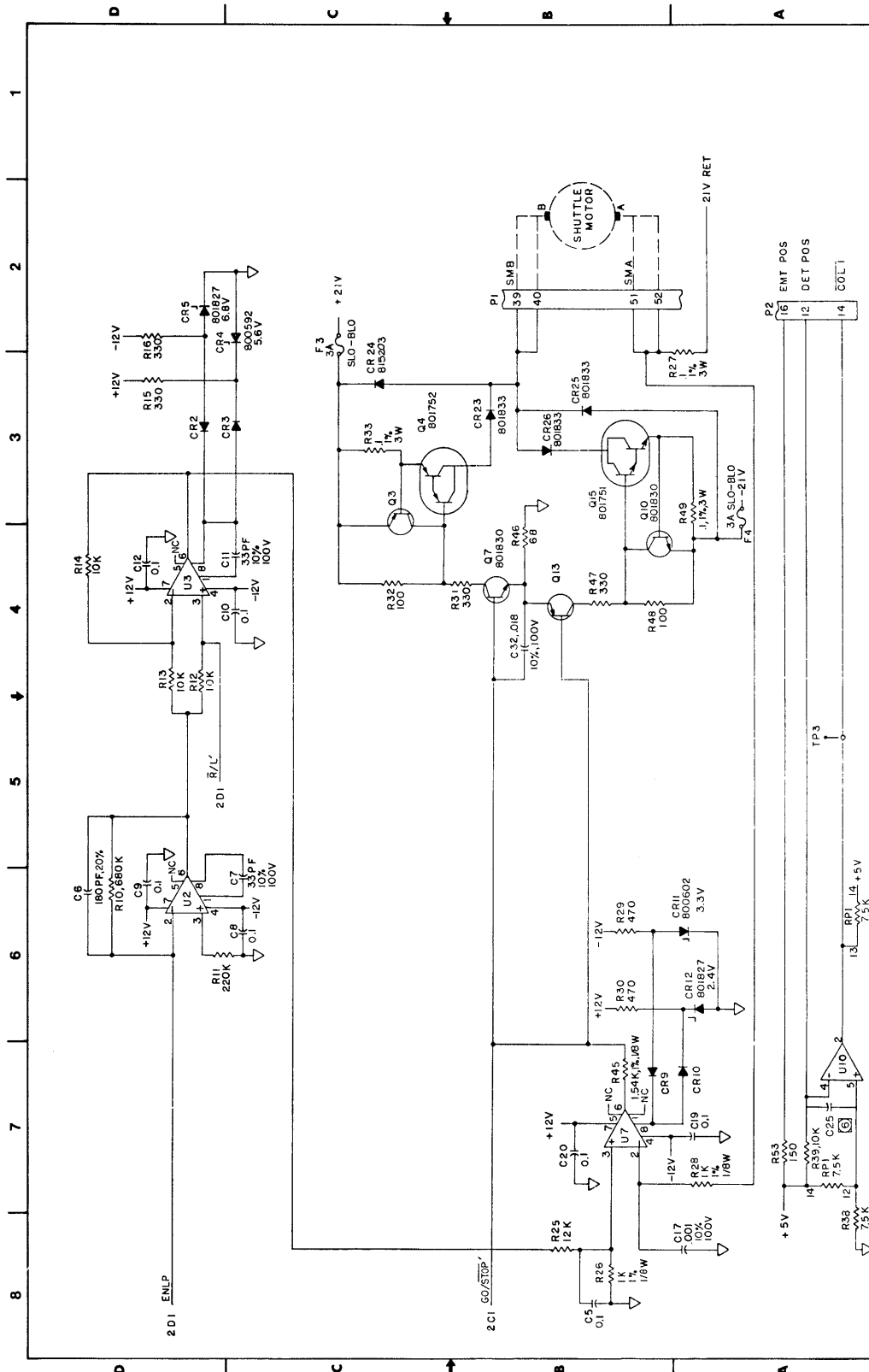
MODEL M200
FIGURE 9-15 (SH 5 OF 5)
LOGIC DIAGRAM
PROCESSOR CCA

MODEL M200
FIGURE 9-16 (SH 1 OF 4)
SCHEMATIC DIAGRAM
MOTOR DRIVER CCA



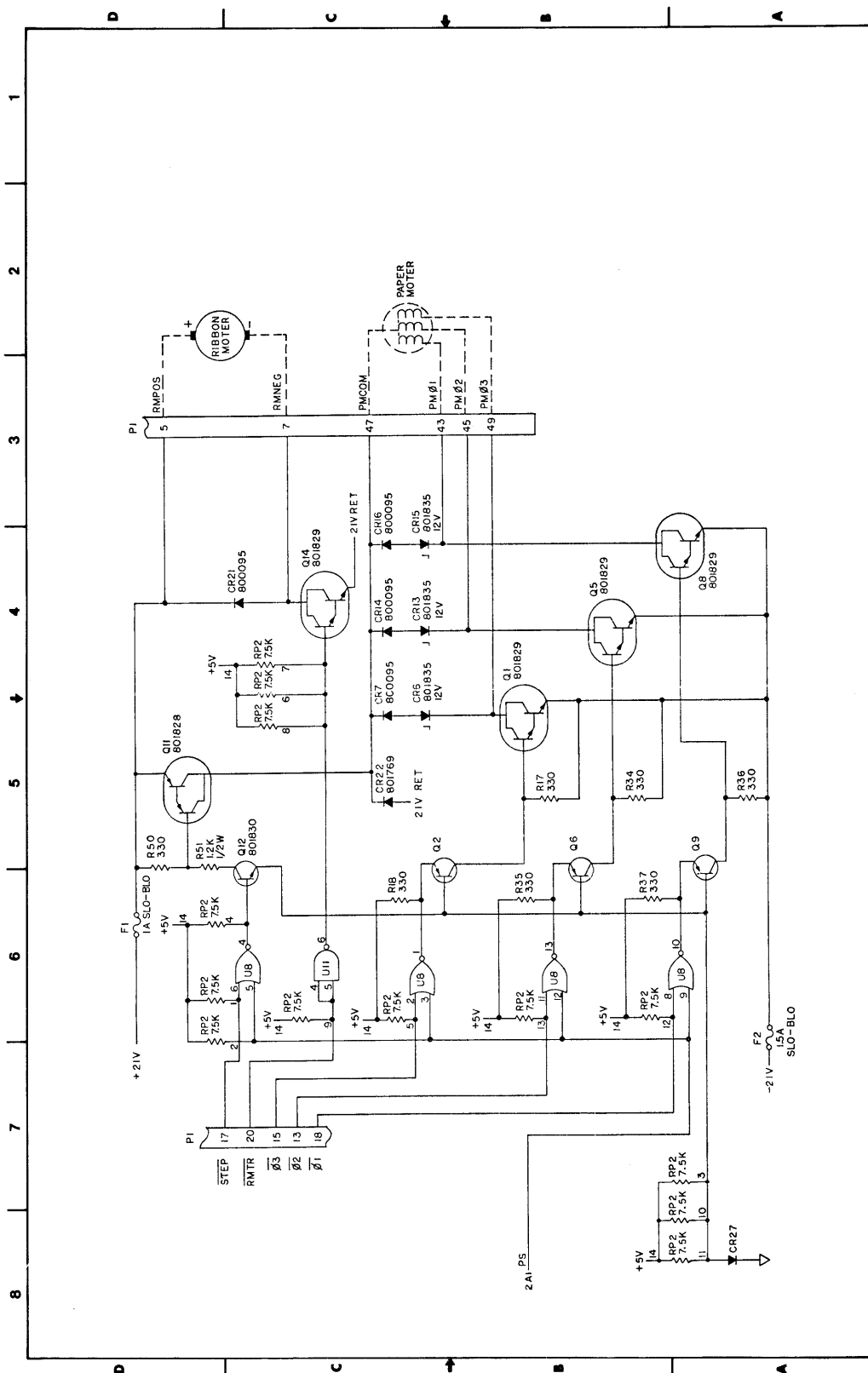


MODEL M200
FIGURE 9-16 (SH 2 OF 4)
SCHEMATIC DIAGRAM
WIRE DRIVER CCA



MODEL M200
FIGURE 9-16 (SH 3 OF 4)
SCHEMATIC DIAGRAM
MOTOR DRIVER CCA

9-76R



MODEL M200
FIGURE 9-16 (SH 4 OF 4)
SCHEMATIC DIAGRAM
MOTOR DRIVER CCA

10. ALL DIODES ARE IN 4934.

9. TRANSISTORS ARE:

TIP 121 Q30-43

TIP 126 Q15-29

8. REFER TO MOTHER BOARD SCHEMATIC 245694

FOR OFF-BOARD SIGNAL LOCATIONS.

7. SOURCE AND DESTINATION POINTS OF INTERRUPTED

SIGNAL LOCATIONS ARE CODED BY SHEET NO AND

ZONE LOCATION (E.G. 7C2 IS SHEET 7, ZONE C 2)

6. POWER AND GROUND FOR ALL INTEGRATED

CIRCUITS WILL BE AS FOLLOWS:

<u>TOTAL NO. OF PINS/IC</u>	<u>+5V (V_{cc}) PIN NO.</u>	<u>GND PIN NO.</u>
8	8	4
14	14	7

5. INTEGRATED CIRCUITS ARE:
(GENERIC PART NOS. ARE FOR REFERENCE ONLY.)

800024-003 7400 UI2,16,19,23

801798-003 75463 UI3,14,17,18,21,22,24

RESISTOR NETWORKS ARE:

801957-681 U1,5,7,11 801957-152 U3,20
801957-821 U2,8 801957-272 U4,9,10,15

4. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 50 VOLTS.

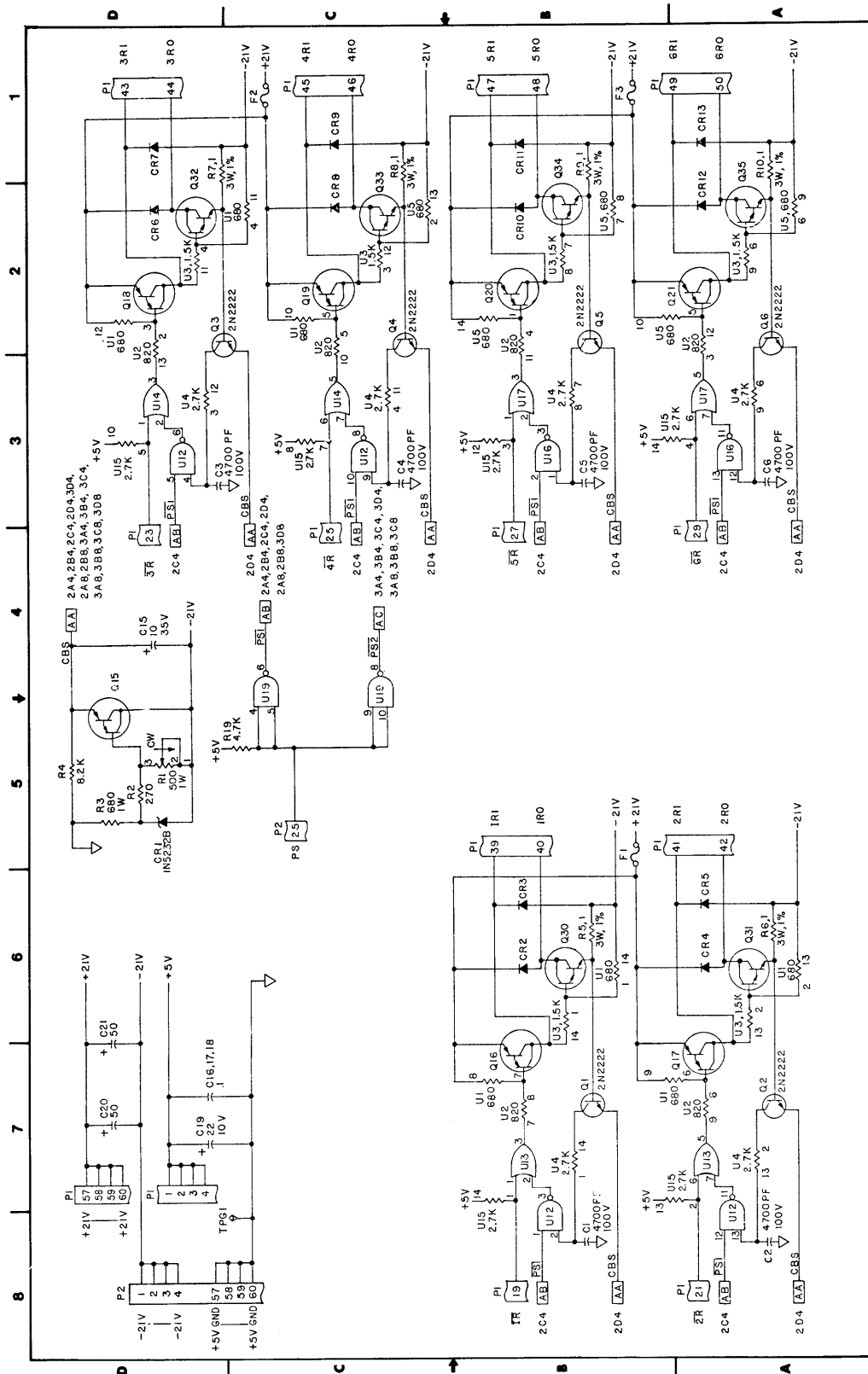
3. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4W.

2. INTERPRET REFERENCE DESIGNATIONS PER DPC SPEC 850027.

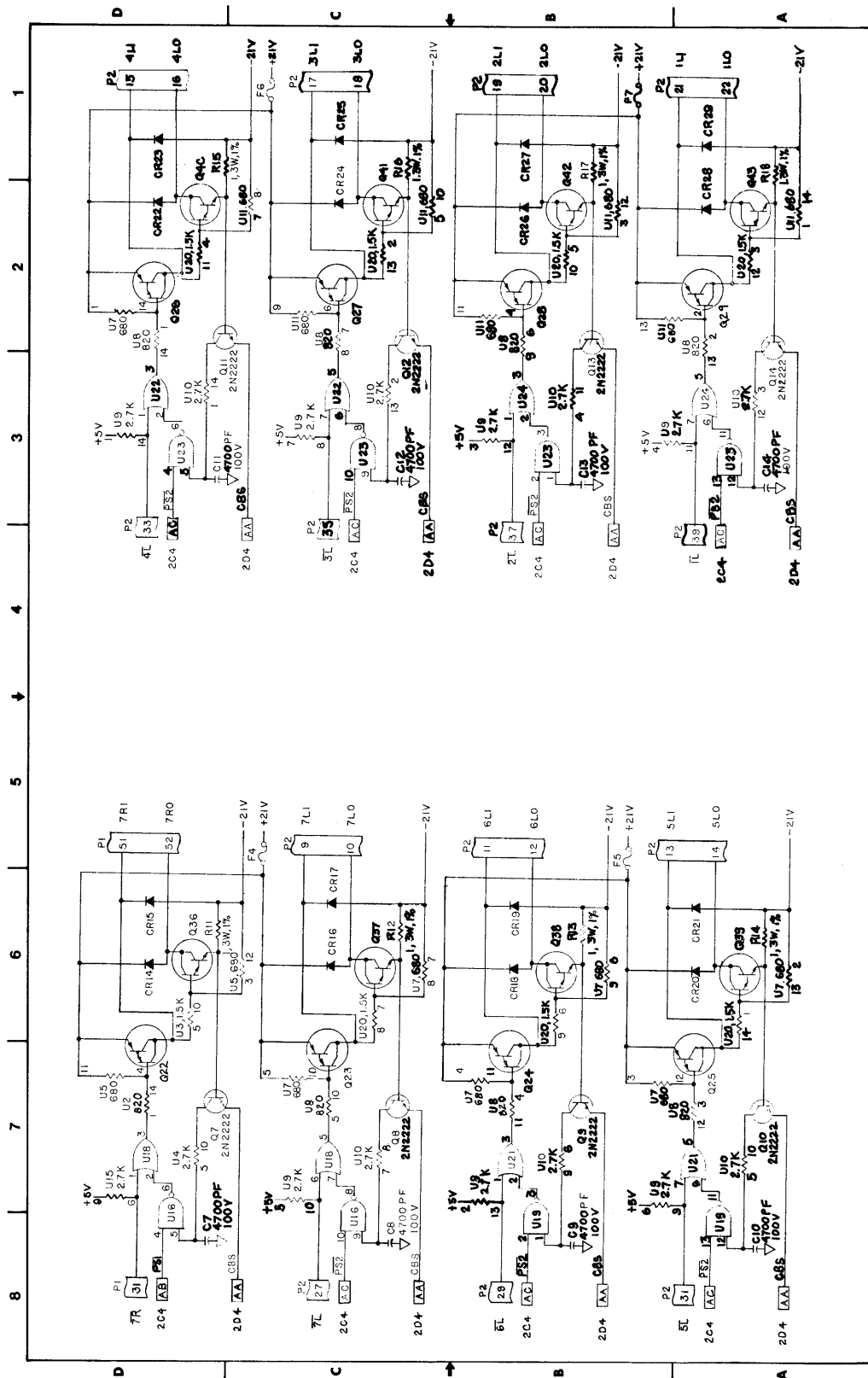
1. INTERPRET ELECTRONIC SYMBOLS PER DPC SPEC 850026.

NOTES (UNLESS OTHERWISE SPECIFIED)

FIGURE 9-17 (SH 1 OF 3)
SCHEMATIC DIAGRAM
WIRE DRIVER CCA



MODEL M200
FIGURE 9-17 (SH 2 OF 3)
SCHEMATIC DIAGRAM
WIRE DRIVER CCA



MODEL M200
FIGURE 9-17 (SH 3 OF 3)
SCHEMATIC DIAGRAM
WIRE DRIVER CCA

LOGIC DIAGRAMS

- 8. REFERENCE LOGIC DIAGRAM 245779, REV. A.
- 7. SIGNAL MNEMONICS WHICH CONTAIN A BAR (—) ARE ACTIVE IN THE LOW STATE.
- 6. SOURCE AND DESTINATION POINTS OF INTERRUPTED SIGNALS GENERATED ON-BOARD ARE CODED BY SHEET NO. AND ZONE LOCATION (E.G. 7C2 IS SHEET 7, ZONE C-2).
- 5. SOURCE AND DESTINATION POINTS OF INPUT/OUTPUT SIGNALS ARE CODED BY FIGURE AND SHEET LOCATION (E.G. FIG. 9-7, SH. 3 IS FIGURE 9-7, SHEET 3).
- 4. POWER AND GROUND FOR ALL INTEGRATED CIRCUITS WILL BE AS FOLLOWS:

TOTAL NO. OF PINS/IC	5V (VCC) PIN NO.	GND PIN NO.
14	14	7

- 3. INTEGRATED CIRCUITS ARE:
(GENERIC PART NUMBERS ARE PROVIDED FOR "REFERENCE ONLY".)

800491-003	74121	U1
800959-003	7414	U2

- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 50 VOLTS.
- 1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4W.

NOTES (UNLESS OTHERWISE SPECIFIED)

SPARE CIRCUITS

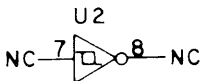
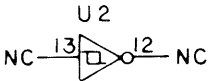
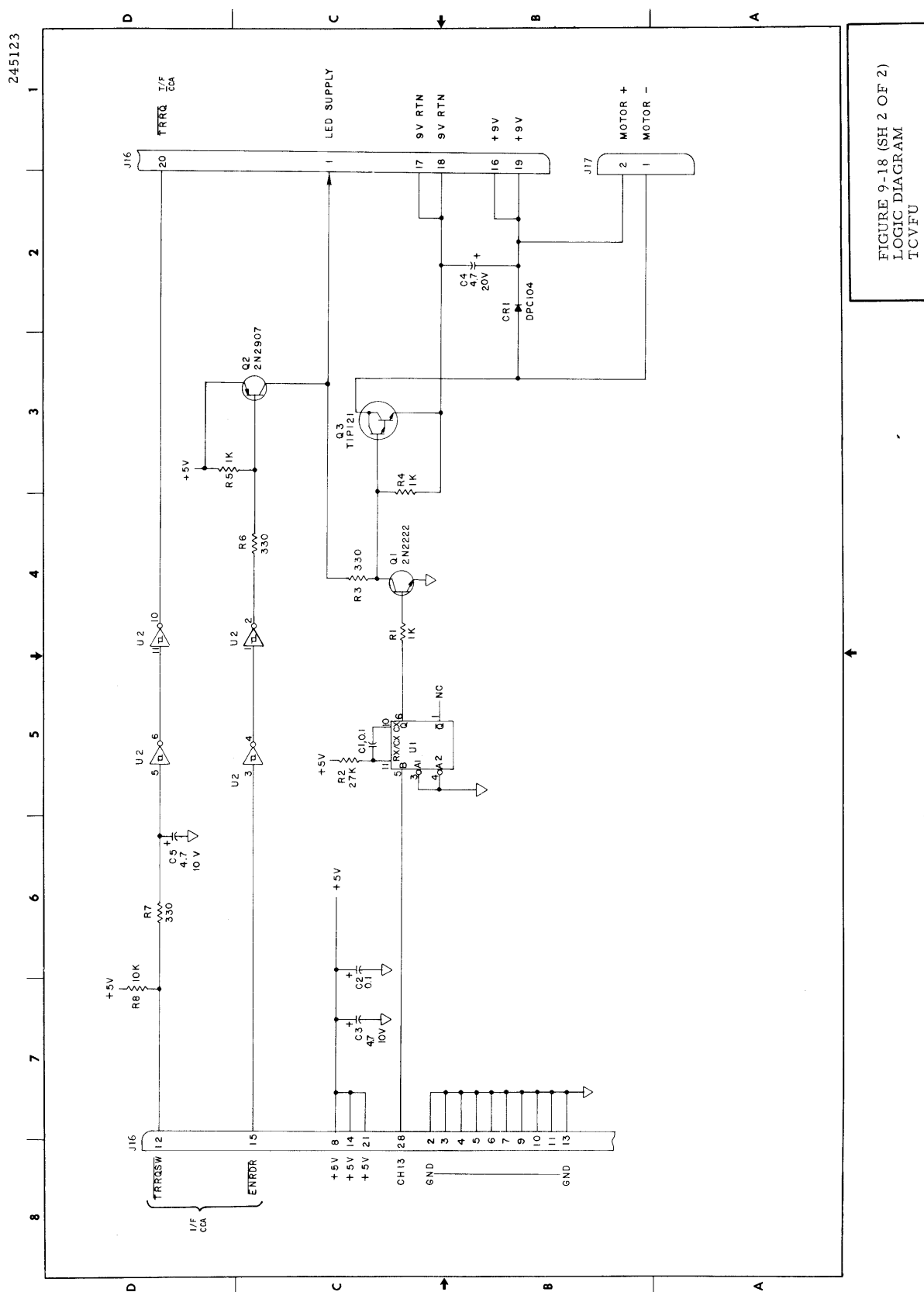


FIGURE 9-18 (SH 1 OF 2)
LOGIC DIAGRAM
TCVFU



- ② SIGNAL NAMES CALLED OUT FOR INTERFACE CONNECTIONS ARE FOR DPC SHORT LINE AND LONG LINE I/F CARDS ONLY.
1. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 50 VOLTS.

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 9-19 (SH 1 OF 3)
INTERCONNECTION DIAGRAM
MOTHER BOARD

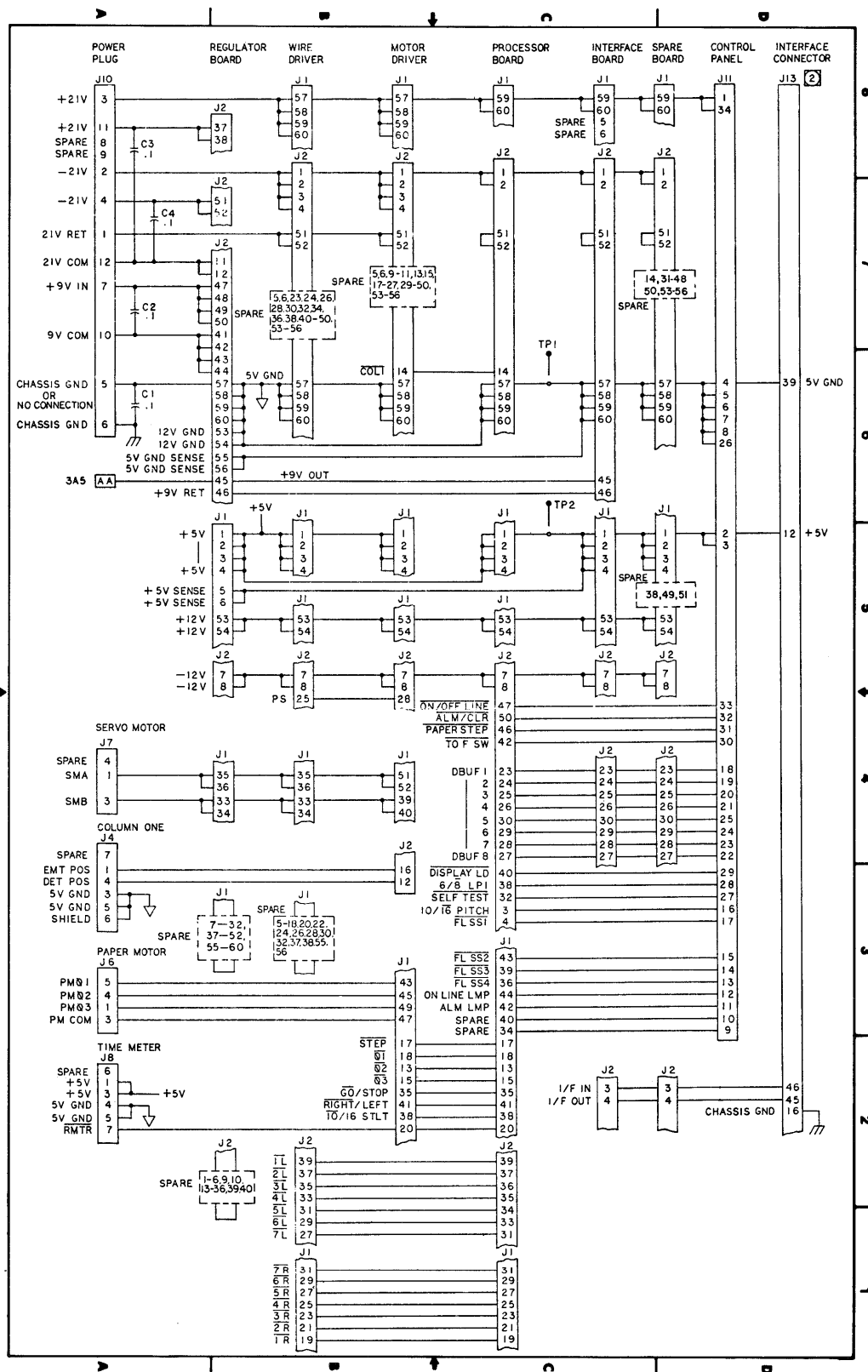


FIGURE 9-19 (SH 2 OF 3)
INTERCONNECTION DIAGRAM
MOTHER BOARD

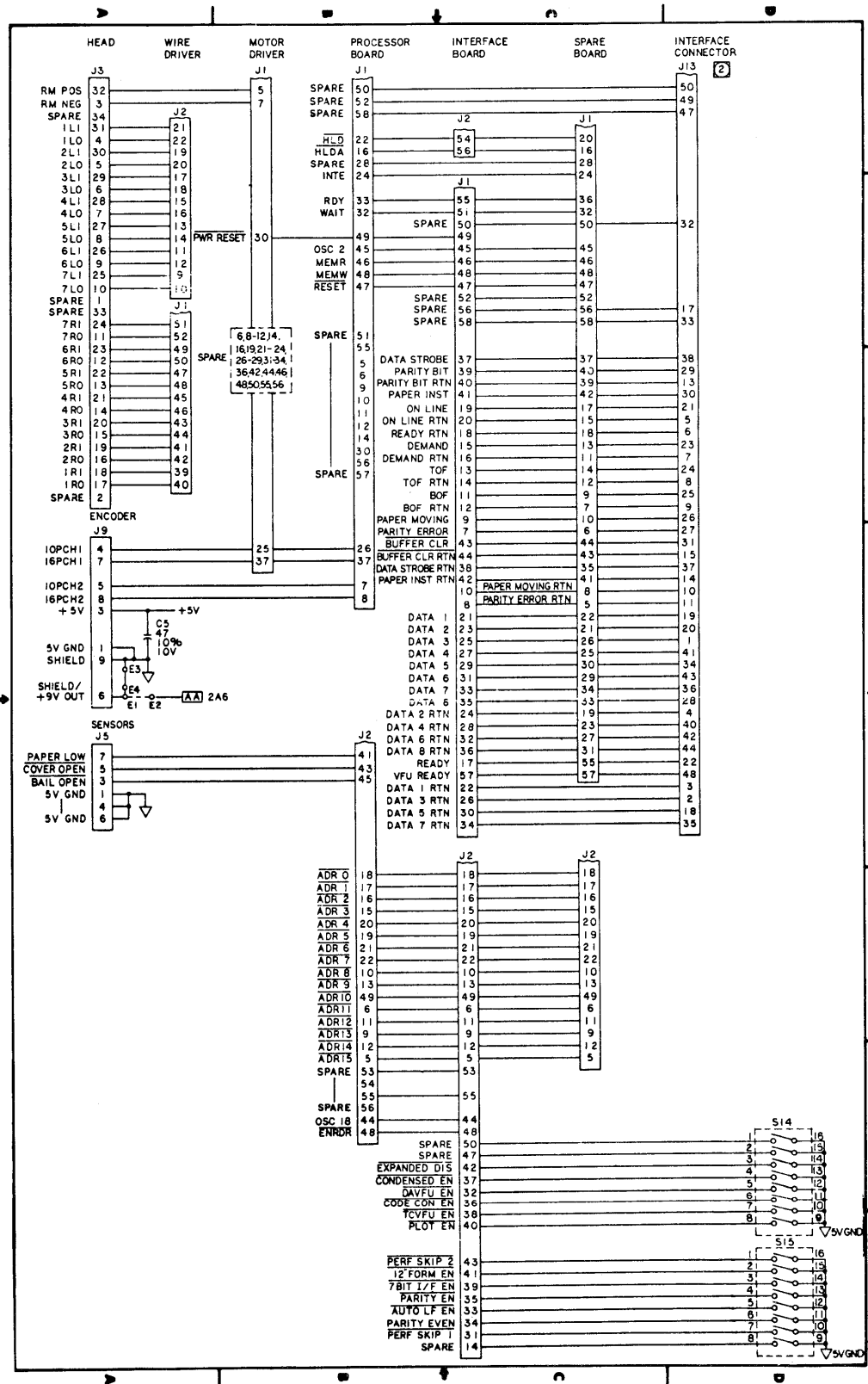


FIGURE 9-19 (SH 3 OF 3)
INTERCONNECTION DIAGRAM
MOTHER BOARD

SECTION X

LOADING DIAGRAMS

10.1 INTRODUCTION

This section contains complete loading diagrams of the integrated circuits (ICs) depicted in the logic diagram sheets of Section IX. Table 10-1 lists the ICs sequentially by DPC drawing number and provides the corresponding package style, IC type number, and loading diagram figure number. Each loading diagram contains complete pin assignments, and in most cases, the functional symbols associated with its circuit elements.

TABLE 10-1. INTEGRATED CIRCUIT LOADING DIAGRAMS

DPC Dwg No.	IC Type No.	Figure No.	DPC Dwg No.	IC Type No.	Figure No.
249687-001-017	2708	1-A	801257-001	LM339	12
249688-001-002	2708	1-B	801528-003	SN74LS00	13
249736-011-014	2716	2	801529-003	SN74LS04	14
800024-003	74LS7400	3	801530-003	SN74LS08	15
800400-003	SN7474	4	801532-003	SN74LS11	16
800491-003	SN74121	5	801533-003	SN74LS14	17
800651-001	74LS7406	6	801534-003	SN74LS20	18
801006-391	Resistor Network	7	801536-003	SN74LS32	19
801006-681	Resistor Network	7	801540-003	SN74LS74	20
801006-752	Resistor Network	7	801541-003	SN74LS75	21
801023-003	SN74221	8	801550-003	SN74LS273	22
801179-001	723N	9	801558-003	SN74LS136	23
801180-003	SN74154	10	801576-005	SN7432	24
801224-001	4N26	11	801584-003	SN74LS02	25
			801585-003	SN74LS138	26

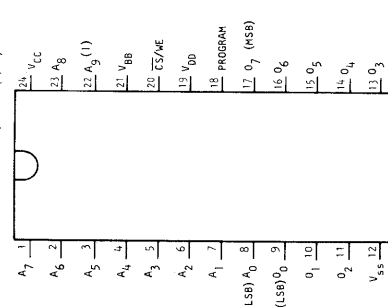
LOADING DIAGRAMS

TABLE 10-1. INTEGRATED CIRCUIT LOADING DIAGRAMS (Contd)

DPC Dwg No.	IC Type No.	Figure No.	DPC Dwg No.	IC Type No.	Figure No.
801614-001	2114	27	801838-003	SN74LS33	48
801691-003	SN74LS240	28	801879-001	TL182C	49
801693-003	SN74273	29	801888-001	MC1489A	50
801694-003	SN74LS393	30	801889-001	MC1488	51
801713-004	8111A-4	31	801913-002	SN74S287	52
801716-003	74LS244	32	801957-152	Resistor Network	55
801759-003	SN74LS86	33	801957-272	Resistor Network	55
801798-003	LM75463	34	801957-681	Resistor Network	55
801799-003	SN74LS221	35	801957-821	Resistor Network	55
801800-003	SN74LS132	36	801961-003	SN74LS373	53
801802-001	8228	37	801963-003	SN74LS197	54
801803-001	8224	38	801964-001	AM9551	56
801804-001	8080A	39	801965-003	DS26LS31	57
801805-001	DP8304	40	801966-003	DS26LS32	58
801806-001	LM301	41	801991-005	MM2316E	59
801807-003	74LS03	43	801996-001	TIL311	60
801808-001	NE555	42	801999-003	SN74LS390	61
801811-003	74LS366	44	810000-001	5307	62
801812-003	SN74LS125	45	810009-001	6N137	63
801813-003	SN74LS112	46	810118-003	SN74122	64
801814-003	SN74LS280	47			

FIGURE 1-A. 8K UV ERASABLE PROM
DPC 249607-001 (2708)

FIGURE 1-B. 8K UV ERASABLE PROM
DPC 249608-001, -002 (2708)



16K UV ERASABLE PROM
DPC 249736-011 THRU -014 (2716)

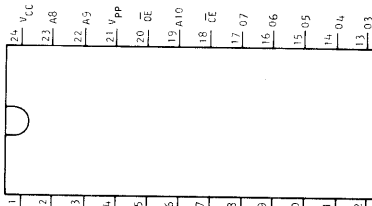


FIGURE 2.

RESISTOR NETWORK, PULLUP, 1/4 WATT
13 RESISTORS
DPC 801006-391 (390 Ω)
801006-481 (680 Ω)
801006-752 (7.5K Ω)

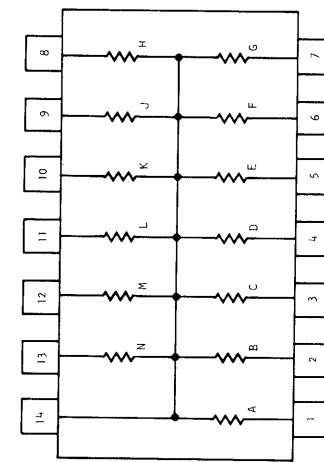


FIGURE 7.

OPTICALLY-COUPLED ISOLATOR
DPC 801224-001 (4N26)

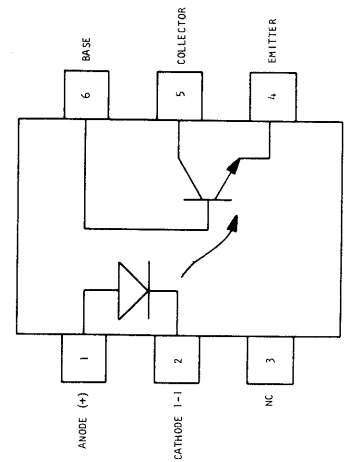


FIGURE 11.

QUADRUPLER 2-INPUT
POSITIVE NAND GATES
DPC 800024-003 (74LS7400)

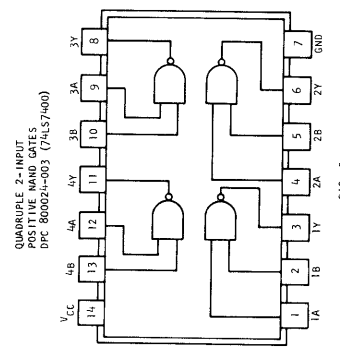


FIGURE 3.

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR
DPC 800400-003 (SN7474)

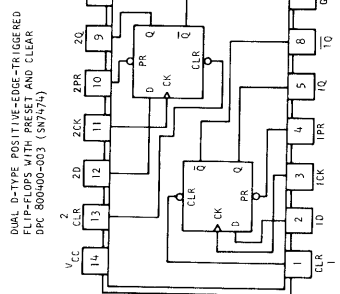


FIGURE 4.

MONOSTABLE MULTIVIBRATOR
DPC 800491-003 (SN 74121)

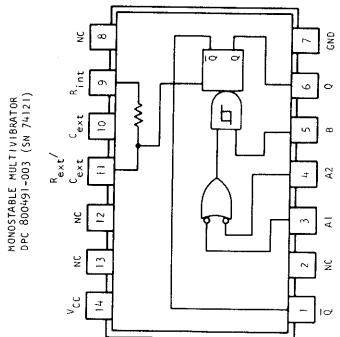


FIGURE 5.

HEX INVERTER BUFFERS/DRIVERS
DPC 800551-001 (74LS7406)

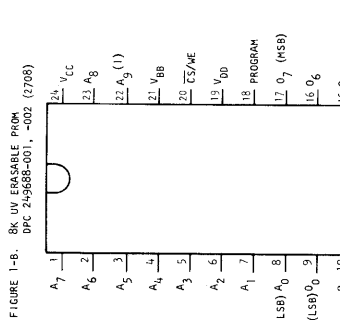


FIGURE 6.

VOLTAGE REGULATOR
DPC 801179-001 (723N)

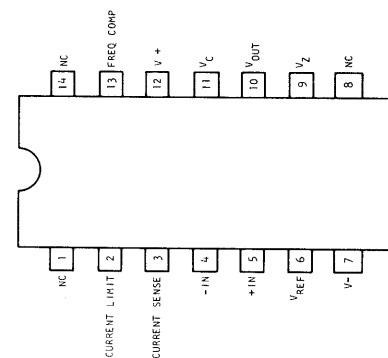


FIGURE 9.

DUAL MONOSTABLE MULTIVIBRATOR
DPC 801023-003 (SN 74221)

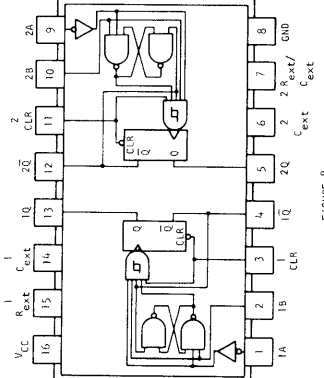


FIGURE 8.

QUAD VOLTAGE COMPARATORS
DPC 801257-001 (LM339)

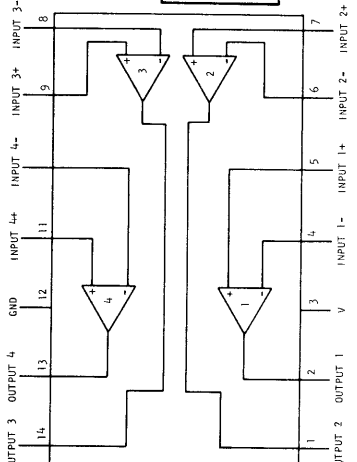


FIGURE 12.

4-LINE-TO-16-LINE DECODER/DEMULTIPLEXER
801180-003 (SN74154)

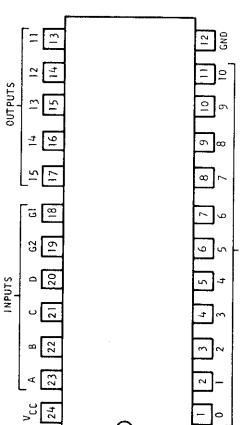


FIGURE 10.

Loading Diagrams
Figures 1 - 12

LOADING DIAGRAMS

QUADRUPLER 2-INPUT
POSITIVE-OR GATES
DPC 801558-003 (SN74LS00)

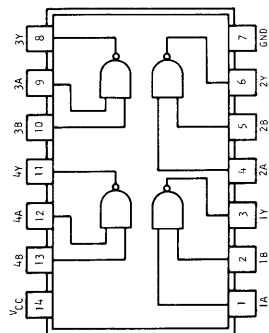


FIG. 13

HEX INVERTERS
DPC 801529-003 (SN74LS04)

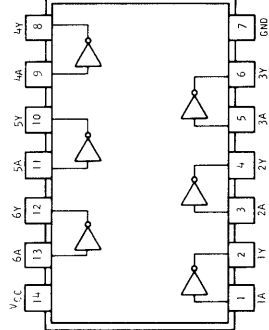


FIG. 14

QUADRUPLER 2-INPUT
POSITIVE-AND GATES
DPC 801530-003 (SN74LS08)

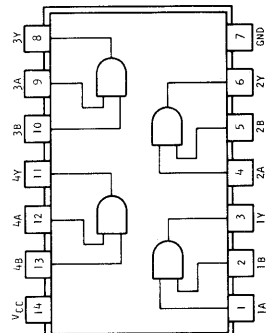


FIG. 15

TRIPLE 3-INPUT
POSITIVE-AND GATES
DPC 801531-003 (SN74LS11)

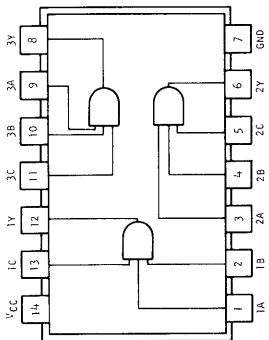


FIG. 16

HEX SCHMITT TRIGGERS/INVERTERS
DPC 801533-003 (SN74LS14)

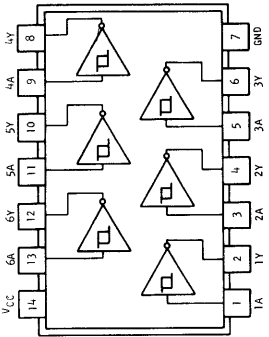


FIG. 17

QUADRUPLER 2-INPUT
POSITIVE-OR GATES
DPC 801536-003 (SN74LS32)

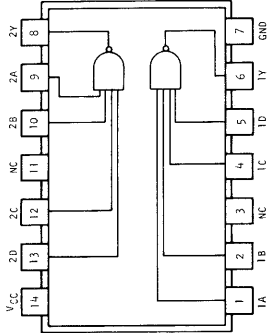


FIG. 18

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR
DPC 801540-003 (SN74LS74)

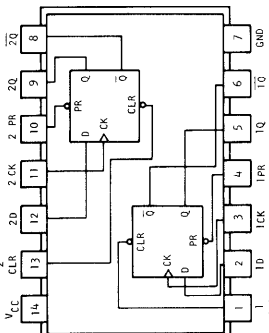


FIG. 19

4-BIT BISTABLE LATCHES
DPC 801541-003 (SN74LS75)

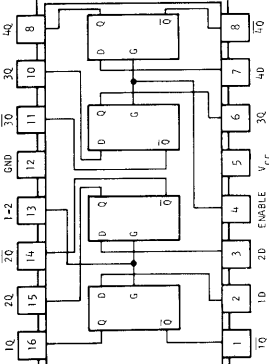


FIG. 20

OCTAL D-TYPE FLIP-FLOPS
DPC 801550-003 (SN74LS273)

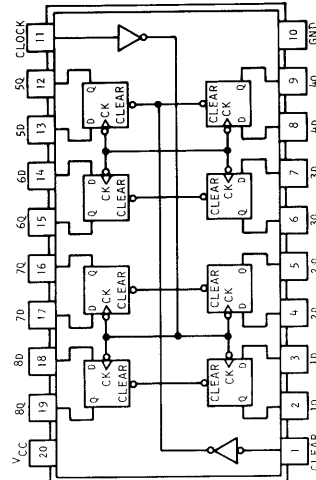


FIG. 22

QUADRUPLER 2-INPUT
POSITIVE-OR GATES
DPC 801536-003 (SN74LS32)

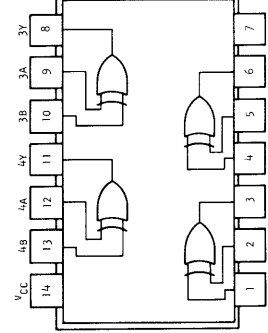


FIG. 23

QUADRUPLER 2-INPUT
POSITIVE-NOR GATES
DPC 801581-003 (SN74LS02)

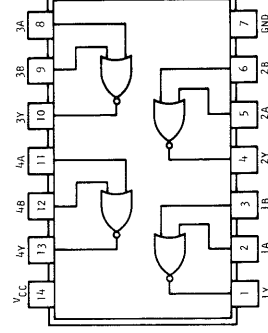


FIG. 25

3-TO-8 LINE DECODER/MULTIPLEXERS
DPC 801585-003 (SN74LS138)

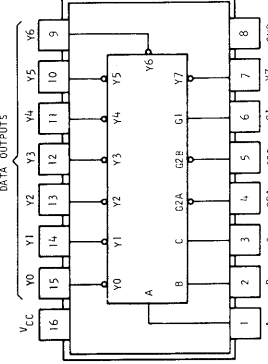
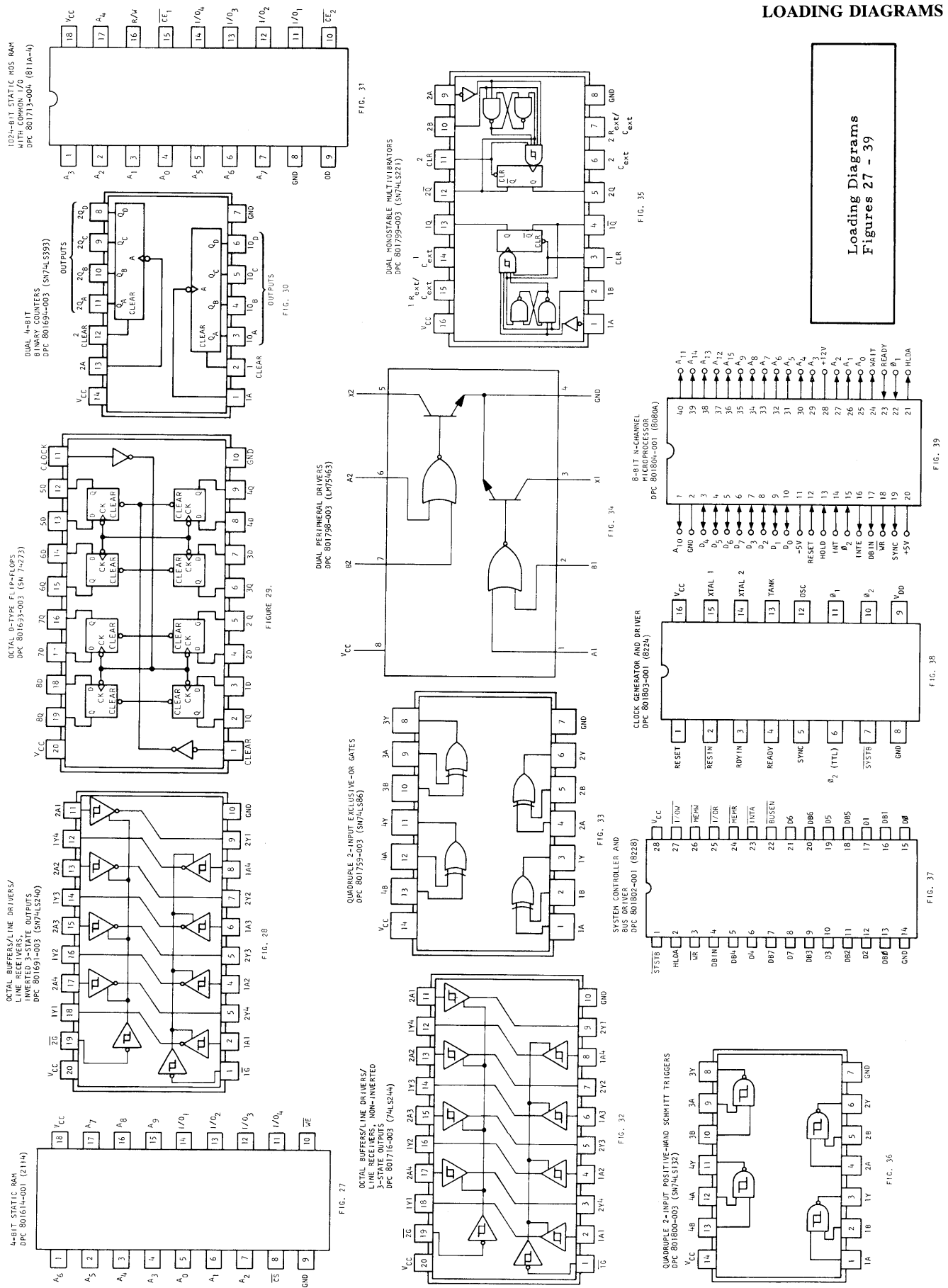


FIG. 26

Loading Diagrams
Figures 13 - 26



LOADING DIAGRAMS

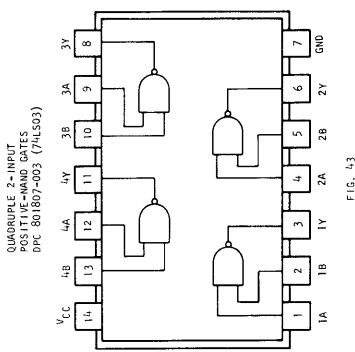


FIG. 43

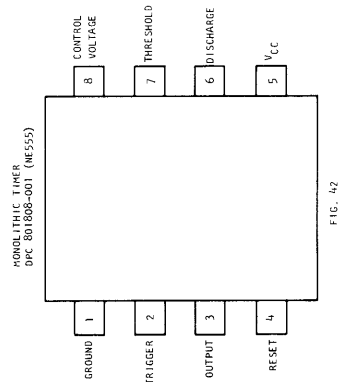


FIG. 42

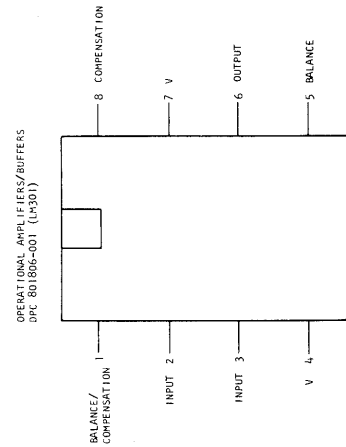


FIG. 41

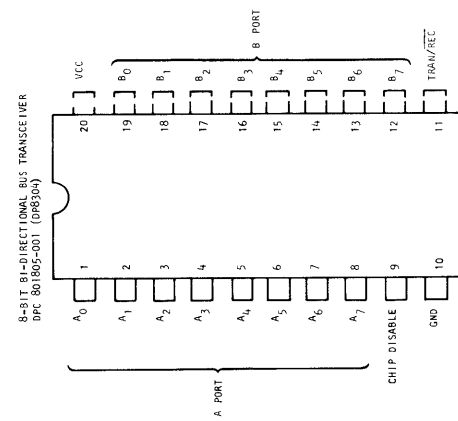


FIG. 40

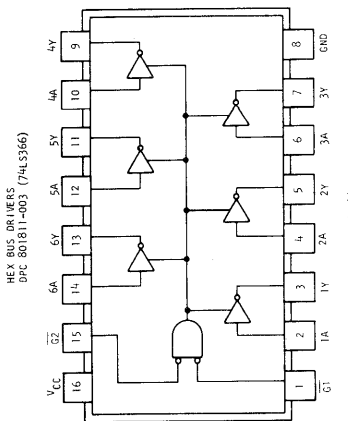


FIG. 44

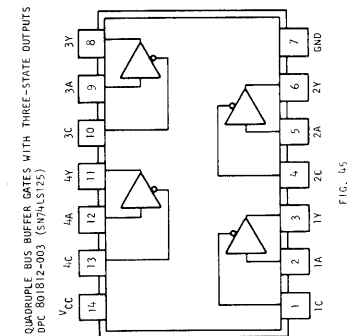


FIG. 45

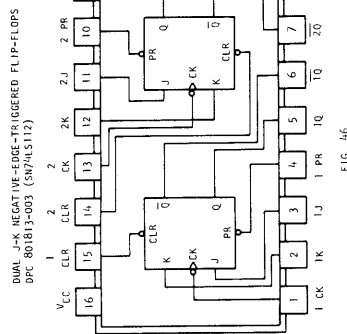


FIG. 46

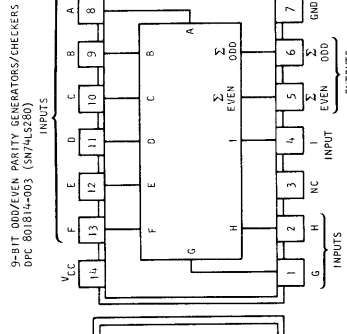


FIG. 47

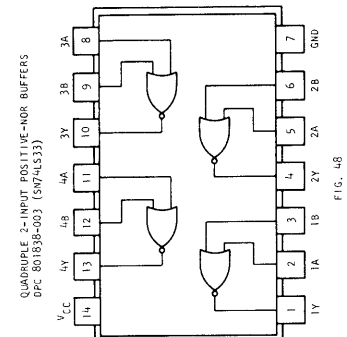


FIG. 48

TWIN SPST ANALOG SWITCHES
DPC 801879-001 (74LS182C)

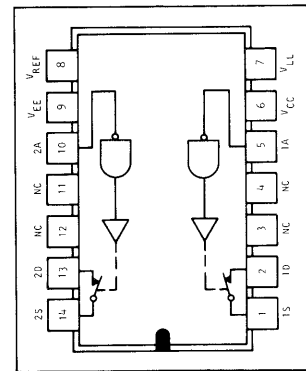


FIG. 49

QUADRUPEL LINE RECEIVERS
DPC 801888-001 (MC1489A)

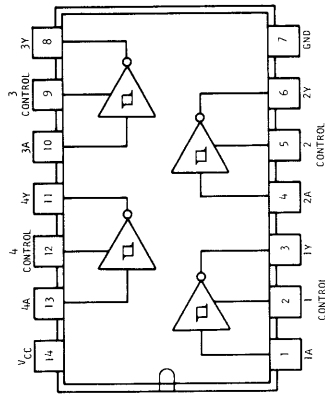


FIG. 50

QUADRUPEL LINE DRIVER
DPC 801889-001 (MC1489)

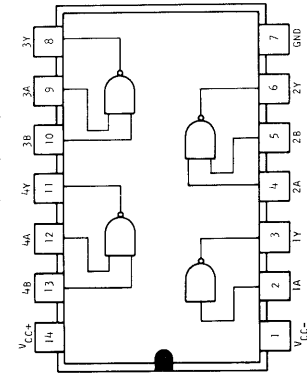
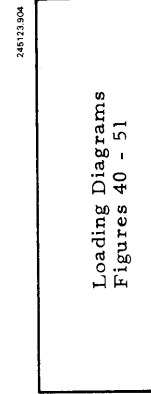
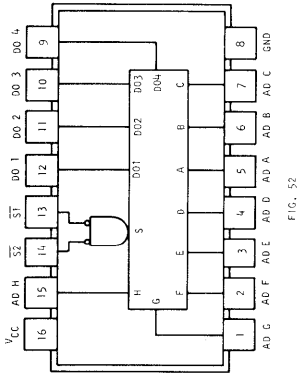


FIG. 51

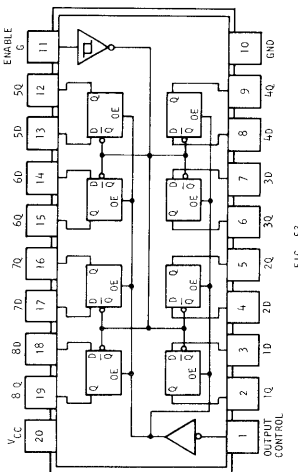


Loading Diagrams
Figures 40 - 51

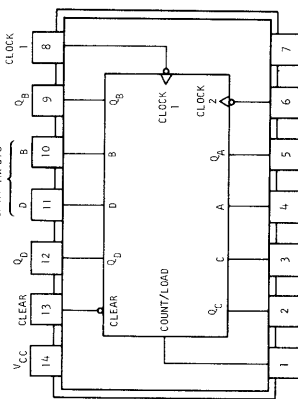
1024-BIT PROGRAMMABLE READ-ONLY MEMORIES
DPC 801913-002 (SN74L287)



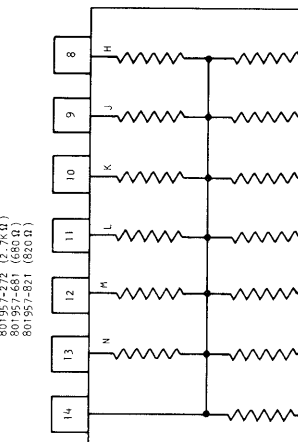
DUAL D-TYPE LATCHES
DPC 801961-003 (SN74L5373)



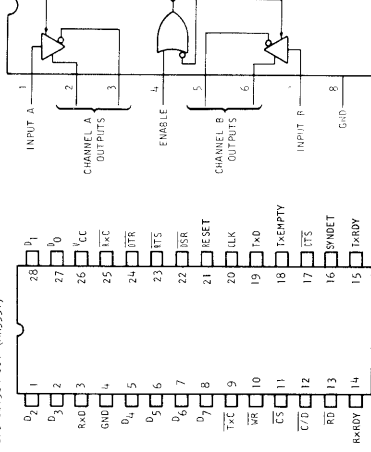
BINARY PRESETTABLE COUNTERS/LATCHES
DPC 801965-003 (SN74L5377)



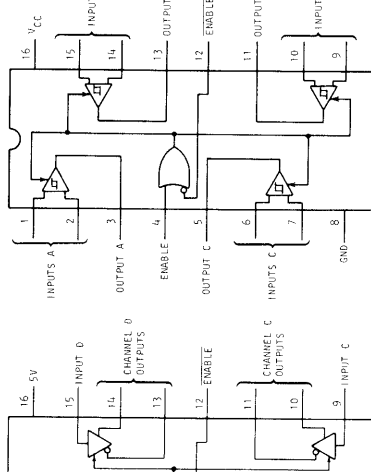
RESISTOR NETWORK, PULL-UP, 1/4 WATT
DPC 801957-15 (1.5K Q)
DPC 801957-272 (2.7K Q)
DPC 801957-681 (680 Q)
DPC 801957-821 (820 Q)



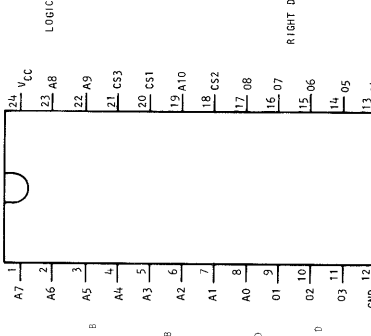
PROGRAMMABLE COMMUNICATION INTERFACE
DPC 801964-001 (AM5551)



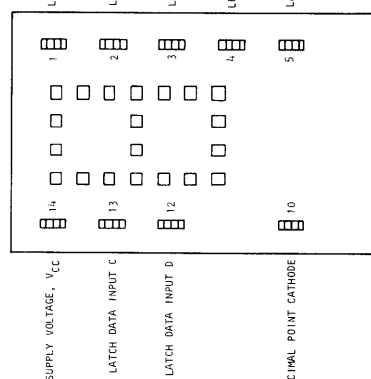
QUAD HIGH SPEED DIFFERENTIAL LINE DRIVER
DPC 801965-003 (DS26L531)



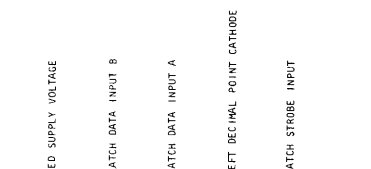
QUAD DIFFERENTIAL LINE RECEIVERS
DPC 801966-003 (DS26L532)



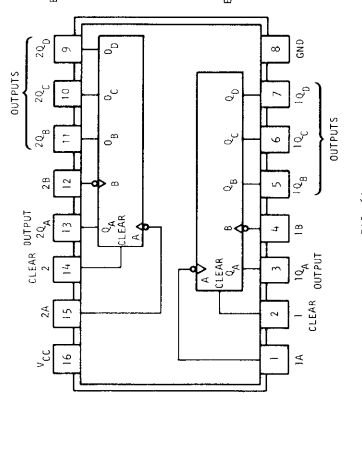
16, 138-BIT READ ONLY MEMORY
(2048 BY 8)
DPC 801991-005 (M2316E)



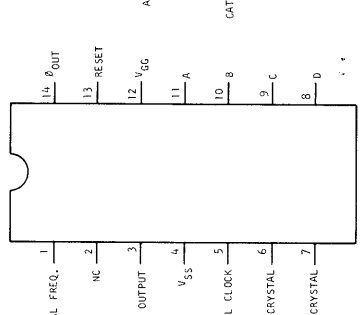
HEADDECIMAL DISPLAY WITH LOGIC
DPC 801996-001 (TIL511)



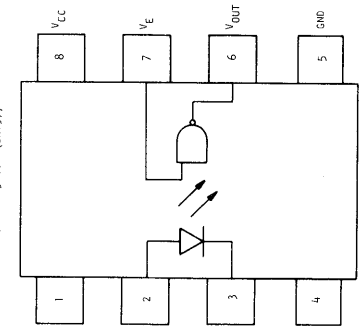
DUAL DECADE COUNTERS
DPC 801999-003 (SN74L5390)



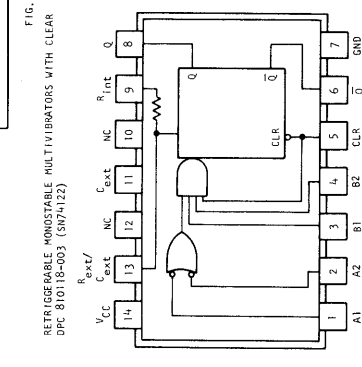
RAID RATE GENERATOR/PROGRAMMABLE DIVIDER
DPC 810000-001 (S307)



OPTICALLY-COUPLED GATE
DPC 810009-001 (6N137)



RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR
DPC 810118-003 (SN74122)



Model M200
Loading Diagrams
Figures 52 - 64

FIG. 52

FIG. 53

FIG. 54

FIG. 55

FIG. 56

FIG. 57

FIG. 58

FIG. 59

FIG. 60

FIG. 61

FIG. 62

FIG. 63

FIG. 64



Section 11

REPLACEABLE PARTS

[illegible]

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

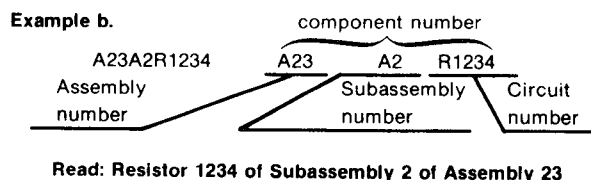
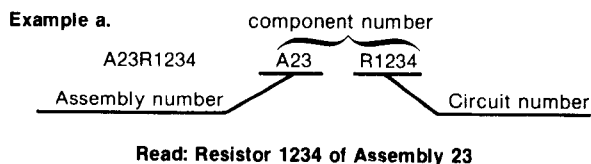
The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:



Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

ILLUSTRATED PARTS LIST

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD, PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
12954	SIEMENS CORPORATION, COMPONENTS GROUP	8700 E THOMAS RD, P O BOX 1390	SCOTTSDALE, AZ 85252
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
20932	EMCON DIV OF ILLINOIS TOOL WORKS INC.	11620 SORRENTO VALLEY RD	
		P O BOX 81542	SAN DIEGO, CA 92121
*23241	DATA PRODUCTS CORP.	21300 ROSCOE BLVD.	CANOGA PARK, CA 91304
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
33096	COLORADO CRYSTAL CORPORATION	2303 W 8TH STREET	LOVELAND, CO 80537
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET	
		P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

*REPLACED BY:

19790	DATA PRODUCTS CORP.	6200 CANOGA AVE.	WOODLAND HILLS, CA 91365
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ILLUSTRATED PARTS LIST

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	118-1291-03	OPT 1	CKT BOARD ASSY:SERIAL INTERFACE	23241	261550-002
A2A1	118-1291-XX		CKT BOARD ASSY:NOT AVAILABLE,SEE A2		
A2.1	118-1287-00		CKT BOARD ASSY:SHORTLINE PARALLEL INTFC	23241	245685-001
A3	118-1250-01		CKT BOARD ASSY:PROCESSOR	23241	261155-001
A3A1	118-1250-XX		CKT BOARD ASSY:NOT AVAILABLE,SEE A3		
A4	118-1249-00		CKT BOARD ASSY:MOTOR DRIVER	23241	261660-001
A5	118-1285-00		CKT BOARD ASSY:WIRE DRIVER	23241	249910-001
A6	118-1251-00		CKT BOARD ASSY:REGULATOR	23241	249785-001
A7	118-1271-00		CKT BOARD ASSY:MOTHER	23241	261645-001
A8	118-1321-00		CONTROL PANEL AS:	23241	245801-001
A11	118-1318-XX		POWER SUPPLY COMPONENTS:(NOT ORDERABLE)		
A2	118-1291-03		CKT BOARD ASSY:SERIAL INTERFACE	23241	261550-002
	-----		(STANDARD ONLY.FOR OPTION 1 SEE A2.1)		
A2M1	118-1167-00		MICROCIRCUIT,DI:1024 X 8 EPROM,PRGM	80009	118-1167-00
A2M2	118-1168-00		MICROCIRCUIT,DI:1024 X 8 EPROM,PRGM	80009	118-1168-00
A2A1	118-1291-XX		CKT BOARD ASSY:(NOT AVAILABLE, SEE A2)		
A2A1C1	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C2	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C3	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C4	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C5	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C6	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C7	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C8	290-0162-00		CAP.,FXD,ELCTLT:22UF,20%,35V	12954	D22C35M1
A2A1C9	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C10	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C11	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C12	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C13	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C14	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C15	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C16	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C17	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C18	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C19	290-0301-00		CAP.,FXD,ELCTLT:10UF,10%,20V	56289	150D106X9020B2
A2A1C20	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C21	281-0757-00		CAP.,FXD,CER DI:10PF,20%,100V	72982	8035-D-COG-100G
A2A1C22	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C23	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C24	290-0162-00		CAP.,FXD,ELCTLT:22UF,20%,35V	12954	D22C35M1
A2A1C25	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C26	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C27	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C28	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C29	290-0134-00		CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A2A1C30	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A2A1C31	281-0788-00		CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A2A1C32	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C33	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C34	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C35	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C36	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C37	281-0788-00		CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K

ILLUSTRATED PARTS LIST

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A2A1C38	281-0788-00		CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A2A1C39	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C40	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2A1C41	283-0191-00		CAP.,FXD,CER DI:0.022UF,20%,50V	72982	8121N07525U0223M
A2A1C42	118-1557-00		CAP.,FXD ELECT:330PF 100V,10%	23241	800046-331
A2A1C43	281-0788-00		CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A2A1C44	281-0788-00		CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A2A1C45	281-0788-00		CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A2A1CR1	152-0024-00		SEMICONV DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A2A1CR2	118-1537-00		SEMICONV DEVICE:REGULATOR	23241	810041-001
A2A1CR4	118-1486-00		SEMICONV DEVICE:ZEN,3.34,5%,DPC-120	23241	800602-001
A2A1CR5	152-0414-00		SEMICONV DEVICE:SILICON,200V,0.75A	12969	UTR308
A2A1CR6	152-0024-00		SEMICONV DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A2A1CR7	152-0024-00		SEMICONV DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A2A1Q1	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A2A1Q2	151-0301-00		TRANSISTOR:SILICON,PNP	27014	2N2907A
A2A1Q3	151-0301-00		TRANSISTOR:SILICON,PNP	27014	2N2907A
A2A1Q4	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A2A1Q5	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A2A1R1	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2A1R2	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2A1R3	315-0471-00		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A2A1R4	315-0222-00		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A2A1R5	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2A1R6	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A2A1R7	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A2A1R8	315-0104-00	B010100 B010385	RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A2A1R8	315-0474-00	B010386	RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A2A1R9	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2A1R10	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A2A1R11	301-0221-00		RES.,FXD,CMPSN:220 OHM,5%,0.50W	01121	EB2215
A2A1R12	315-0222-00		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A2A1R13	315-0222-00		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A2A1R14	315-0222-00		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A2A1R15	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2A1R16	315-0681-00		RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A2A1R17	315-0681-00		RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A2A1R18	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2A1R19	315-0222-00		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A2A1R20	315-0270-00		RES.,FXD,CMPSN:27 OHM,5%,0.25W	01121	CB2705
A2A1R21	315-0820-00		RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
A2A1R22	315-0181-00		RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A2A1S1	260-1965-00		SWITCH,ROCKER:(4)SPST,125MA,30VDC	23241	801115-004
A2A1S2	260-1965-00		SWITCH,ROCKER:(4)SPST,125MA,30VDC	23241	801115-004
A2A1S3	260-1965-00		SWITCH,ROCKER:(4)SPST,125MA,30VDC	23241	801115-004
A2A1TP1	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A2A1TP2	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A2A1U1	156-0954-00		MICROCIRCUIT,DI:8 BIT MICROPROCESSOR	80009	156-0954-00
A2A1U2	156-0078-02		MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A2A1U5	156-1461-00		MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2A1U7	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2A1U8	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2A1U9	156-0914-02		MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A2A1U10	156-1461-00		MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2A1U11	156-1461-00		MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2A1U12	156-0382-02		MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2A1U13	156-0383-02		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02

ILLUSTRATED PARTS LIST

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A2A1U14	118-1466-00		MICROCIRCUIT,DI:256 X 4 RAM	23241	801713-004
A2A1U15	118-1466-00		MICROCIRCUIT,DI:256 X 4 RAM	23241	801713-004
A2A1U16	156-0383-02		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A2A1U17	156-1461-00		MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2A1U19	156-0479-02		MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A2A1U20	156-0865-02		MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A2A1U21	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2A1U22	156-1065-01		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A2A1U23	156-1065-01		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A2A1U24	118-1467-00		MICROCIRCUIT,DI:8 BIT BIDIRECTIONAL	23241	801805-001
A2A1U25	118-1467-00		MICROCIRCUIT,DI:8 BIT BIDIRECTIONAL	23241	801805-001
A2A1U26	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2A1U27	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2A1U28	156-0947-00		MICROCIRCUIT,DI:SYSTEM CONTROLLER/BUS DRVR	34649	D8228
A2A1U29	118-1554-00		MICROCIRCUIT,DI:USART,9551	23241	810021-001
A2A1U30	156-0733-02		MICROCIRCUIT,DI:DUAL MONOSTABLE MV,SCRN	04713	SN74LS221N/J
A2A1U31	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2A1U32	156-0480-02		MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A2A1U33	118-1532-00		MICROCIRCUIT,DI:BAUD RATE GEN PRGM	23241	801805-001
A2A1U34	118-1530-00		RES NTWK,FXD,FI:7.5K OHMS	23241	801006-752
A2A1U35	156-0153-02		MICROCIRCUIT,DI:HEX INVERTER BUFFER	27014	DM8006
A2A1U36	156-0469-02		MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A2A1U37	156-1373-01		MICROCIRCUIT,DI:QUAD BUS BFR GATES W/3	01295	SN74LS125N3
A2A1U38	156-0471-02		MICROCIRCUIT,DI:DUAL 4/1 LINEDATA SEL	01295	SN74LS253NP3
A2A1U39	118-1534-00		MICROCIRCUIT,DI:OPTICAL COUPLED GATE	23241	810009-001
A2A1U40	118-1530-00		RES NTWK,FXD,FI:7.5K OHMS	23241	801006-752
A2A1U41	156-0479-02		MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A2A1U42	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2A1U43	118-1533-00		MICROCIRCUIT,DI:OPTO-ISOLATOR	23241	810053-001
A2A1U44	156-0945-01		MICROCIRCUIT,DI:CLOCK GEN/DRIVER,PRGM	34649	QD8224
A2A1U45	156-1258-01		MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A2A1U46	156-0910-02		MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A2A1U47	156-0645-02		MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A2A1U48	156-0385-02		MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A2A1U49	156-0879-01		MICROCIRCUIT,DI:QUAD LINE DRIVER,SCRN	80009	156-0879-01
A2A1U50	156-0645-02		MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A2A1U51	156-0645-02		MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A2A1U52	156-0464-02		MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A2A1U53	156-0878-01		MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A2A1U54	156-0878-01		MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A2A1U55	156-0480-02		MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A2A1U56	118-1530-00		RES NTWK,FXD,FI:7.5K OHMS	23241	801006-752
A2A1U57	118-1556-00		MICROCIRCUIT,DI:VOLTAGE REG NEGATIVE	23241	801205-502
A2A1Y1	158-0136-00		XTAL UNIT,QTZ:18.432 MHZ 0.01% SERIES	33096	CCAT 101123

ILLUSTRATED PARTS LIST

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A2.1	118-1287-00	OPT 1	CKT BOARD ASSY:SHORTLINE PARALLEL INTFC	23241	245685-001
A2.1C1	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C2	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C3	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C4	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C5	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C6	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C7	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C8	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C9	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C10	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C11	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C12	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C13	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C14	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C15	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C16	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C17	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C18	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C19	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C20	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C21	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C22	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C23	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C24	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C25	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C26	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C27	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C28	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C29	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C30	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C31	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C32	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C33	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C34	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1C35	290-0134-00	OPT 1	CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A2.1C36	118-1462-00	OPT 1	CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A2.1C38	283-0421-00	OPT 1	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2.1M2	118-2018-00	OPT 1	MICROCIRCUIT,DI:512 X 8 PROM,PROGRAMMED	23241	261200-001
A2.1M3	118-2017-00	OPT 1	MICROCIRCUIT,DI:M200 PROM,PROGRAMMED	23241	801913-002
A2.1R1	315-0472-00	OPT 1	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2.1R2	315-0472-00	OPT 1	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2.1R3	315-0472-00	OPT 1	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2.1R4	315-0472-00	OPT 1	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2.1R5	315-0472-00	OPT 1	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2.1R6	315-0101-00	OPT 1	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A2.1R7	315-0103-00	OPT 1	RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2.1S1	260-1965-00	OPT 1	SWITCH,ROCKER:(4)SPST,125MA,30VDC	23241	801115-004
A2.1TP1	214-0579-00	OPT 1	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A2.1TP2	214-0579-00	OPT 1	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A2.1TP3	214-0579-00	OPT 1	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A2.1TP4	214-0579-00	OPT 1	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A2.1U1	156-0464-02	OPT 1	MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A2.1U2	156-0388-03	OPT 1	MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A2.1U3	156-0479-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A2.1U4	156-0480-02	OPT 1	MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A2.1U5	156-1528-01	OPT 1	MICROCIRCUIT,DI-BIPOLAR,QUAD 2-INP NAND	56289	UHP-408

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Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A2.1U6	156-0388-03	OPT 1	MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A2.1U7	156-1258-01	OPT 1	MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A2.1U8	156-0382-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2.1U9	156-1258-01	OPT 1	MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A2.1U10	156-0388-03	OPT 1	MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A2.1U11	156-0382-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2.1U12	156-0479-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A2.1U13	156-0480-02	OPT 1	MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A2.1U14	156-0385-02	OPT 1	MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A2.1U15	156-1258-01	OPT 1	MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A2.1U16	156-0383-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A2.1U17	156-0385-02	OPT 1	MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A2.1U18	156-0479-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP ORGATE	01295	SN74LS32NP3
A2.1U19	156-0735-02	OPT 1	MICROCIRCUIT,DI:4 BIT BISTABLE LCH,BURN-IN	01295	SN74LS75
A2.1U20	156-0381-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A2.1U21	156-0382-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2.1U22	156-0469-02	OPT 1	MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A2.1U23	156-1373-01	OPT 1	MICROCIRCUIT,DI:QUAD BUS BFR GATES W/3	01295	SN74LS125N3
A2.1U24	156-0481-02	OPT 1	MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A2.1U26	156-0388-03	OPT 1	MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A2.1U27	156-1258-01	OPT 1	MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A2.1U28	156-1518-00	OPT 1	MICROCIRCUIT,DI:QUINT EXCLUSIVE OR NOR GAT	07263	F100107DC
A2.1U29	156-0645-02	OPT 1	MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A2.1U30	156-0462-00	OPT 1	MICROCIRCUIT,DI:HEX SCHMITT TRIG,TTL	80009	156-0462-00
A2.1U31	156-0462-00	OPT 1	MICROCIRCUIT,DI:HEX SCHMITT TRIG,TTL	80009	156-0462-00
A2.1U32	156-0480-02	OPT 1	MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A2.1U33	156-0865-02	OPT 1	MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A2.1U34	156-0956-02	OPT 1	MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2.1U35	156-1258-01	OPT 1	MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A2.1U36	156-0462-00	OPT 1	MICROCIRCUIT,DI:HEX SCHMITT TRIG,TTL	80009	156-0462-00
A2.1U37	118-1518-00	OPT 1	HEATSINK,ELEC:WIRE DRIVER	23241	245885-001
A2.1U38	118-1530-00	OPT 1	RES NETWK,FXD,FI:7.5K OHMS	23241	801006-752
A2.1U39	156-1461-00	OPT 1	MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2.1U40	156-0914-02	OPT 1	MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A2.1U41	156-0956-02	OPT 1	MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2.1U42	156-0914-02	OPT 1	MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A2.1U43	156-1065-01	OPT 1	MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A2.1U44	156-0915-02	OPT 1	MICROCIRCUIT,DI:9 BIT ODD/EVEN PARITY GEN	80009	156-0915-02
A2.1U45	156-0956-02	OPT 1	MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2.1U46	156-0702-01	OPT 1	MICROCIRCUIT,DI:3 STATE INVERTING HEX BFR	01295	SN74LS366
A2.1U47	156-1461-00	OPT 1	MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2.1U48	156-0956-02	OPT 1	MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2.1U49	118-1467-00	OPT 1	MICROCIRCUIT,DI:8 BIT BIDIRECTIONAL	23241	801805-001
A2.1U50	156-0956-02	OPT 1	MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2.1U51	156-0956-02	OPT 1	MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2.1U52	156-0385-02	OPT 1	MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A2.1U53	156-0382-02	OPT 1	MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2.1U54	156-1172-01	OPT 1	MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	01295	SN74LS393
A2.1U55	156-0956-02	OPT 1	MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2.1U56	156-0914-02	OPT 1	MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A2.1U57	118-1467-00	OPT 1	MICROCIRCUIT,DI:8 BIT BIDIRECTIONAL	23241	801805-001
A2.1U58	118-1530-00	OPT 1	TRANSISTOR:	23241	801828-001

ILLUSTRATED PARTS LIST

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A3	118-1250-01		CKT BOARD ASSY:PROCESSOR	23241	261155-001
A3M1	118-1598-00		MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	118-1598-00
A3M2	118-1597-00		MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	118-1597-00
A3M3	118-1599-00		MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	118-1599-00
A3M4	118-1600-00		MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	118-1600-00
A3M5	118-1150-01		MICROCIRCUIT,DI:2048 X 8 ROM,PRGM	80009	118-1150-01
A3A1	118-1250-XX		CKT BOARD ASSY:PROCESSOR (NOT AVAILABLE,SEE A3)		
A3A1C1	281-0757-00		CAP.,FXD,CER DI:10PF,20%,100V	72982	8035-D-COG-100G
A3A1C2	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C3	290-0301-00		CAP.,FXD,ELCTLT:10UF,10%,20V	56289	150D106X9020B2
A3A1C4	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C5	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C6	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C7	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C8	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C9	281-0775-00		CAP.,FXD,CER DI:0.1UF,20%,50V	04222	SA205E104MAA
A3A1C10	281-0775-00		CAP.,FXD,CER DI:0.1UF,20%,50V	04222	SA205E104MAA
A3A1C12	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C14	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C15	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C16	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C17	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C18	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C19	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C20	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C21	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C22	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C23	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C24	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C25	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C26	290-0162-00		CAP.,FXD,ELCTLT:22UF,20%,35V	12954	D22C35M1
A3A1C27	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C28	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C29	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C30	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C31	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C32	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C33	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C35	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C36	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C37	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C38	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C39	290-0134-00		CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A3A1C41	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C42	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C43	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C44	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C45	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C46	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C47	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C48	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C49	290-0134-00		CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A3A1C51	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3A1C52	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102

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Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A3A1C53	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C54	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C55	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1C56	118-1462-00		CAP.,FXD,ELCTLT:1000PF,20%,50V	23241	801311-102
A3A1CR1	152-0279-00		SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL
A3A1R1	315-0681-00		RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A3A1R3	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R4	315-0150-00		RES.,FXD,CMPSN:15 OHM,5%,0.25W	01121	CB1505
A3A1R5	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R6	315-0680-00		RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A3A1R7	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R8	118-1433-00		RES.,VAR,WW:10K OHM,0.24%,1W	23241	800150-103
A3A1R9	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R10	118-1433-00		RES.,VAR,WW:10K OHM,0.24%,1W	23241	800150-103
A3A1R12	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R14	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R17	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R18	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3A1R19	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R20	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R21	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R22	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R23	315-0221-00		RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A3A1R27	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R28	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R29	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R30	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R31	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R33	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3A1R35	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R36	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A3A1R37	315-0182-00		RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A3A1R38	303-0121-00		RES.,FXD,CMPSN:120 OHM,5%,1W	01121	GB1215
A3A1R39	303-0121-00		RES.,FXD,CMPSN:120 OHM,5%,1W	01121	GB1215
A3A1R40	315-0182-00		RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A3A1R41	315-0150-00		RES.,FXD,CMPSN:15 OHM,5%,0.25W	01121	CB1505
A3A1R45	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3A1R47	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A3A1R48	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A3A1RP3	118-1431-00		MICROCIRCUIT,DI:RESISTOR	23241	801006-681
A3A1RP4	118-1431-00		MICROCIRCUIT,DI:RESISTOR	23241	801006-681
A3A1TP1	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A3A1TP2	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A3A1TP3	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A3A1TP4	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A3A1TP5	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A3A1U1	156-0945-00		MICROCIRCUIT,DI:CLOCK GENERATOR/DRIVER	34649	D8224
A3A1U2	156-0954-00		MICROCIRCUIT,DI:8 BIT MICROPROCESSOR	80009	156-0954-00
A3A1U3	156-0385-02		MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A3A1U4	156-0078-02		MICROCIRCUIT,DI:1 OF 16 DECODER DEMUX,SCRN	01295	SN74154
A3A1U6	156-0706-00		MICROCIRCUIT,DI:DUAL MONOSTABLE MV	01295	SN74221N
A3A1U8	156-0469-02		MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A3A1U9	156-0382-02		MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A3A1U10	156-0645-02		MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A3A1U11	156-0041-05		MICROCIRCUIT,DI:DUAL D-TYPE FF,BURN-IN	01295	SN7474
A3A1U12	156-0041-05		MICROCIRCUIT,DI:DUAL D-TYPE FF,BURN-IN	01295	SN7474
A3A1U13	156-0385-02		MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04

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Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A3A1U14	156-1461-00		MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A3A1U15	156-1461-00		MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A3A1U16	156-0480-02		MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A3A1U19	156-0947-00		MICROCIRCUIT,DI:SYSTEM CONTROLLER/BUS DRVR	34649	D8228
A3A1U20	156-0480-02		MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A3A1U21	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A3A1U22	156-0982-02		MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-02
A3A1U23	156-0865-01		MICROCIRCUIT,DI:OCTAL D FLIP-FLOP W/CLEAR	80009	156-0865-01
A3A1U24	156-0865-01		MICROCIRCUIT,DI:OCTAL D FLIP-FLOP W/CLEAR	80009	156-0865-01
A3A1U25	156-0865-01		MICROCIRCUIT,DI:OCTAL D FLIP-FLOP W/CLEAR	80009	156-0865-01
A3A1U26	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A3A1U27	118-1467-00		MICROCIRCUIT,DI:8 BIT BIDIRECTIONAL	23241	801805-001
A3A1U28	118-1467-00		MICROCIRCUIT,DI:8 BIT BIDIRECTIONAL	23241	801805-001
A3A1U29	156-0865-01		MICROCIRCUIT,DI:OCTAL D FLIP-FLOP W/CLEAR	80009	156-0865-01
A3A1U30	156-0865-01		MICROCIRCUIT,DI:OCTAL D FLIP-FLOP W/CLEAR	80009	156-0865-01
A3A1U31	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A3A1U34	156-0721-02		MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A3A1U35	118-1544-00		MICROCIRCUIT,DI:PERIPHERAL DRIVERS	23241	801798-003
A3A1U36	156-0383-02		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A3A1U37	156-0383-02		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A3A1U38	156-0385-02		MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A3A1U39	156-0385-02		MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A3A1U40	156-0385-02		MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A3A1U41	156-0383-02		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A3A1U42	156-0383-02		MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A3A1Y1	158-0136-00		XTAL UNIT,QTZ:18.432 MHZ 0.01% SERIES	33096	CCAT 101123

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Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A4	118-1249-00		CKT BOARD SSY:MOTOR DRIVER	23241	261660-001
A4C1	281-0773-00		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A4C2	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C3	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4C4	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C5	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C6	281-0851-00		CAP.,FXD,CER DI:180PF,5%,100VDC	20932	401E0100AD181J
A4C7	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4C8	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C9	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C10	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C11	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4C12	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C13	281-0812-00		CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A4C14	281-0773-00		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A4C15	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C16	281-0707-00		CAP.,FXD,CER DI:15000PF,20%,100V	20932	402EM200AD153K
A4C17	281-0812-00		CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A4C18	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C19	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C20	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C21	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C22	290-0488-00		CAP.,FXD,ELCTLT:2.2UF,10%,20V	90201	TAC225K020P02
A4C24	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C26	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C27	290-0167-00		CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A4C28	290-0167-00		CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A4C30	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C31	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4C32	281-0707-00		CAP.,FXD,CER DI:15000PF,20%,100V	20932	402EM200AD153K
A4C33	281-0773-00		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A4C34	290-0117-00		CAP.,FXD,ELCTLT:50UF,+75-10%,50V	56289	30D506G050DD9
A4C35	290-0117-00		CAP.,FXD,ELCTLT:50UF,+75-10%,50V	56289	30D506G050DD9
A4C36	290-0301-00		CAP.,FXD,ELCTLT:10UF,10%,20V	56289	150D106X9020B2
A4C37	290-0167-00		CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A4C38	290-0301-00		CAP.,FXD,ELCTLT:10UF,10%,20V	56289	150D106X9020B2
A4C39	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A4CR1	152-0123-00		SEMICOND DEVICE:ZENER,0.5W,9V,5%	04713	SZ11530RL
A4CR2	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR3	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR4	118-1489-00		SEMICOND DEVICE:	23241	800592-001
A4CR5	152-0647-00		SEMICOND DEVICE:ZENER,0.4W,6.8V,5%	04713	SZG35014K3RL
A4CR6	152-0809-00		SEMICOND DEVICE:ZENER,SI,12V,5%,5W	23241	801835-001
A4CR7	152-0414-00		SEMICOND DEVICE:SILICON,200V,0.75A	12969	UTR308
A4CR8	118-1484-00		SEMICOND DEVICE:90MA,80MW	23241	801834-001
A4CR9	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR10	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR11	118-1486-00		SEMICOND DEVICE:ZEN,3.34,5,DPC-120	23241	800602-001
A4CR12	152-0688-00		SEMICOND DEVICE:ZENER,2.4V,5%,0.4W	04713	1N4370A
A4CR13	152-0809-00		SEMICOND DEVICE:ZENER,SI,12V,5%,5W	23241	801835-001
A4CR14	152-0414-00		SEMICOND DEVICE:SILICON,200V,0.75A	12969	UTR308
A4CR15	152-0809-00		SEMICOND DEVICE:ZENER,SI,12V,5%,5W	23241	801835-001
A4CR16	152-0414-00		SEMICOND DEVICE:SILICON,200V,0.75A	12969	UTR308
A4CR18	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR19	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR20	118-1484-00		SEMICOND DEVICE:90MA,80MW	23241	801834-001
A4CR21	152-0414-00		SEMICOND DEVICE:SILICON,200V,0.75A	12969	UTR308

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Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A4CR22	118-1483-00		SEMICOND DEVICE:3A,100V	23241	801769-001
A4CR23	152-0784-00		SEMICOND DEVICE:RECT,SI,FAST RCVY,200V,5.0	04713	SR3688
A4CR24	152-0784-00		SEMICOND DEVICE:RECT,SI,FAST RCVY,200V,5.0	04713	SR3688
A4CR25	152-0784-00		SEMICOND DEVICE:RECT,SI,FAST RCVY,200V,5.0	04713	SR3688
A4CR26	152-0784-00		SEMICOND DEVICE:RECT,SI,FAST RCVY,200V,5.0	04713	SR3688
A4CR27	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR28	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4CR29	152-0024-00		SEMICOND DEVICE:ZENER,1W,15V,5%	04713	1N3024B
A4F1	159-0019-00		FUSE,CARTRIDGE:3AG,1A,250V,SLOW BLOW	71400	MDL1
A4F2	159-0160-00		FUSE,CARTRIDGE:3AG,1.5 A,250V,18 SEC,UL	71400	MDX 1-1/2
A4F3	159-0005-00		FUSE,CARTRIDGE:3AG,3A,125V,30 SEC,CER	71400	MDA3
A4F4	159-0005-00		FUSE,CARTRIDGE:3AG,3A,125V,30 SEC,CER	71400	MDA3
A4Q1	118-1540-00		TRANSISTOR:	23241	801829-001
A4Q2	151-0301-00		TRANSISTOR:SILICON,PNP	27014	2N2907A
A4Q3	151-0301-00		TRANSISTOR:SILICON,PNP	27014	2N2907A
A4Q4	118-1515-00		TRANSISTOR:	23241	801752-001
A4Q5	118-1540-00		TRANSISTOR:	23241	801829-001
A4Q6	151-0301-00		TRANSISTOR:SILICON,PNP	27014	2N2907A
A4Q7	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A4Q8	118-1540-00		TRANSISTOR:	23241	801829-001
A4Q9	151-0301-00		TRANSISTOR:SILICON,PNP	27014	2N2907A
A4Q10	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A4Q11	118-1520-00		TRANSISTOR:	23241	801828-001
A4Q12	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A4Q13	151-0301-00		TRANSISTOR:SILICON,PNP	27014	2N2907A
A4Q14	118-1540-00		TRANSISTOR:	23241	801829-001
A4Q15	118-1436-00		TRANSISTOR:	23241	801751-001
A4Q16	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A4Q17	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A4R1	321-0289-00		RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A4R2	321-0289-00		RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A4R3	321-0193-00		RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A4R4	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A4R5	118-2215-00		RES.,VAR,WW:TRIMMER 220 OHM,1W,LINEAR	23241	800150-201
A4R6	315-0224-00		RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A4R7	315-0512-00		RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A4R8	315-0104-00		RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A4R9	315-0224-00		RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A4R10	315-0684-00		RES.,FXD,CMPSN:680K OHM,5%,0.25W	01121	CB6845
A4R11	315-0224-00		RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A4R12	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R13	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R14	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R15	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R16	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R17	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R18	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R19	321-0193-00		RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A4R20	321-0211-00		RES.,FXD,FILM:1.54K OHM,1%,0.125W	91637	MFF1816G15400F
A4R21	315-0221-00		RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A4R22	321-0275-00		RES.,FXD,FILM:7.15K OHM,1%,0.125W	91637	MFF1816G71500F
A4R23	315-0332-00		RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A4R24	315-0332-00		RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A4R25	315-0123-00		RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A4R26	321-0193-00		RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A4R27	308-0828-00		RES.,FXD,WW:0.1 OHM,1%,3W	91637	RS-2B-ER1000F
A4R28	321-0193-00		RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F

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Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A4R29	315-0471-00		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A4R30	315-0471-00		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A4R31	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R32	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A4R33	308-0828-00		RES.,FXD,WW:0.1 OHM,1%,3W	91637	RS-2B-ER1000F
A4R34	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R35	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R36	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R37	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R38	315-0752-00		RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A4R39	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R40	315-0393-00		RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A4R41	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R42	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R43	315-0104-00		RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A4R44	315-0680-00		RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A4R45	321-0211-00		RES.,FXD,FILM:1.54K OHM,1%,0.125W	91637	MFF1816G15400F
A4R46	315-0680-00		RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A4R47	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R48	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A4R49	308-0828-00		RES.,FXD,WW:0.1 OHM,1%,3W	91637	RS-2B-ER1000F
A4R50	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4R51	301-0122-00		RES.,FXD,CMPSN:1.2K OHM,5%,0.50W	01121	EB1225
A4R52	315-0273-00		RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A4R53	315-0151-00		RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A4R54	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R55	315-0332-00		RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A4R56	315-0471-00		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A4R57	315-0471-00		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A4R58	315-0682-00		RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A4RP1	118-1530-00		RES NTWK,FXD,FI:7.5K OHMS	23241	801006-752
A4RP2	118-1530-00		RES NTWK,FXD,FI:7.5K OHMS	23241	801006-752
A4TP1	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A4TP2	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A4TP3	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A4TP4	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A4TP5	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A4U1	156-0105-00		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM301AN
A4U2	156-0105-00		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM301AN
A4U3	156-0105-00		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM301AN
A4U4	156-0384-02		MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS03
A4U5	156-0402-00		MICROCIRCUIT,LI:TIMER	27014	LM555CN
A4U6	118-1559-00		MICROCIRCUIT,DI:ANALOG SWITCHES	23241	801879-001
A4U7	156-0105-00		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM301AN
A4U8	156-0730-02		MICROCIRCUIT,DI:QUAD 2-INP NOR BFR,BURN-IN	01295	SN74LS33
A4U9	156-0143-02		MICROCIRCUIT,DI:RETRIG ONE SHOT,W/CLEAR	80009	156-0143-02
A4U10	156-0411-00		MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A4U11	156-0384-02		MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS03
A4U12	156-0030-03		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	27014	DM8000

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A5	118-1285-00		CKT BOARD ASSY:WIRE DRIVER	23241	249910-001
A5C1	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C2	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C3	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C4	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C5	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C6	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C7	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C8	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C9	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C10	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C11	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C12	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C13	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C14	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A5C15	118-1547-00		CAP.,FXD,ELCTLT:10UF,36V	23241	801942-001
A5C16	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A5C17	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A5C18	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A5C19	290-0134-00		CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A5C20	290-0117-00		CAP.,FXD,ELCTLT:50UF,+75-10%,50V	56289	30D506G050DD9
A5C21	290-0117-00		CAP.,FXD,ELCTLT:50UF,+75-10%,50V	56289	30D506G050DD9
A5CR1	118-1489-00		SEMICOND DEVICE:	23241	800592-001
A5CR2	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR3	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR4	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR5	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR6	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR7	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR8	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR9	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR10	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR11	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR12	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR13	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR14	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR15	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR16	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR17	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR18	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR19	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR20	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR21	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR22	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR23	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR24	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR25	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR26	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR27	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR28	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR29	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5F1	118-1253-00		FUSE,CARTRIDGE:1.25A	23241	801906-125
A5F2	118-1253-00		FUSE,CARTRIDGE:1.25A	23241	801906-125
A5F3	118-1253-00		FUSE,CARTRIDGE:1.25A	23241	801906-125
A5F4	118-1253-00		FUSE,CARTRIDGE:1.25A	23241	801906-125
A5F5	118-1253-00		FUSE,CARTRIDGE:1.25A	23241	801906-125
A5F6	118-1253-00		FUSE,CARTRIDGE:1.25A	23241	801906-125

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A5F7	118-1253-00		FUSE, CARTRIDGE:1.25A	23241	801906-125
A5Q1	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q2	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q3	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q4	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q5	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q6	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q7	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q8	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q9	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q10	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q11	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q12	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q13	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q14	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A5Q15	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q16	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q17	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q18	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q19	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q20	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q21	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q22	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q23	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q24	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q25	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q26	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q27	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q28	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q29	118-1520-00		TRANSISTOR:	23241	801828-001
A5Q30	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q31	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q32	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q33	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q34	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q35	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q36	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q37	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q38	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q39	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q40	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q41	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q42	118-1540-00		TRANSISTOR:	23241	801829-001
A5Q43	118-1540-00		TRANSISTOR:	23241	801829-001
A5R1	311-0658-00		RES.,VAR,WW:500 OHM,1W	75042	100-0000-501
A5R2	315-0271-00		RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A5R3	118-2216-00		RES.,FXD,CMPSN:680 OHM,5%,1W	23241	800032-681
A5R4	315-0822-00		RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A5R5	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R6	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R7	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R8	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R9	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R10	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R11	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R12	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R13	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100

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A5R14	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	80084-100
A5R15	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R16	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R17	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R18	118-1539-00		RES.,FXD,FILM:1.0 OHM,1%,3W	23241	800084-100
A5R19	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A5TP1	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A5U1	118-1541-00		RES NTKW,FXD,FI:680 OHMS	23241	801957-681
A5U2	118-1545-00		RES NTKW,FXD,FI:820 OHMS	23241	801957-821
A5U3	118-1542-00		RES NTKW,FXD,FI:1.5K OHMS	23241	801957-152
A5U4	118-1543-00		RES NTKW,FXD,FI:2.7K OHMS	23241	801957-272
A5U5	118-1541-00		RES NTKW,FXD,FI:680 OHMS	23241	801957-681
A5U7	118-1541-00		RES NTKW,FXD,FI:680 OHMS	23241	801957-681
A5U8	118-1545-00		RES NTKW,FXD,FI:820 OHMS	23241	801957-821
A5U9	118-1543-00		RES NTKW,FXD,FI:2.7K OHMS	23241	801957-272
A5U10	118-1543-00		RES NTKW,FXD,FI:2.7K OHMS	23241	801957-272
A5U11	118-1541-00		RES NTKW,FXD,FI:680 OHMS	23241	801957-681
A5U12	156-0030-03		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	27014	DM8000
A5U13	118-1544-00		MICROCIRUCIT,DI:PERIPHERAL DRIVERS	23241	801798-003
A5U14	118-1544-00		MICROCIRUCIT,DI:PERIPHERAL DRIVERS	23241	801798-003
A5U15	118-1543-00		RES NTKW,FXD,FI:2.7K OHMS	23241	801957-272
A5U16	156-0030-03		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	27014	DM8000
A5U17	118-1544-00		MICROCIRUCIT,DI:PERIPHERAL DRIVERS	23241	801798-003
A5U18	118-1544-00		MICROCIRUCIT,DI:PERIPHERAL DRIVERS	23241	801798-003
A5U19	156-0030-03		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	27014	DM8000
A5U20	118-1542-00		RES NTKW,FXD,FI:1.5K OHMS	23241	801957-152
A5U21	118-1544-00		MICROCIRUCIT,DI:PERIPHERAL DRIVERS	23241	801798-003
A5U22	118-1544-00		MICROCIRUCIT,DI:PERIPHERAL DRIVERS	23241	801798-003
A5U23	156-0030-03		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	27014	DM8000
A5U24	118-1544-00		MICROCIRUCIT,DI:PERIPHERAL DRIVERS	23241	801798-003

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Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A6	118-1251-00		CKT BOARD ASSY:REGULATOR	23241	249785-001
A6C1	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A6C2	290-0177-00		CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A6C3	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A6C4	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A6C5	118-1469-00		CAP.,FXD,ELCTLT:2.2UF,10%,50V	23241	800090-225
A6C6	290-0177-00		CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A6C7	281-0772-00		CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A6C8	290-0177-00		CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A6C9	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A6C10	290-0177-00		CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A6C11	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A6C12	118-2217-00		CAP.,FXD,CER DI:0.32UF,10%,50V	23241	800090-334
A6CR1	152-0757-00		SEMICON D DEVICE:ZENER,SI,6.2V,5%,1W	04713	1N4735A
A6CR2	118-1439-00		SEMICON DVC DI:SIL,200V,1W	23241	800095-001
A6CR3	152-0746-00		SEMICON D DEVICE:ZENER,SI,14V,1%,1W	23241	801827-005
A6CR4	118-1439-00		SEMICON DVC DI:SIL,200V,1W	23241	800095-001
A6CR5	118-1439-00		SEMICON DVC DI:SIL,200V,1W	23241	800095-001
A6CR6	152-0746-00		SEMICON D DEVICE:ZENER,SI,14V,1%,1W	23241	801827-005
A6CR7	118-1439-00		SEMICON DVC DI:SIL,200V,1W	23241	800095-001
A6F1	159-0013-00		FUSE,CARTRIDGE:3AG,6A,125V,7SEC	71400	MTH6
A6F2	159-0025-00		FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC 1/2
A6F3	159-0025-00		FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC 1/2
A6Q1	118-1436-00		TRANSISTOR:	23241	801751-001
A6Q2	151-0302-00		TRANSISTOR:SILICON,NPN	07263	S038487
A6Q3	118-1438-00		RECTIFIER:50V,8A	23241	801887-001
A6Q4	118-1438-00		RECTIFIER:50V,8A	23241	801887-001
A6Q5	118-1438-00		RECTIFIER:50V,8A	23241	801887-001
A6R1	303-0101-00		RES.,FXD,CMPSN:100 OHM,5%,1W	01121	CB1015
A6R2	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A6R3	308-0828-00		RES.,FXD,WW:0.1 OHM,1%,3W	91637	RS-2B-ER1000F
A6R4	308-0828-00		RES.,FXD,WW:0.1 OHM,1%,3W	91637	RS-2B-ER1000F
A6R5	118-1494-00		RES.,VAR,WW:1K OHM,0.52%,1W	23241	800150-102
A6R6	321-0257-00		RES.,FXD,FILM:4.64K OHM,1%,0.125W	91637	MFF1816G46400F
A6R7	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A6R8	321-0211-00		RES.,FXD,FILM:1.54K OHM,1%,0.125W	91637	MFF1816G15400F
A6R9	315-0220-00		RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A6R10	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A6R11	321-0205-00		RES.,FXD,FILM:1.33K OHM,1%,0.125W	91637	MFF1816G13300F
A6R12	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A6R13	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A6TP1	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A6U1	156-0071-00		MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC1723CL
A6U2	118-1435-00		MICROCIRCUIT,DI:REGULATOR,12V	23241	801205-112
A6U3	118-1457-00		MICROCIRCUIT,LI:+12V REGULATOR	23241	801204-012

ILLUSTRATED PARTS LIST

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A7	118-1271-00		CKT BOARD ASSY:MOTHER	23241	249865-001
A7C1	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A7C2	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A7C3	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A7C4	283-0421-00		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A7C5	290-0312-00		CAP.,FXD,ELCTLT:47UF,10%,35V	56289	150D476X9035S2
A7J1	118-1511-00		CONN,RCPT,ELEC:60 PIN,CARD EDGE	23241	800042-002
A7J2	118-1511-00		CONN,RCPT,ELEC:60 PIN,CARD EDGE	23241	800042-002
A7J3	118-1429-00		CONN,RCPT,ELEC:HEAD	23241	801908-001
A7J4	118-1505-00		CONN,RCPT,ELEC:HEADER PLZD,2.54MM CENTERS	23241	801909-001
A7J5	118-1505-00		CONN,RCPT,ELEC:HEADER PLZD,2.54MM CENTERS	23241	801909-001
A7J6	118-1504-00		CONN,RCPT,ELEC:HEADER,PLZD,3.96MM CENTERS	23241	801885-002
A7J7	118-1525-00		CONN,RCPT,ELELC:HEADER,PLZD,3.96MM	23241	801885-001
A7J8	118-1505-00		CONN,RCPT,ELEC:HEADER PLZD,2.54MM CENTERS	23241	801909-001
A7J9	118-1526-00		CONN,RCPT,ELECT:HEADER,PLZD,2.4MM CENTERS	23241	801909-002
A7J10	118-1507-00		CONN,RCPT ELECT:12 PIN HEADER	23241	301882-001
A7J11	118-1429-00		CONN,RCPT,ELEC:HEAD	23241	801908-001
A7S14	260-1721-00		SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	435166-5
A7S15	260-1721-00		SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	435166-5
A7TP1	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A7TP2	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00

ILLUSTRATED PARTS LIST

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A8	118-1157-00		CKT BOARD ASSY:CONTROL PANEL	23241	245865-016
A8J10	118-1429-00		CONN,RCPT,ELEC:HEAD	23241	801908-001
A8L4	118-1170-00		LAMP,INCAND:#73	23241	801931-001
A8L7	118-1170-00		LAMP,INCAND:#73	23241	801931-001
A8S1	118-1159-00		SWITCH,ROCKER:SPDT	23241	801932-001
A8S2	118-1159-00		SWITCH,ROCKER:SPDT	23241	801932-001
A8S3	118-1159-00		SWITCH,ROCKER:SPDT	23241	801932-001
A8S4	118-1303-00		SWITCH,PUSH:	23241	801932-001
A8S5	118-1303-00		SWITCH,PUSH:	23241	801932-001
A8S6	118-1303-00		SWITCH,PUSH:	23241	801932-001
A8S7	118-1303-00		SWITCH,PUSH:	23241	801932-001
A8S8	118-1288-00		SWITCH,ROTARY:16 POSITION	23241	801953-001
A8U1	118-1140-00		LT EMITTING DIODE:STATUS DISPLAY	23241	801996-001
A8U2	118-1140-00		LT EMITTING DIODE:STATUS DISPLAY	23241	801996-001
A8W2	118-1141-00		WIRING HARNESS:CONTROL PANEL	23241	245829-001
A11	118-1318-XX		POWER SUPPLY COMPONENTS:(NOT ORDERABLE)		
A11B1	118-1293-00		FAN ASSY:	23241	245899-001
A11C1	118-1420-00		CAP.,FXD,ELCTLT:68K UF,30V	23241	800092-301
A11C2	118-1420-00		CAP.,FXD,ELCTLT:68K UH,30V	23241	80092-301
A11C3	118-1145-00		CAP.,FXD,ELCTLT:77UF,15V	23241	800092-158
A11C4	118-1419-00		CAP.,FXD,ELCTLT:3UF,6%,660V	23241	801944-003
A11CR1	118-1418-00		BRIDGE RECT:	23241	801837-001
A11CR2	118-1418-00		BRIDGE RECT:	23241	801837-001
A11F1	159-0160-00,A1,2,3,4		FUSE,CARTRIDGE:3AG,1.5 A,250V,18 SEC,UL	71400	MDX 1-1/2
A11F1	159-0005-00		FUSE,CARTRIDGE:3AG,3A,125V,30 SEC,CER	71400	MDA3
A11F2	159-0046-00		FUSE,CARTRIDGE:3AG,8A,250V,MED-BLOW	71400	ABC 8
A11L1	118-1417-00		FILTER,LINE:	23241	801930-001
A11R1	118-1416-00		PWR RES ASSY:	23241	245890-001
A11R2	118-1416-00		PWR RES ASSY:	23241	245890-001
A11S1	118-1311-00		SWITCH,ROCKER:DPST,AC POWER	23241	810137-001
A11S2	118-1415-00		THERMOSTAT,ASSY:	23241	245894-001
A11T1	118-1414-00		XFMR ASSY:	23241	118-1414-00
A11TB1	118-1413-00		BLOCK,TERMINAL:	23241	801955-001
A11TB2	118-1412-00		BLOCK,TERMINAL:	23241	801955-002

[illegible]

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000 Part first added at this serial number

00X Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component

Attaching parts for Assembly and/or Component

---*---

Detail Part of Assembly and/or Component

Attaching parts for Detail Part

---*---

Parts of Detail Part

Attaching parts for Parts of Detail Part

---*---

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol ---*--- indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICON	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVEING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OB	ORDER BY DESCRIPTION	SO	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W/	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDNT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

ILLUSTRATED PARTS LIST

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
S3109	FELLER ASA ADOLF AG., C/O PANEL COMPONENTS CORP.	355 TESCONI CIRCLE	SANTA ROSA, CA 95401
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
28520	HEYMAN MFG. CO.	147 N. MICHIGAN AVE.	KENILWORTH, NJ 07033
71400	BUSSMAN MFG., DIVISION OF MCGRAW- EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
76381	MINNESOTA MINING AND MFG. CO.	3M CENTER	ST. PAUL, MN 55101
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80126	PACIFIC ELECTRICORD CO.	747 W. REDONDO BEACH, P O BOX 10	GARDENA, CA 90247

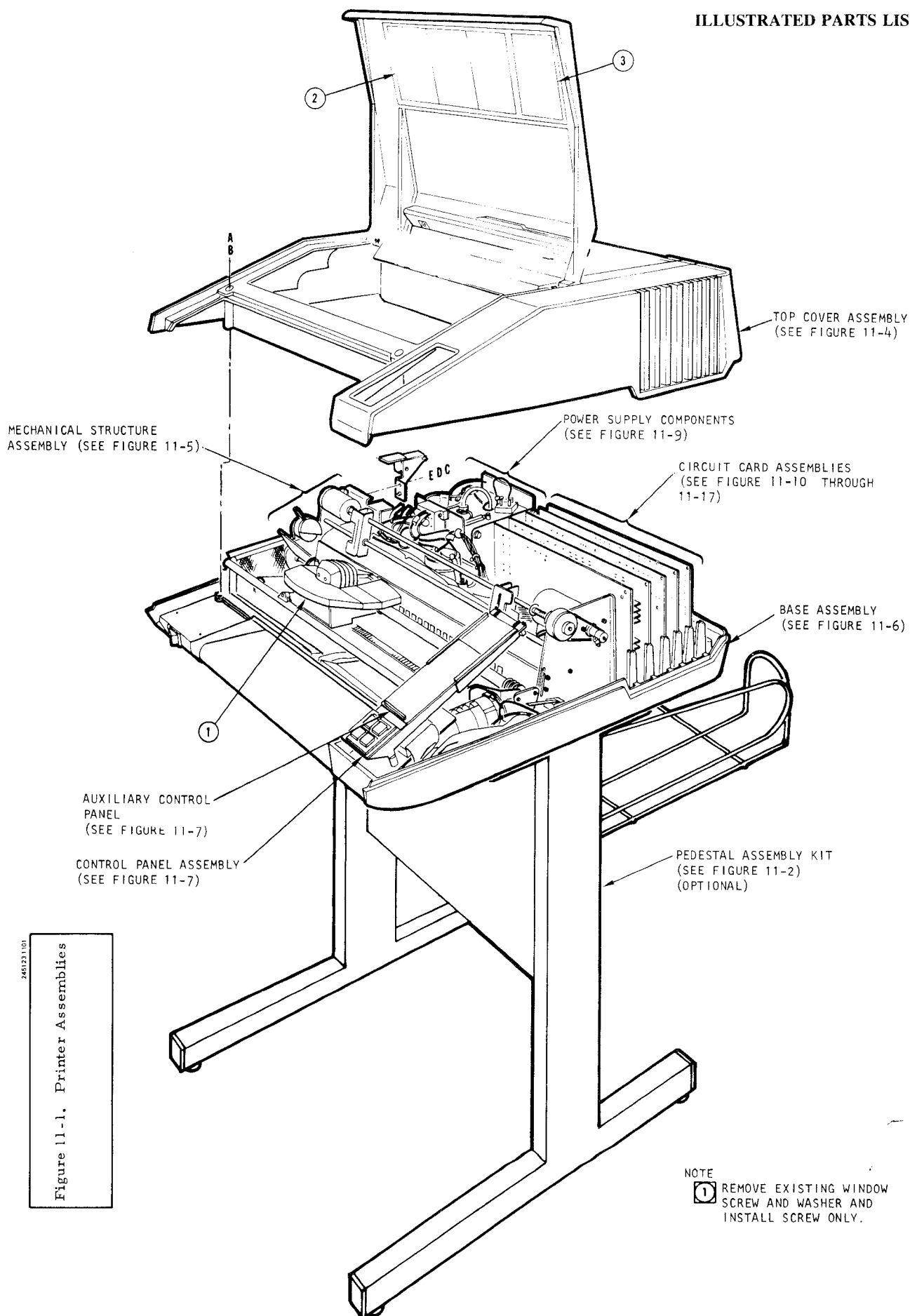
ILLUSTRATED PARTS LIST

SOME PARTS, SUCH AS COMMON HARDWARE ITEMS, OPTIONAL ASSEMBLIES, AND CONTROL PANEL BUTTONS AND LAMPS, ARE AVAILABLE ONLY AS PART OF A KIT. IN (EPROM) INTEGRATED CIRCUITS THAT ARE USED WITH THE CIRCUIT BOARD ASSEMBLIES.

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-1		PRINTER ASSEMBLIES									
11-2		PEDESTAL ASSEMBLY KIT(OPTION) AND PAPER BASKET (OPTION)									
11-4		TOP COVER ASSEMBLY									
11-5		MECHANICAL STRUCTURE AND TRACTOR DRIVE ASSEMBLIES									
11-6		BASE ASSEMBLY									
11-7		CONTROL PANEL ASSEMBLY									
11-9		POWER SUPPLY COMPONENTS									
11-10		REGULATOR CIRCUIT BOARD ASSEMBLY									
11-11		WIRE DRIVER CIRCUIT BOARD ASSEMBLY									
11-12		MOTOR DRIVER CIRCUIT BOARD ASSEMBLY									
11-13		PROCESSOR CIRCUIT BOARD ASSEMBLY									
11-14		DPC SHORT LINE PARALLEL INTERFACE CIRCUIT BOARD ASSEMBLY									
11-16		SERIAL INTERFACE CIRCUIT BOARD ASSEMBLY									
11-18		MOTHER BOARD CIRCUIT BOARD ASSEMBLY									
11-19		ADAPTER CABLE ASSEMBLIES									
11-21		HEAD HARNESS ROUTING DIAGRAM									
11-22		SWITCH HARNESS ROUTING DIAGRAM									
11-23		COLUMN 1 HARNESS ROUTING DIAGRAM									
11-24		CONTROL PANEL HARNESS ROUTING DIAGRAM									
11-25		TIME METER CABLINE DIAGRAM									
11-26		AC HARNESS ROUTING DIAGRAM									
11-27		POWER HARNESS ROUTING DIAGRAM									
11-28		UNIVERSAL HARNESS ROUTING DIAGRAM									
11-29		FAN CABLINE DIAGRAM									
11-30		SERVO POWER HARNESS ROUTING DIAGRAM									
11-31		CONTROL PANEL BUTTON KIT									
11-32		KNOB ASSEMBLY KIT									
11-36		SPRING KIT									
11-37		HARDWARE KIT									

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-1	-----	-----	-						PRINTER ASSEMBLIES		
11-1	118-1314-00		1						CASSETTE ASSY,R	-----	261319-005
-2	118-1337-00		1						MARKER IDENT:INSTRUCTION	-----	249484-001
-3	118-1324-00		1						MARKER,IDNET:STATUS DISPLAY	-----	249502-001
	118-1552-00		1						HARDWARE KIT:4643	-----	249747-001
	-----	-----	-						(SEE FIG 11-37)		
-A	-----	-----	2						. SCREW,PNH STL M4 X 10MM		
-B	-----	-----	2						. WASHER FLAL,STL M4 X 9MM		
-C	-----	-----	1						. SCREW HEX HEAD M3 X 8MM		
-D	-----	-----	1						. WASHER,LOCK INTERNAL M3		
-E	-----	-----	1						. WASHER,FLAT:STL M3 X 7MM		



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Figure 11-1. Printer Assemblies

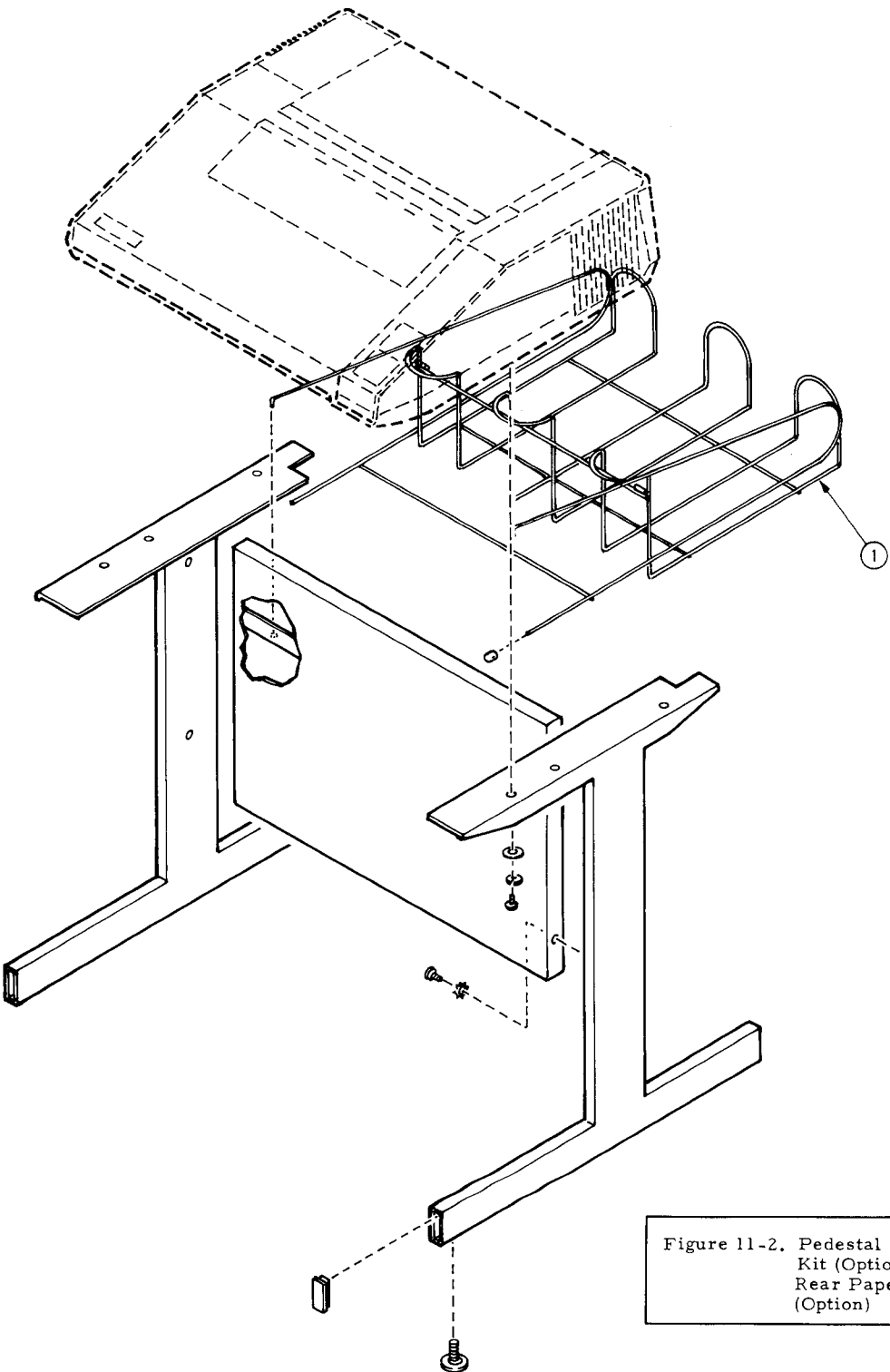


Figure 11-2. Pedestal Assembly
Kit (Option) and
Rear Paper Chute
(Option)

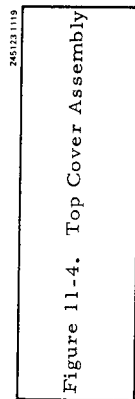
ILLUSTRATED PARTS LIST

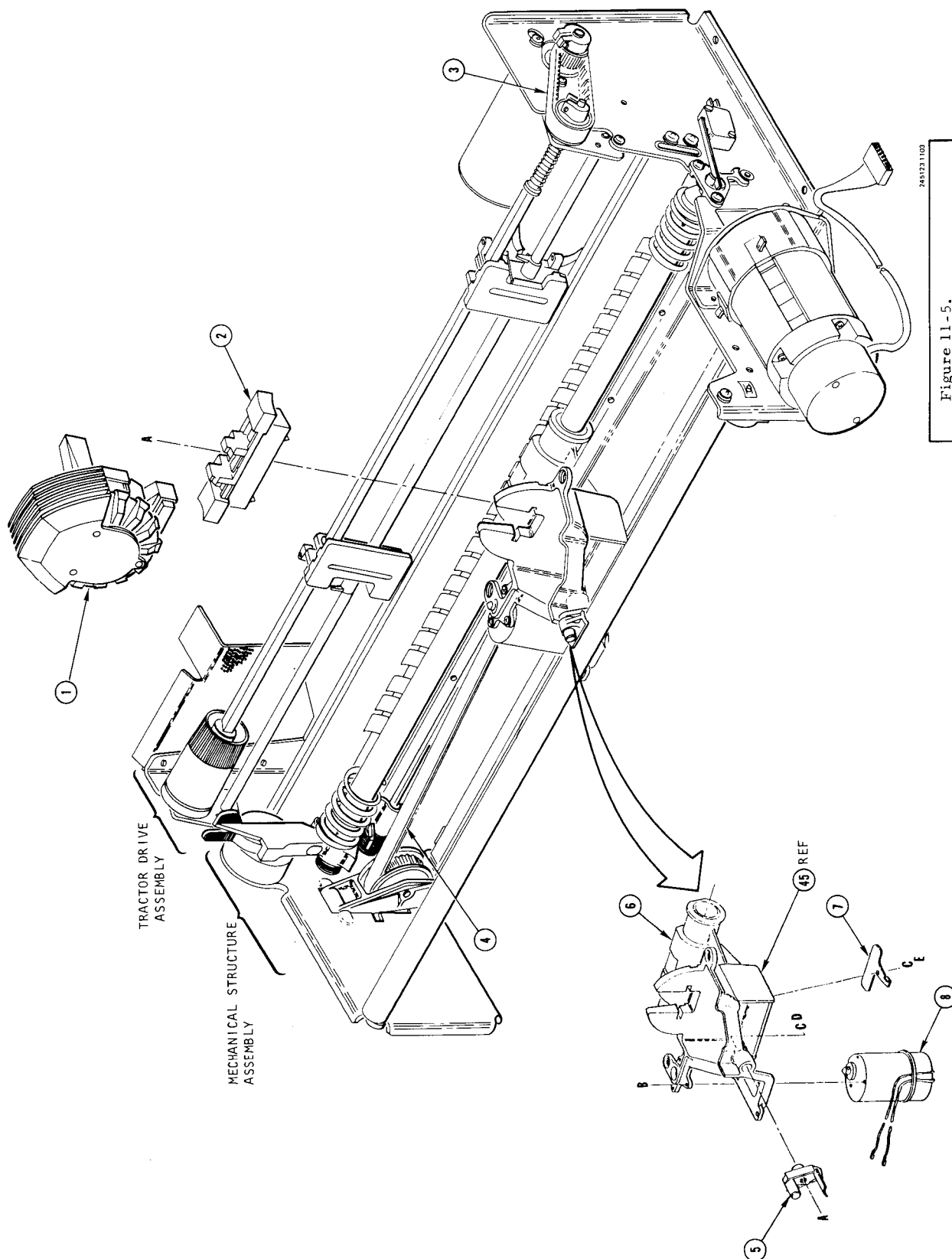
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-2	118-1335-00		1						PEDESTAL ASSY	-----	261406-019
-1	118-2358-00		1						CATCHER PAPER:	-----	261411-001
-2	118-2359-00		1						HARDWARE KIT:PEDISTAL	-----	261470-001

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-4	-----	-----	-						TOP COVER ASSEMBLY		
-1	118-2414-00		1						LID DOOR:	-----	261147-241
-2	118-1380-00		1						DAMPER, DOOR:	-----	801968-001
-3	-----		2						FASTENER: SPEED CLIP	-----	8010050-002
-4	118-1378-00		1						PIN, DAMPER:	-----	249507-001
-5	334-5023-00		1						MARKER IDENT: 4643	80009	334-5023-00
-6	118-1377-00		1						WINDOW:	-----	261442-001
-7	118-2409-00		2						HINGE DOOR: RIGHT AND LEFT	-----	261137-001
-8	118-1349-00		2						LATCH, COVER:	-----	801949-001
-9	118-2411-00		1						COVER, TOP:	-----	261144-001
-10	118-1373-00		1						SPRING, CONT PNL:	-----	245543-001
-11	118-2410-00		1						CLIP, CONT PNL: LOWER	-----	261349-001
-12	118-2406-00		1						SOUND CONT BATT: RIGHT	-----	261623-001
-13	118-2405-00		1						SOUND CONT BATT: LEFT	-----	261622-001
-14	118-2404-00		1						SOUND CONT BATT: PRONT	-----	261624-001
-15	118-2412-00		1						SOUND, CONT BATT:	-----	261430-001
-16	118-2399-00		1						SOUND CONT BATT: RIGHT FRONT	-----	261432-001
-17	118-2408-00		1						BATT: RIGHT REAR	-----	261529-001
-18	118-2403-00		1						PADDING SOUND; REAR BAFFLE, TOP COVER	-----	261433-001
-19	118-2402-00		1						SOUND CONT BATT: FRONT LEFT	-----	261528-001
-20	118-2401-00		1						SOUND CONT BATT: FRONT MIDDLE LEFT	-----	261527-001
-21	118-2400-00		1						SOUND CONT BATT: FRONT LEFT REAR	-----	261431-001
-22	-----		1						PADDING, SOUND: FAN	-----	261612-001
	118-1552-00		1						HARDWARE KIT: 4643		
	-----		-						(SEE HARDWARE KIT FIG 11-37)		
-A	-----		1						. SCREW, PNH, STL, M3 X 0.5 X 12MM		
-B	-----		1						. WASHER, LOCK, SPLIT STEEL M3, 5.9MM		
-C	-----		12						. WASHER, FLAT, STL M4, 9MM		
-D	-----		12						. SCREW, PNH, M4 X 8MM		
-E	-----		4						. SCREW, FLAT HEAD: M3 X 16MM		
-F	-----		4						. WASHER, FLAT HEAD, STL M3 X 7MM		
-G	-----		4						. NUT, HEX: STL M3 X 0.5MM		

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Figure 11-5,
Mechanical Structure and
Tractor Drive Assemblies
(Sheet 1 of 2)

11-11

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-5	-----	-----	-						TRACTOR DRIVE ASSEMBLY		
-1	118-1146-00		1						PRINTHEAD ASSY:	-----	245601-001
-2	118-1375-00		1						MOUNT, HEAD ASSY:	-----	249531-001
-3	118-1308-00		1						BELT TIMING: 103 TEETH	-----	801862-002
-4	118-1153-00		1						BELT TIMING: SHUTTLE DRIVE	-----	800299-018
-5	118-1152-00		1						BRACKET, BEARING: REAR SHUTTLE	-----	249684-001
-6	118-1376-00		1						BEARING ASSY: SHUTTLE	-----	249534-001
-7	118-1354-00		1						PL, INTERRUPTER	-----	245704-001
-8	118-1149-00		1						MOTOR ASSY: RIBBON DRIVE	-----	249610-001
	-----		-						(B5)		
-9	118-1309-00		1						TRACTOR: LEFT SIDE	-----	815908-003
	-----		-						NOTE: FIG 11-5 INDEX 10 SEE NEXT PAGE		
	-----		-						(SEE FIG 11-37)		
-A	-----		3						. SCREW PNH STL M3 X 22MM		
-B	-----		3						. SCREW, PAN HEAD, STEEL, M3 X 8MM		
-C	-----		2						. WASHER, LOCK, EXTERNAL TOOTH, STEEL M3MM		
-D	-----		2						. NUT, HEX STEEL LARGE PATTERN, M3 X 0.5MM		
-E	-----		1						. SCREW, PNH STL M3 X 10MM		
-F	-----		2						. RING RETAINING		
-G	-----		1						. WASHER, FLAT STL, M14		
-H	-----		1						. CLIP, STL		
-I	-----		2						. WASHER, FLAT STL M7, 14MM MAX OD		
-J	-----		1						. SCREW PNH STL, M2 X 10MM		
-K	-----		7						. NUT HEX, STL M2.5MM		
-L	-----		1						. SCREW, PNH, STL M3 X 4MM		
-M	-----		5						. WASHER, LOCK, SPLIT M3, 5.9MM MAX OD		
-N	-----		1						. SCREW, TAPTITE		
-O	-----		1						. WASHER, ADJUSTMENT KNOB		
-P	-----		1						. WASHER, SPRING WAVY		
-Q	-----		2						. SCREW, PNH STL, M4 X 6MM		
-R	-----		15						. WASHER, LOCK SPLIT, STL M4, 7.3MM MAX OD		
-S	-----		5						. SCREW, PNH STL, M4 X 10MM		
-T	-----		1						. WASHER, FRONT BAR		
-U	-----		2						. WASHER, FLAT M7, 14MM MAX OD		
-V	-----		1						. SCREW, CAP, SOCKET HEAD M3 X 12MM		
-W	-----		6						. SCREW, PNH STL, M3 X 6MM		
-X	-----		10						. WASHER, FLAT STL M4, 9MM MAX OD		
-Y	-----		4						. SCREW, PNH STL, M4 X 12MM		
-Z	-----		2						. SCREW, PNH STL, M2.5 X 16MM		
-AA	-----		4						. WASHER, FLAT, STL 2.5		
-BB	-----		2						. WASHER, LOCK SPLIT, STL 2.5MM		
-CC	-----		2						. WASHER, FLAT STL M3, 7MM MAX OD		
-DD	-----		6						. SCREW, PNH STL, M3 X 6MM		
-EE	-----		4						. SCREW, PNH STL, M4 X 8MM		
-FF	-----		5						. SCREW, PNH, STL, M4 X 10MM		

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	-----				- TRACTOR DRIVE CONTINUED		
-10	118-1351-00		1		SHAFT,DRIVE:	-----	254492-001
-11	118-1310-00		1		TRACTOR:RIGHT SIDE	-----	815908-004
-12	118-2239-00		1		SPRING,CLUTCH:PAPER FEED	-----	254350-001
-13	-----		1		STRAP,GROUNDING:TRACTOR DRIVE	-----	249628-001
-14	118-2234-00		1		PLATE ASSEMBLY:RIGHT	-----	261540-001
-15	118-1461-00		1		PLATE,ASSEMBLY:LEFT	-----	261051-001
-16	118-1460-00		1		CYLINDER,UNIV:	-----	245586-001
-17	118-1459-00		1		YOKE,UNIVERSAL:	-----	245585-001
-18	118-1458-00		1		HUB,UNIVERSAL:	-----	245584-001
-19	118-1551-00		1		SPRING,KIT:4643	-----	249748-001
-20	118-1148-00		1		MOTOR ASSEMBLY:STEPPING PAPER FEED	-----	245587-001
	-----				(B2)		
-21	118-1448-00		1		PULLEY,DRIVE:	-----	245557-001
-22	118-1449-00		1		SPLINE DRIVE:	-----	245558-001
-23	118-1447-00		1		COLLER:	-----	254499-001
-24	118-1551-00		1		SPRING KIT:4643	-----	249748-001
-25	118-1470-00		1		CAM,PLATEN GAF:	-----	245735-001
-26	118-1551-00		1		SPRING KIT:	-----	249748-001
-27	118-1445-00		1		LEVER CHUTE:PAPER	-----	272061-001
-28	118-1156-00		1		IDLE PULLEY ASSY:	-----	245759-001
-29	118-2238-00		1		BELT ASSY:TENSION ADJUSTER	-----	254186-001
-30	118-1443-00		1		CAP END:FRONT BAR RIGHT	-----	249791-001
-31	118-2235-00		2		BUMPER SPRING:SHUTTLE	-----	345741-001
-32	118-1551-00		1		SPRING KIT:4643	-----	249748-001
-33	118-1442-00		1		CAP END:PAPER TENSION LEFT	-----	245587-001
-34	118-1441-00		1		FINGER ASSY:	-----	254420-001
-35	118-1450-00		1		PLATEN:	-----	261602-001
-36	118-2237-00		1		TAPE,PLATEN:DAMPING	-----	815400-001
-37	118-1451-00		1		END CAP:PAPER TENSION LEFT	-----	245588-001
-38	118-1452-00		1		BEARING:FRONT BAR	-----	245731-001
-39	118-1158-00		1		SWITCH,SENS:BALL OPEN	-----	801970-001
-40	118-1477-00		1		BAR,SUPPORT:FRONT	-----	261599-001
-41	118-1478-00		1		BAR,SUPPORT:REAR GUIDE	-----	345746-001
-42	118-1144-00		1		SHUTTLE ASSY:	-----	245701-001
-43	118-1286-00		1		SLIDE GUIDE:REAR BAR	-----	245755-001
-44	118-1476-00		1		END CAP:FRONT BAR LEFT	-----	261600-001
-45	118-1147-00		1		DR CONT ASSY:SHUTTLE SERVO MOTOR W/ENCODER	-----	245758-001
-46	118-2232-00		1		FRAME ASSY:RIGHT	-----	261475-001
-47	-----		1		PADDING,SOUND:SIDEFRAME RIGHT	-----	249514-001
-48	118-2233-00		1		FRAME ASSY:LEFT	-----	261539-001
-49	-----		1		PADDING,SOUND:SIDEFRAME LEFT	-----	249513-001
	118-1552-00		1		HARDWARE KIT:4643		

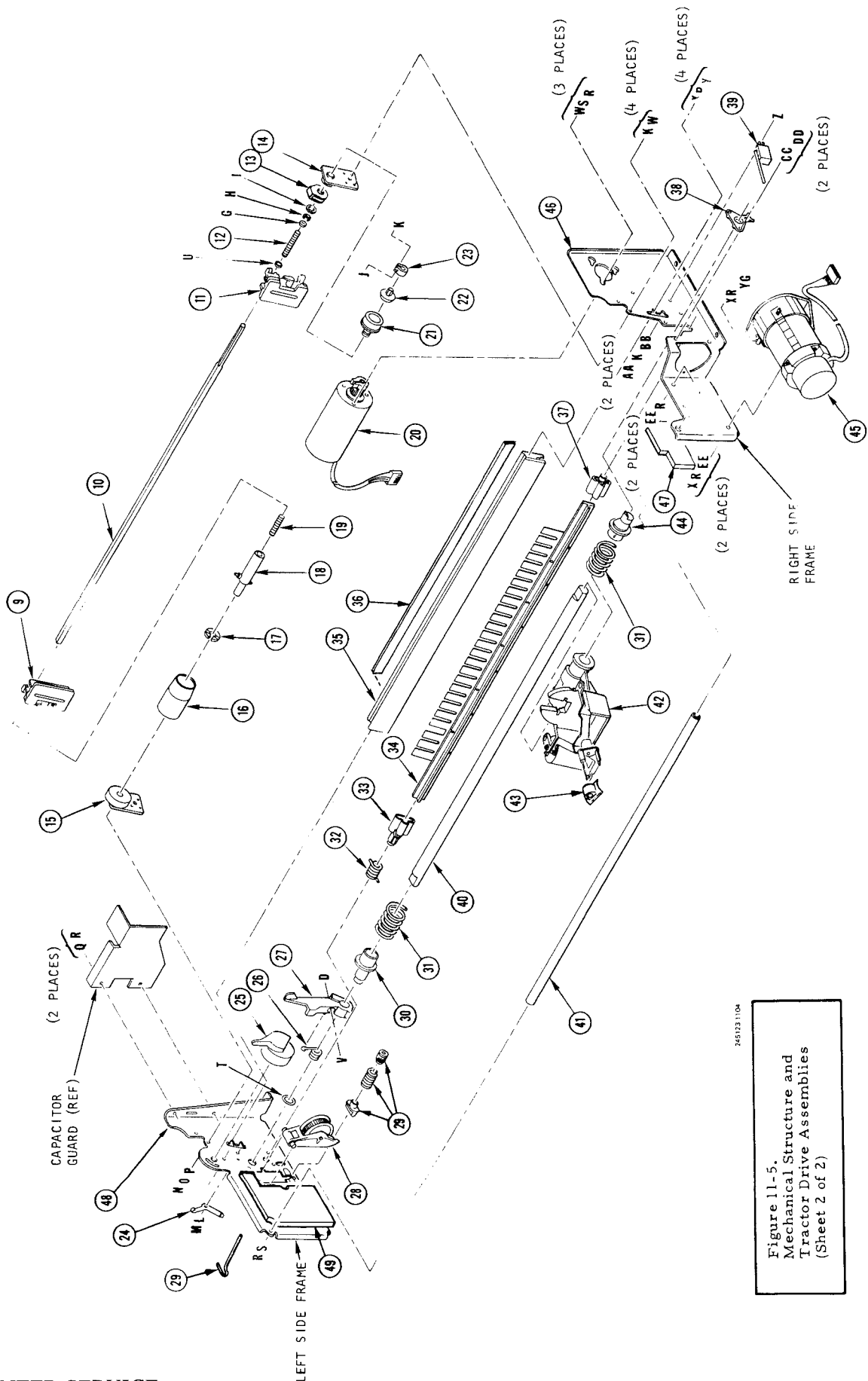


Figure 11-5.
Mechanical Structure and
Tractor Drive Assemblies
(Sheet 2 of 2)

ILLUSTRATED PARTS LIST

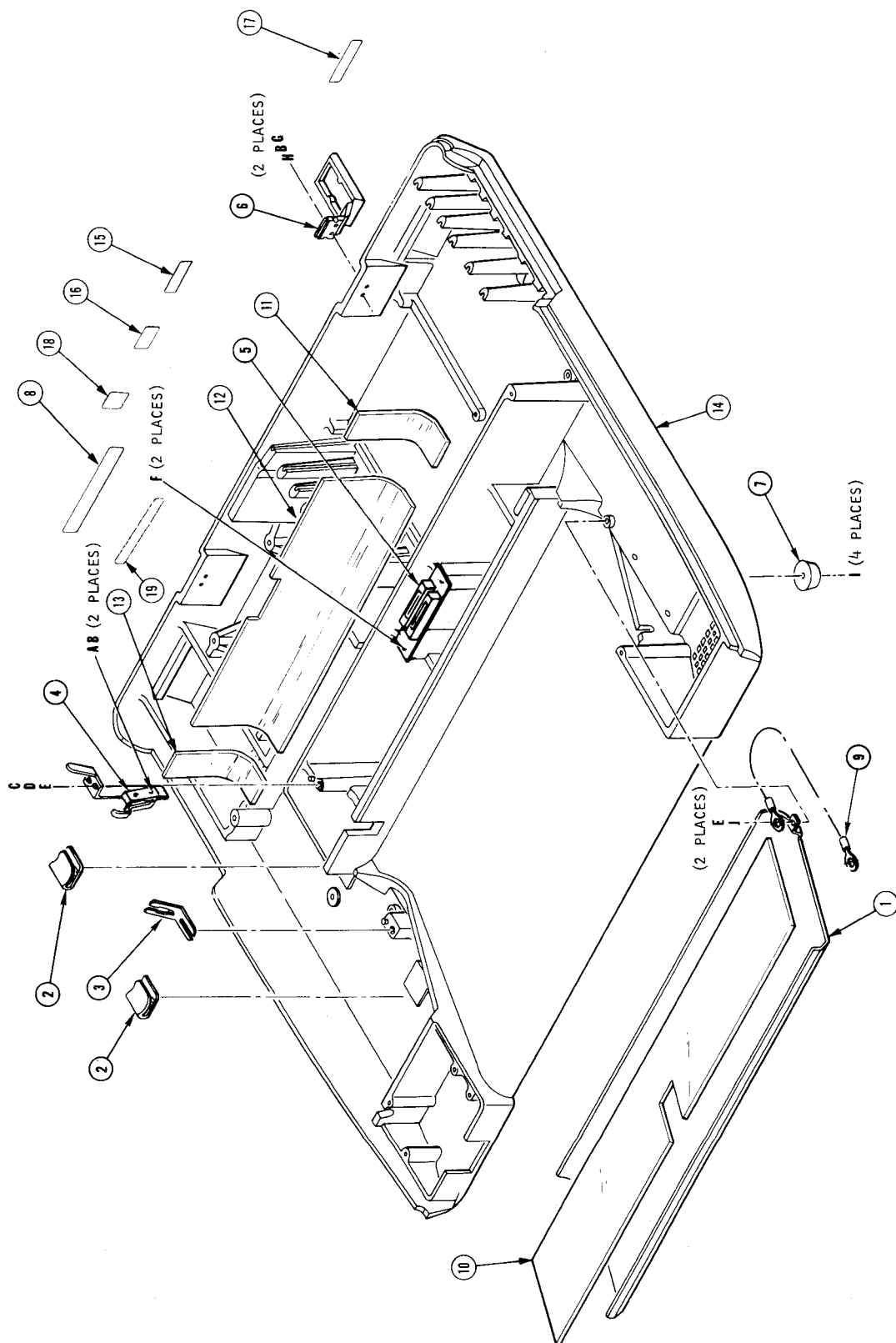


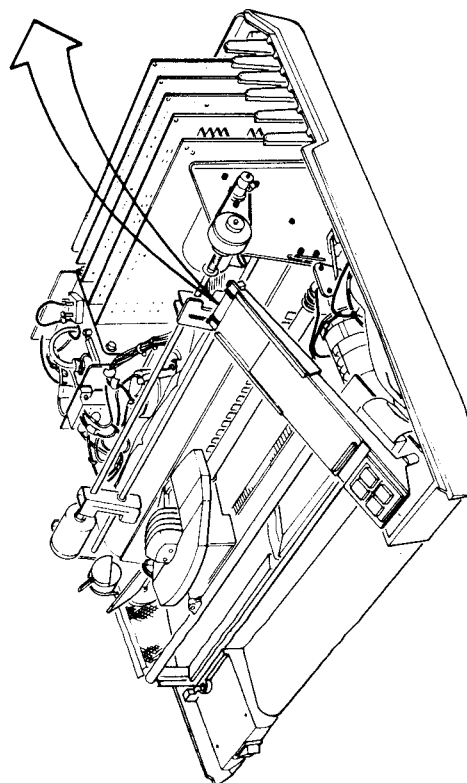
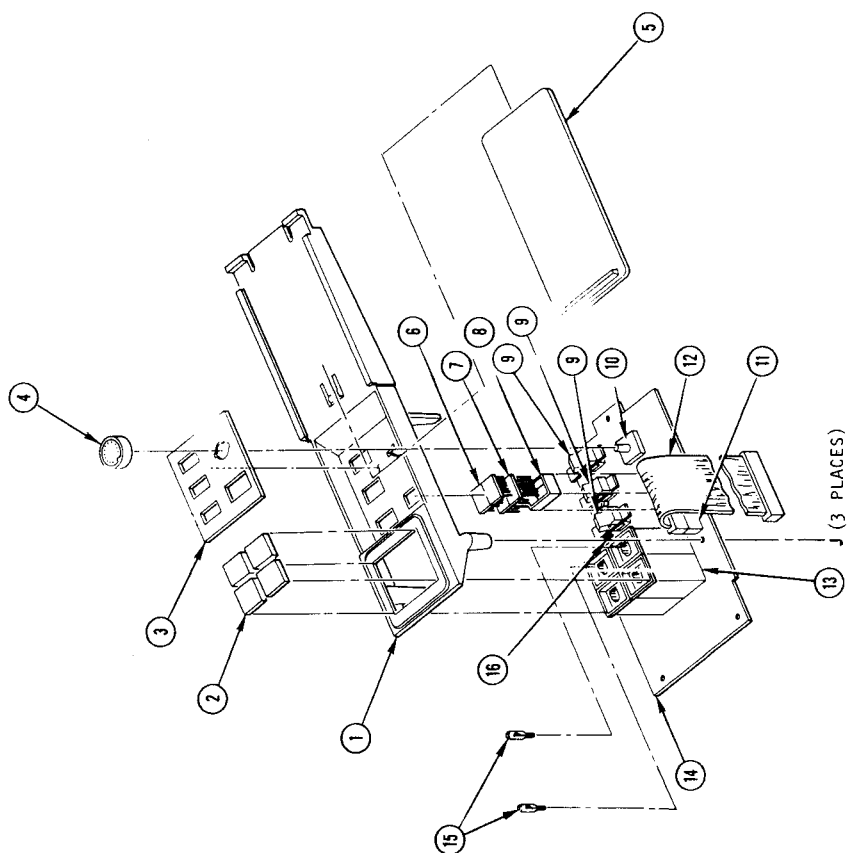
Figure 11-6. Base Assembly

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
11-6	-----	-----		-		BASE ASSEMBLY		
-1	118-1473-00			1		CHUTE PAPER:		245580-001
-2	343-0775-00			12		CLIP, SPR TNSN: CABLE	76381	3484-1000
-3	118-1471-00			1		BRACKET MOUNTING:	-----	271907-001
-4	118-1304-00			1		SWITCH ASSY: PAPER OUT	-----	261003-001
-5	118-1142-00			1		TIME METER ASSY:	-----	271896-001
-6	118-1456-00			2		COVER, KEEPER:	-----	801949-002
-7	118-1472-00			4		FOOT: NEOPRENE	-----	801656-001
-8	-----			1		LABEL: TO AVOID ELECT SHOCK	-----	249848-001
-9	118-1454-00			1		LEAD ELECT: GROUND CABLE ASSY	-----	249505-001
-10	-----			1		PADDING, SOUND: PAPER CHUTE	-----	261437-001
-11	-----			1		PADDING, SOUND: BASE BAFFLE RIGHT	-----	261440-001
-12	-----			1		PADDING, SOUND: BASE BAFFLE MDL	-----	261439-001
-13	-----			1		PADDING, SOUND: BASE BAFFLE LEFT	-----	261438-001
-14	118-2413-00			1		BASE: PAINTED	-----	261145-241
-15	334-2553-00			1		MARKER, IDENT: MARKED CAUTION	80009	334-2553-00
-16	334-3288-00			1		MARKER, IDENT: MARKED CAUTION	80009	334-3288-00
-17	334-4715-00			1		MARKER IDENT: SERIAL RS232-C LEVELS	80009	334-4715-00
-18	334-4905-00			1		MARKER IDENT: 3AT(SLOW)250V	80009	334-4905-00
	334-4906-00			1		MARKER IDENT: 1.5AT(SLOW)250V	80009	334-4906-00
	-----			-		(OPTION A1, A2, A3, A4)		
-19	334-4932-00			1		MARKER IDENT: 220/240V 50/60HZ 2A	80009	334-4932-00
	-----			-		(OPTION A1, A2, A3, A4)		
	118-1552-00			1		HARDWARE KIT: 4643		
	-----			-		(SEE FIG 11-37)		
-A	-----			2		SCREW PNH, M2.5 X 16MM		
-B	-----			2		WASHER, FLAT, STL M3, 7MM MAX OD		
-C	-----			2		SCREW, PNH STL, M4 X 8MM		
-D	-----			2		WASHER, LOCK SPLIT, STL, M4, 7.3MM MAX OD		
-E	-----			4		WASHER, FLAT, STL M4 X 9MM MAX OD		
-F	-----			2		SCREW, TAPPING, PNH 8 X 0.312 MM		
-G	-----			4		SCREW, FLH, CORROSION RESISTANT STL, M3 X 16MM		
-H	-----			4		NUT, HEX STL M3 X 0.5MM		
-I	-----			4		SCREW, TAPPING, COUNTERSUNK, M3.5 X 6 X 8MM		
-J	-----			2		SCREW, TAPPING, PNH M4 X 7 X 8MM		

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
11-7	118-1321-00		1		CONTROL PANEL ASSEMBLY:	----	261418-016
-1	118-1475-00		1		. HOUSING:CONTROL PANEL	----	249784-001
-2	118-1558-00		1		. KIT,CONTROL PANEL BUTTON:	----	249745-001
-3	118-1474-00		1		. LABEL:CONTROL PANEL	----	249483-001
-4	118-1549-00		1		. KNOB ASSY KIT:	----	249782-001
	-----		-		. (SEE FIG 11-32)		
-5	118-1426-00		1		. DOOR ACCESS:CONTROL PANEL	----	245855-001
-6	118-1140-00		2		. LT EMITTING DIO:STATUS DISPLAY	----	801996-001
	-----		-		. (U1,U2)		
-7	118-1427-00		2		. SOCKET PIN TERM:	----	801915-001
-8	118-1428-00		2		. SPACER SLEEVE	----	245854-001
-9	118-1159-00		3		. SWITCH ROCKER:SPDT	----	801938-001
	-----		-		. (S1,S2,S3)		
-10	118-1288-00		1		. SWITCH ROTARY:16 POSITION	----	801953-001
	-----		-		. (S8)		
-11	118-1429-00		1		. CONNECTOR RCPT ELEC:HEAD	----	801908-001
	-----		-		. (J10)		
-12	118-1141-00		1		. WIRING HARNESS:	----	245829-001
	-----		-		. (SEE FIG 11-24)		
-13	118-1303-00		4		. SWITCH PUSH:SOLID STATE	----	801932-002
	-----		-		. (S4 THRU S7)		
-14	118-1157-00		1		. CKT BOARD ASSY:CONTROL PANEL	----	245865-001
-15	118-1170-00		1		. LAME INCAND:#73	----	801931-001
	-----		-		. (L4,L7)		
-16	214-0579-00		1		. TERM,TEST POINT:BRS CD PL	80009	214-0579-00
	-----		-		. (TPG1)		
	118-1552-00		1		HARDWARE KIT:4643		
	-----		-		. (SEE FIG 11-32)		
-J	-----		1		. SCREW,TAPPING M3.5 X 6.8MM		



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Figure 11-7. Control Panel Assembly

ILLUSTRATED PARTS LIST

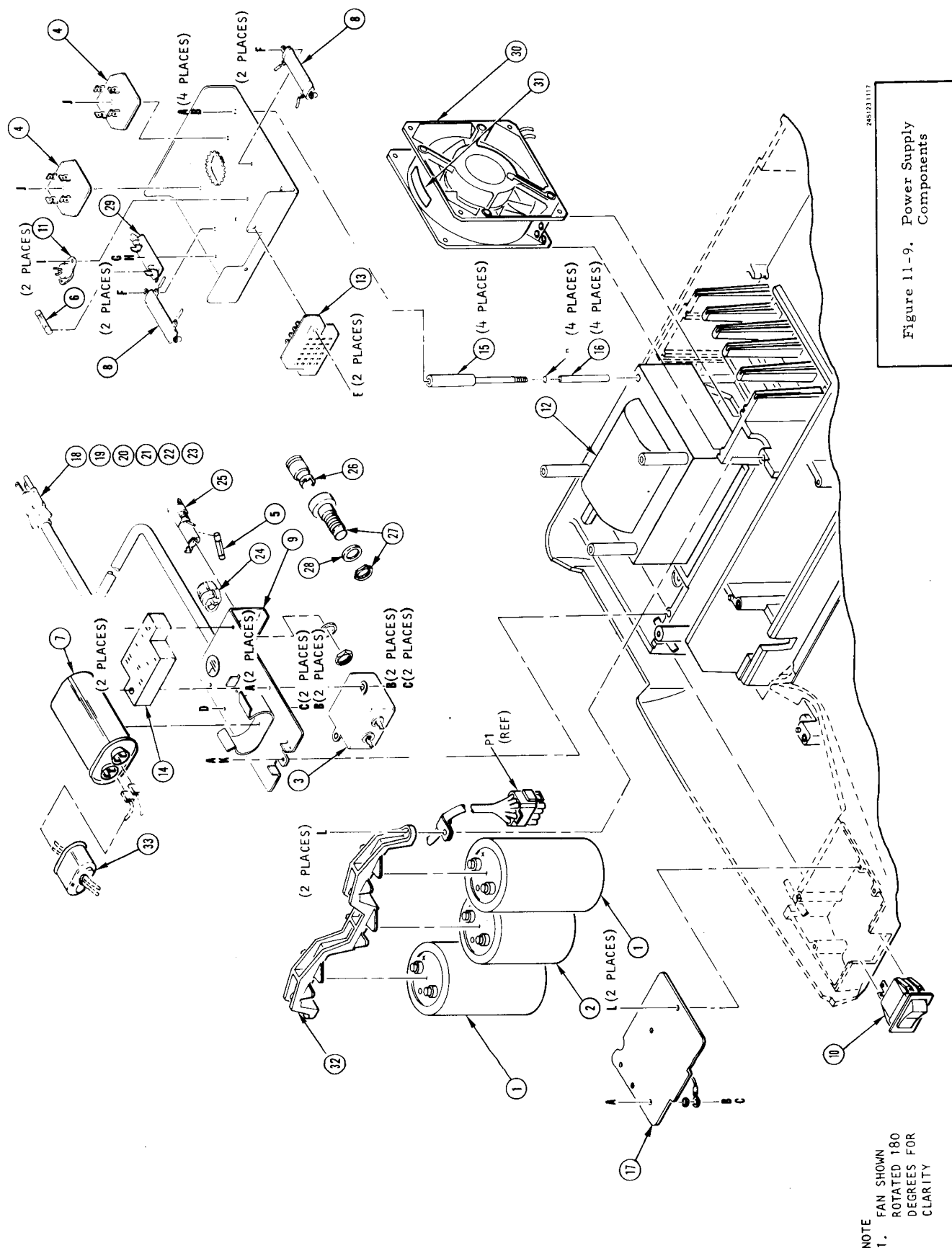


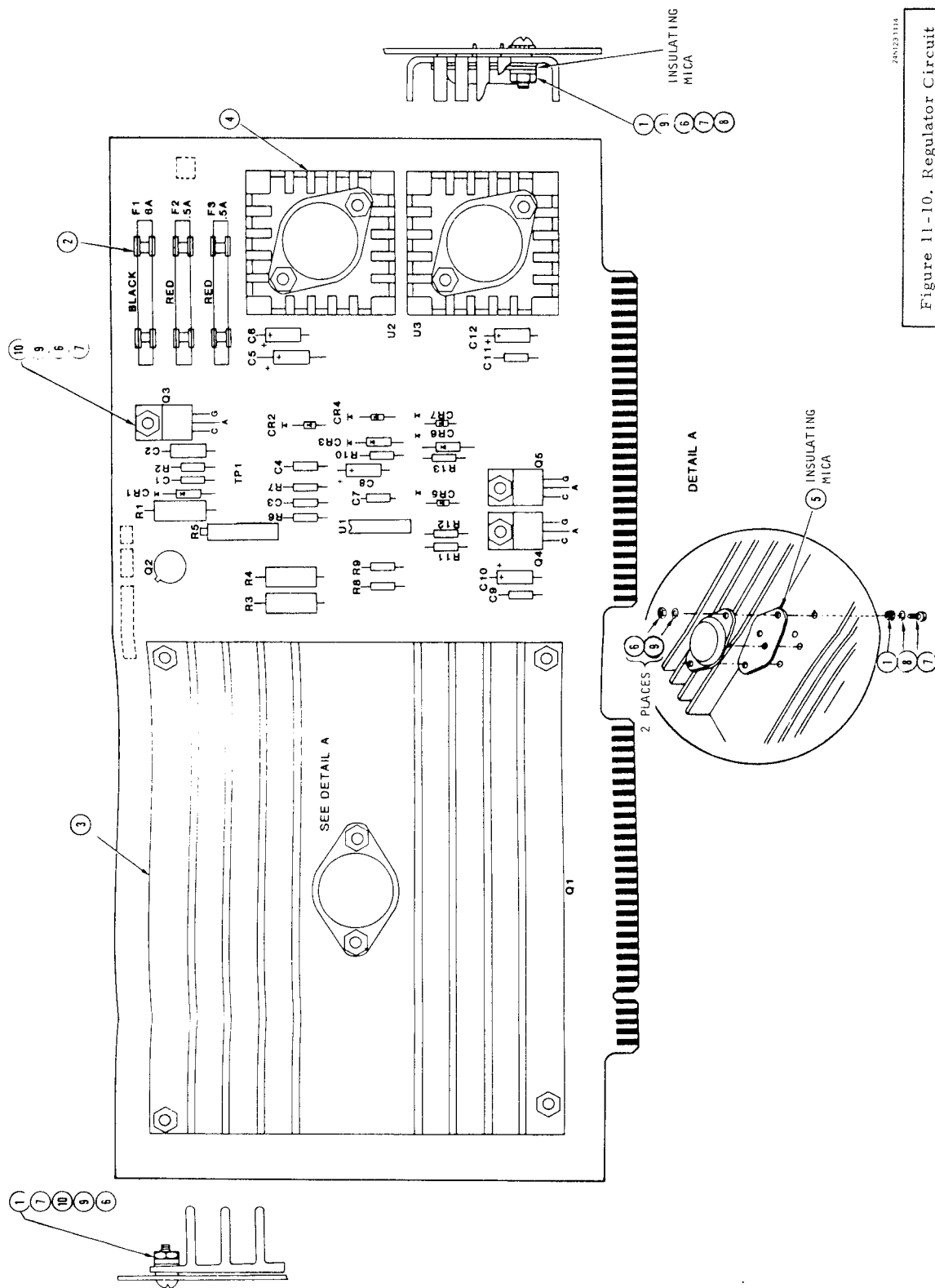
Figure 11-9. Power Supply Components

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
11-9	-----	-----	-		POWER SUPPLY COMPONENTS		
-1	118-1420-00		2		CAP.,FXD,ELECT:68K UF,30V	-----	800092-301
	-----		-		(C1,C2)		
-2	118-1145-00		1		CAP.,FXD,ELECT:77UF,15V	-----	800092-158
	-----		-		(C3)		
-3	118-1419-00		1		CAP.,FXD,ELECT:34F,6%,660V	-----	801944-003
	-----		-		(C4)		
-4	118-1418-00		2		BRIDGE RECT:	-----	801837-001
	-----		-		(CR1,CR2)		
-5	159-0005-00		1		FUSE,CARTRIDGE:3AG,3A,125V,30 SEC,CER	71400	MDA3
	159-0160-00		1		FUSE,CARTRIDGE:3AG,1.5 A,250V,18 SEC,UL	71400	MDX 1-1/2
	-----		-		(F1),(OPTION A1,A2,A3,A4)		
-6	159-0046-00		1		FUSE,CARTRIDGE:3AG,8A,250V,MED-BLOW	71400	ABC 8
	-----		-		(F2)		
-7	118-1417-00		1		FILTER,LINE:	-----	801930-001
	-----		-		(L1)		
-8	118-1416-00		2		POWER RESISTOR ASSY:	-----	245890-001
	-----		-		(R1,R2)		
-9	118-2398-00		1		COVER AC:	-----	271960-001
-10	118-1311-00		1		SWITCH ROCKER:DPST,AC POWER	-----	810137-001
	-----		-		(S1)		
-11	118-1415-00		1		THERMOSTAT ASSY:	-----	245894-001
	-----		-		(S2)		
-12	118-1414-00		1		TRANSFORMER ASSY:	-----	249538-001
	-----		-		(T1)		
-13	118-1413-00		1		BLOCK TERMINAL:	-----	801955-001
	-----		-		(TB1)		
-14	118-1412-00		4		BLOCK,TERMINAL:	-----	801955-002
	-----		-		(TB2)		
-15	118-1524-00		4		STANDOFF,TRANSFORMER:	-----	245808-002
-16	118-1523-00		4		SLEEVE TRANSFORMER:	-----	245824-002
-17	118-2397-00		1		COVER AC:	-----	271873-001
-18	118-1302-00		1		CABLE ASSY POWER:AC MOLDED MALE PLUG	-----	801627-001
-19	161-0017-32		1		CABLE ASSY POWER:EUROPEAN	80126	OBD
-20	161-0017-33		1		CABLE ASSY POWER:UNITED KINGDOM	80126	OBD
-21	161-0017-34		1		CABLE ASSY POWER:AUSTRALIAN	S3109	OBD
-22	334-3995-00		1		MARKER IDENT:CAUTION	80009	334-3995-00
-23	161-0017-35		1		CABLE ASSY POWER:NORTH AMERICAN	80126	OBD
-24	358-0025-00		1		BSHG,STRAIN RLF:	28520	SR-6P-4
	-----		-		(OPTION A1,A2,A3,A4)		
-25	118-1513-00		1		FUSEHOLDER:3AG RIGHT ANGLE	-----	801652-001
-26	200-2264-00		1		CAP.,FUSEHOLDER:3AG FUSES	S3629	FEK 031 1666
	-----		-		(A1,A2,A3,A4)		
-27	204-0833-00		1		BODY,FUSEHOLDER:3AG & 5 X 20MM FUSES	S3629	031.1653(MDLFEU)
	-----		-		(A1,A2,A3,A4)		
-28	210-1039-00		1		WASHER,LOCK:INT,0.521 ID X 0.625 INCH OD	24931	OBD
	-----		-		(A1,A2,A3,A4)		
-29	352-0515-00		1		FUSE HOLDER:3AG,15A,250V,CHASSIS MOUNTED		
-30	118-1293-00		1		FAN ASSY:	-----	245899-001
-31	118-1290-00		1		MARKER IDNET:ELECTRICAL SHOCK	-----	249858-001
-32	118-1521-00		1		CLAMP,CAPACITOR:	-----	245003-001
-33	118-1522-00		1		BOOT,CAP:RUBBER	-----	800670-001
	118-1552-00		1		HARDWARE KIT:4643		
	-----		-		(SEE FIG 11-37)		
-A	-----		2		. SCREW,PNH STL M4 X 8MM		
-B	-----		13		WASHER,LOCK,EXTERNAL TOOTH,STL SIZE 4		
-C	-----		5		NUT,HEX,LARGE PATTERN,STL M4 X 0.7MM		
-D	-----		1		SCREW,PNH,STL,M4 X 16MM		
-E	-----		4		SCREW,PNH STL,M4 X 20MM		
-F	-----		4		SCREW,PNH STL,M3 X 10MM		
-G	-----		1		SCREW,PNH,STL,M3 X 8MM		
-H	-----		1		WASHER,FLAT,STL,M3		
-I	-----		2		SCREW,PNH,STL,M3 X 4MM		
-J	-----		2		SCREW,PNH,STL,M3 X 16MM		
-K	-----		1		WASHER,LOCK,SPLIT,STL,M4,7.3 MAX OD		
-L	-----		4		SCREW,TAPPING,COUNTERSUNK,M3.5 X 0.6 X 8MM		

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-10	-----	-----	1						CKT BOARD ASSY:REGULATOR	-----	249785-001
	-----	-----	-						(SEE A6 REPL)		
-1	-----	-----	6						. BUSHING INSULATION	-----	800778-003
-2	334-0154-00		6						. CLIP,ELECTRICAL:FUSE,CKT BD MT,CU BE	80009	334-0154-00
-3	-----	-----	1						. HEAT SINK:POWER SUPPLY	-----	261587-001
-4	118-1411-00		2						. HEAT SING,XSTR:	-----	800588-003
-5	386-0978-00		3						. INSULATOR,PLATE:TRANSISTOR,MICA	80009	386-0978-00
	-----	-----	-						(FOR HARDWARE SEE FIG 11-37)		
-6	-----	-----	6						. NUT,HEX M2.5		
-7	-----	-----	6						. SCREW,PNH:X-RECESSED STL M2.5 X 14MM		
-8	-----	-----	6						. WASHER,LOCK INTERNAL TOOTH M2.5		
-9	-----	-----	6						. WASHER,SPLIT LOCK,M3,5.9MM		
-10	-----	-----	6						. WASHER,FLAT,STL		



24N1231114

Figure 11-10. Regulator Circuit Card Assembly

Sheet 2 of 2

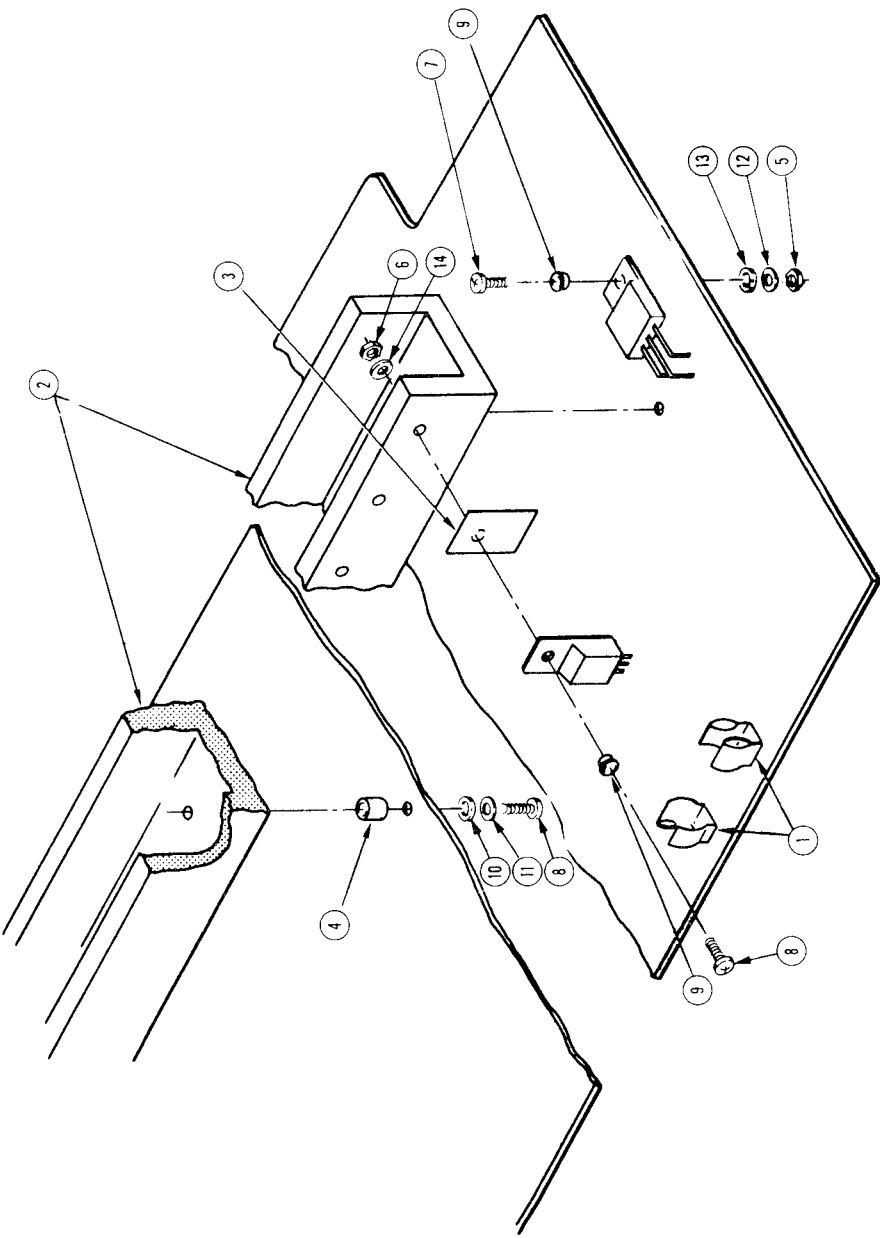


Figure 11-11.
Wire Driver Circuit Card
Assembly (Sheet 2 of 2)

ILLUSTRATED PARTS LIST

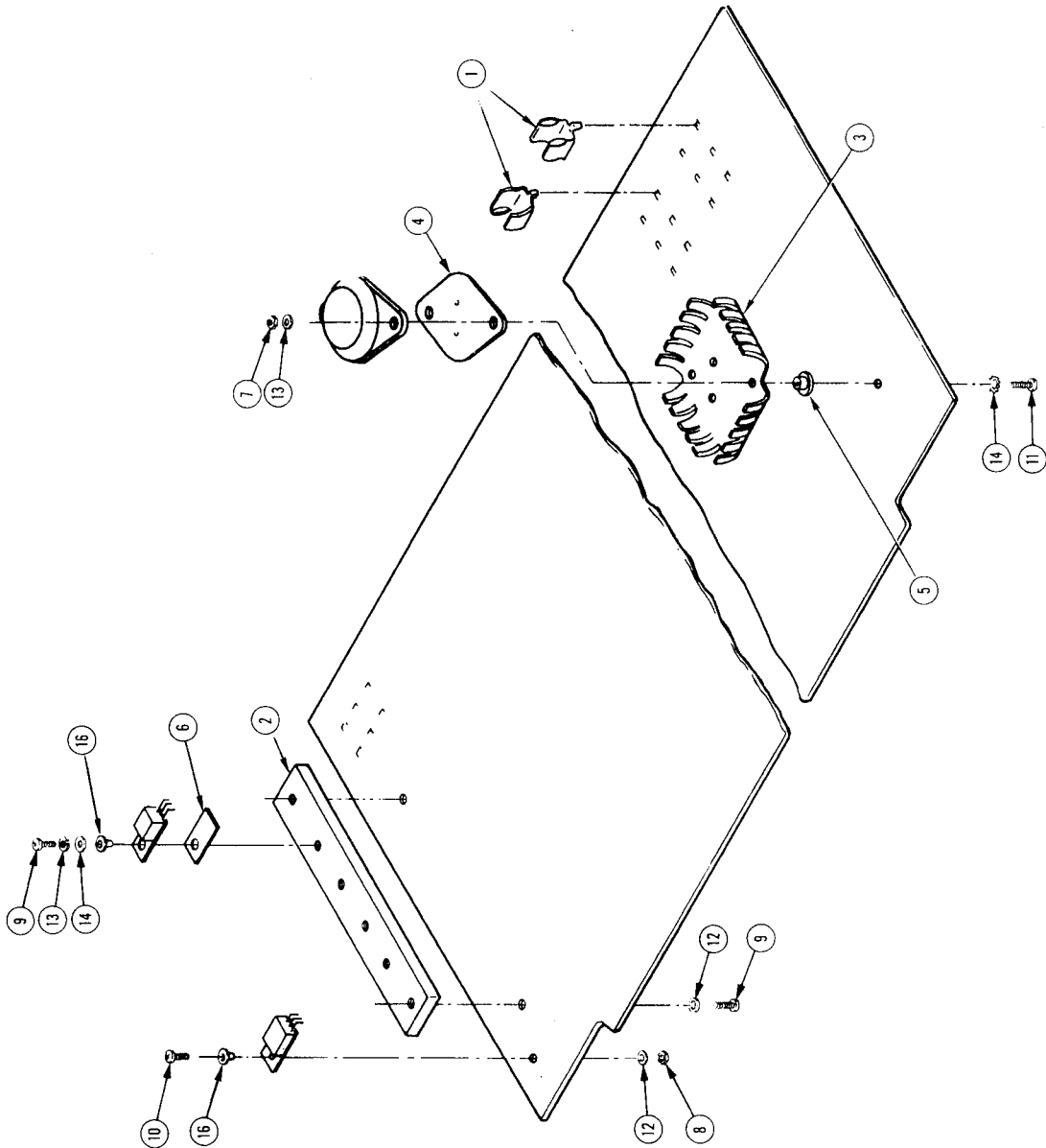
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Discont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-11	-----	-----		1						CKT BOARD ASSY:WIRE DRIVER		
	-----	-----		-						(SEE A5 REPL)		
-1	344-0154-00			14						. CLIP,ELECTRICAL:FUSE,CKT BD MT	80009	344-0154-00
-2	-----	-----		1						. HEAT SINK	-----	261422-001
-3	-----	-----		28						. INSULATOR,RECTANGULAR MICA TO-220	-----	801860-001
-4	-----	-----		3						. INSULATOR TO-3	-----	801881-001
	-----	-----		-						. (FOR HARDWARE SEE FIG 11-37)		
-5	-----	-----		1						. NUT,HEX M3 X 0.5 LARGE PATTERN		
-6	-----	-----		28						. NUT,HEX M2.5		
-7	-----	-----		1						. SCREW,PNH X-RECESSED STL,M3 X 8MM		
-8	-----	-----		31						. SCREW,PNH X-RECESSED STL M2.5 X 10MM		
-9	-----	-----		29						. WASHER INSULATOR SHOULDER		
-10	-----	-----		3						. WASHER FLAT STEEL		
-11	-----	-----		32						. WASHER,LOCK INTERNAL,M2.5,5.9MM		
-12	-----	-----		1						WASHER SPLIT LOCK,M3 X 5.9MM		
-13	-----	-----		1						WASHER,FLAT STL,M3.7MM		
-14	-----	-----		28						WASHER,LOCK EXT M3		

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-12	-----	-----	1						CKT BOARD ASSY:MOTOR DRIVE		
	-----	-----	-						(SEE A4 REPL)		
-1	344-0154-00		8						. CLIP,ELECTRICAL:FUSE,CKT BD MT	80009	344-0154-00
-2	118-1528-00		1						. HEAT SINK,PAPER MOTION	-----	245885-001
-3	118-1411-00		2						. HEAT SINK	-----	800588-003
-4	-----	-----	2						. INSULATOR HEAT SINK	-----	815902-001
-5	-----	-----	4						. INSULATOR SEMICONDUCTOR	-----	815902-003
-6	-----	-----	4						. INSULATOR,MICA		
	-----	-----	-						(FOR HARDWARE SEE FIG 11-37)		
-7	-----	-----	4						. NUT,HEX M3 X 0.5		
-8	-----	-----	4						. NUT,HEX M2.5		
-9	-----	-----	6						. SCREW,PNH,X-RECESSED STL M2.5 X 6MM		
-10	-----	-----	1						. SCREW,PNH,X-RECESSED M2.5 X 8MM		
-11	-----	-----	1						. SCREW,PNH X-RECESSED STL M3 X 14 MM		
-12	-----	-----	3						. WASHER LOCK INTERNAL M2.5		
-13	-----	-----	8						. WASHER SPLIT LOCK M3,5.9MM		
-14	-----	-----	4						. WASHER LOCK,EXTERNAL M3		
-15	-----	-----	4						. WASHER FLAT STL,M3,7MM MAX OD		
-16	-----	-----	5						. WASHER SHOULDER:INSULATING		

245131 108/2

Figure 11-12. Motor Driver
Circuit Card
Assembly
(Sheet 2 of 2)



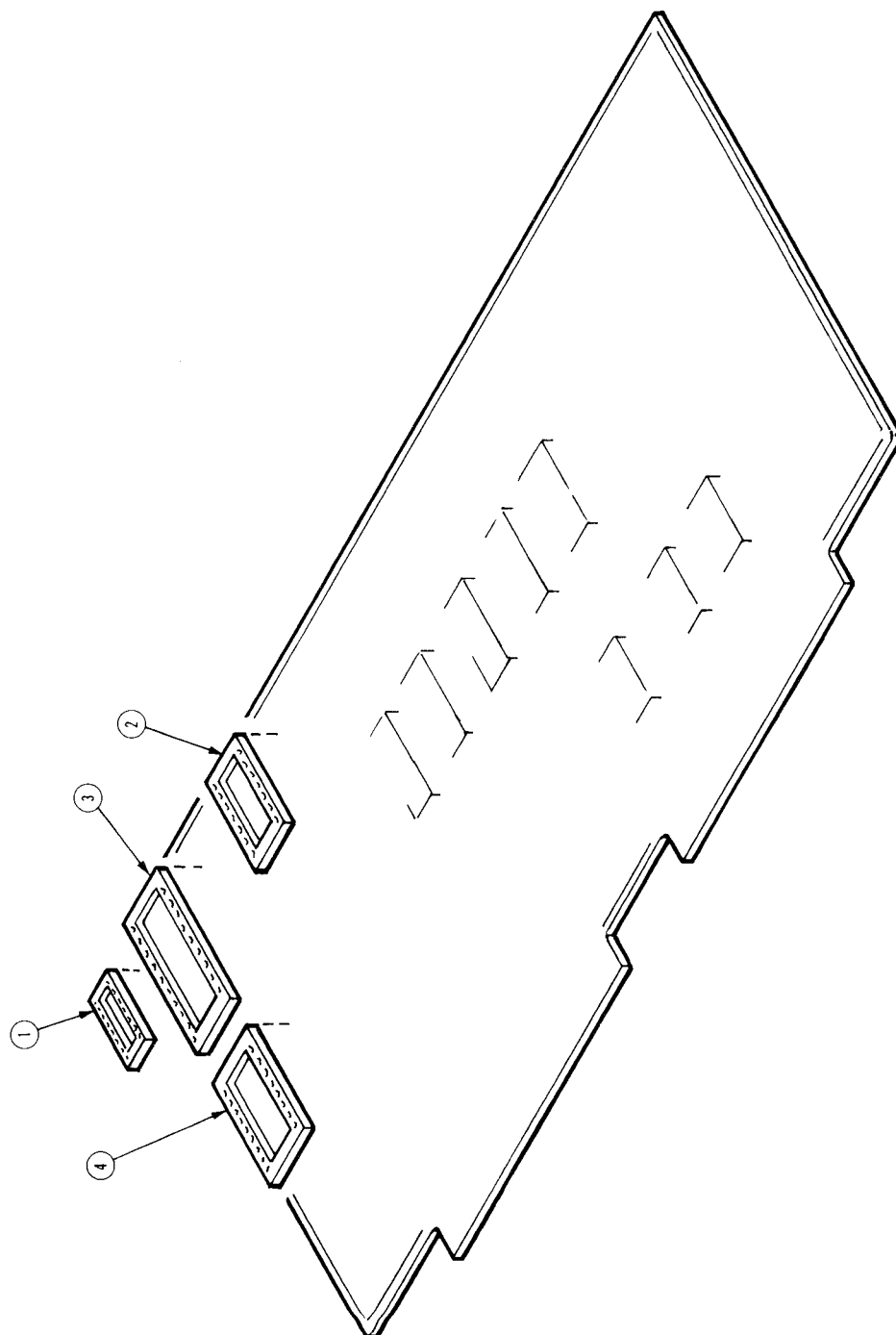


Figure 11-13. Processor Circuit
Card Assembly

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-13	-----	-----	1						CKT BOARD ASSY:PROCESSOR		
			-						(SEE A3 REPL)		
-1	136-0649-00		1						. SKT,PL-IN ELEK:3 CONTACT	-----	801864-003
-2	136-0751-00		5						. SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-3	136-0757-00		1						. SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-4	136-0260-02		1						. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008

ILLUSTRATED PARTS LIST

11-14 -----

1 CKT BOARD ASSY:SHORT LINE PAR INT
- (SEE A2-1 REPL)

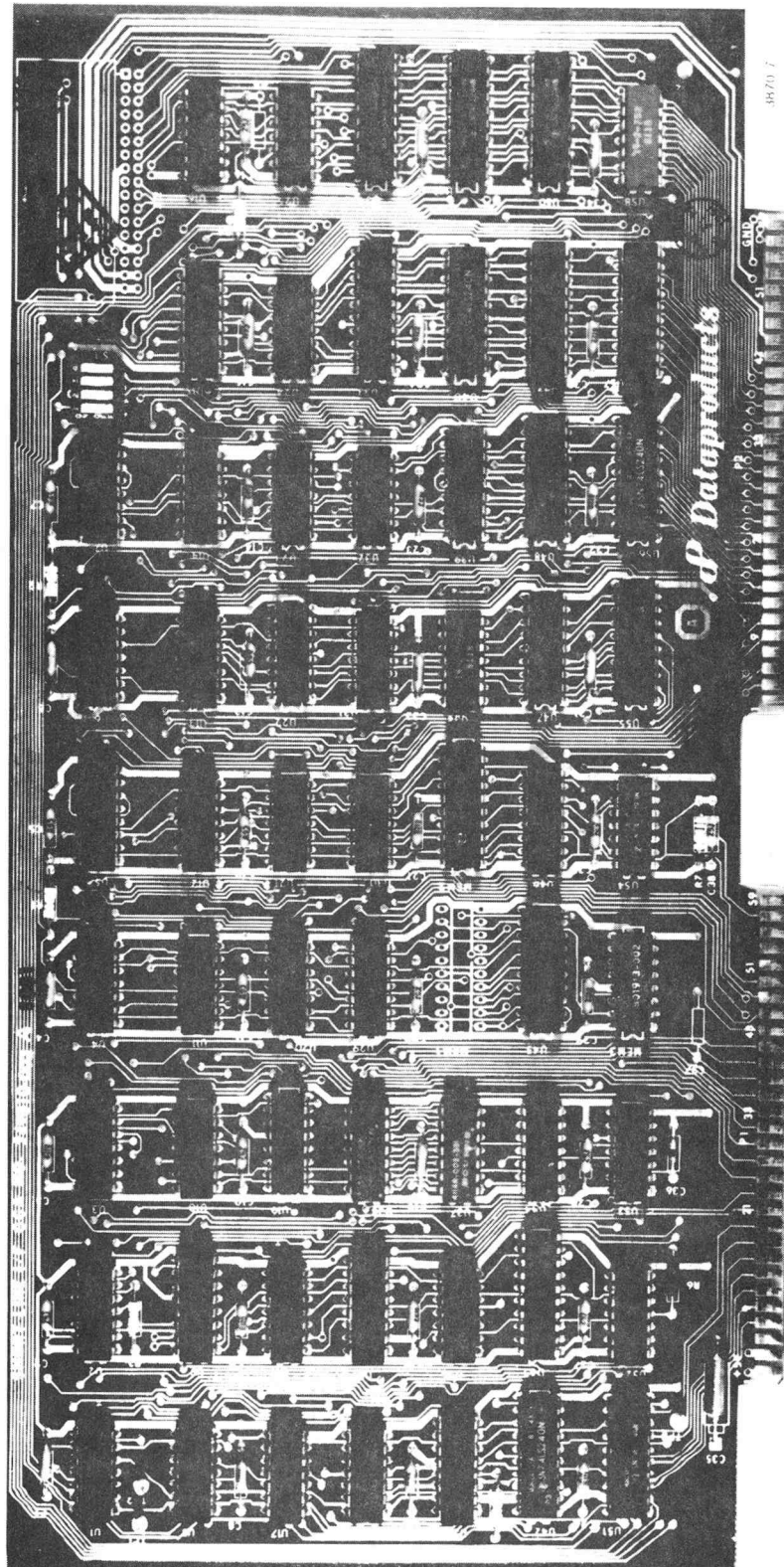


Figure 11-14. DP-14 Short-Line Parallel Interface Circuit Card Assembly

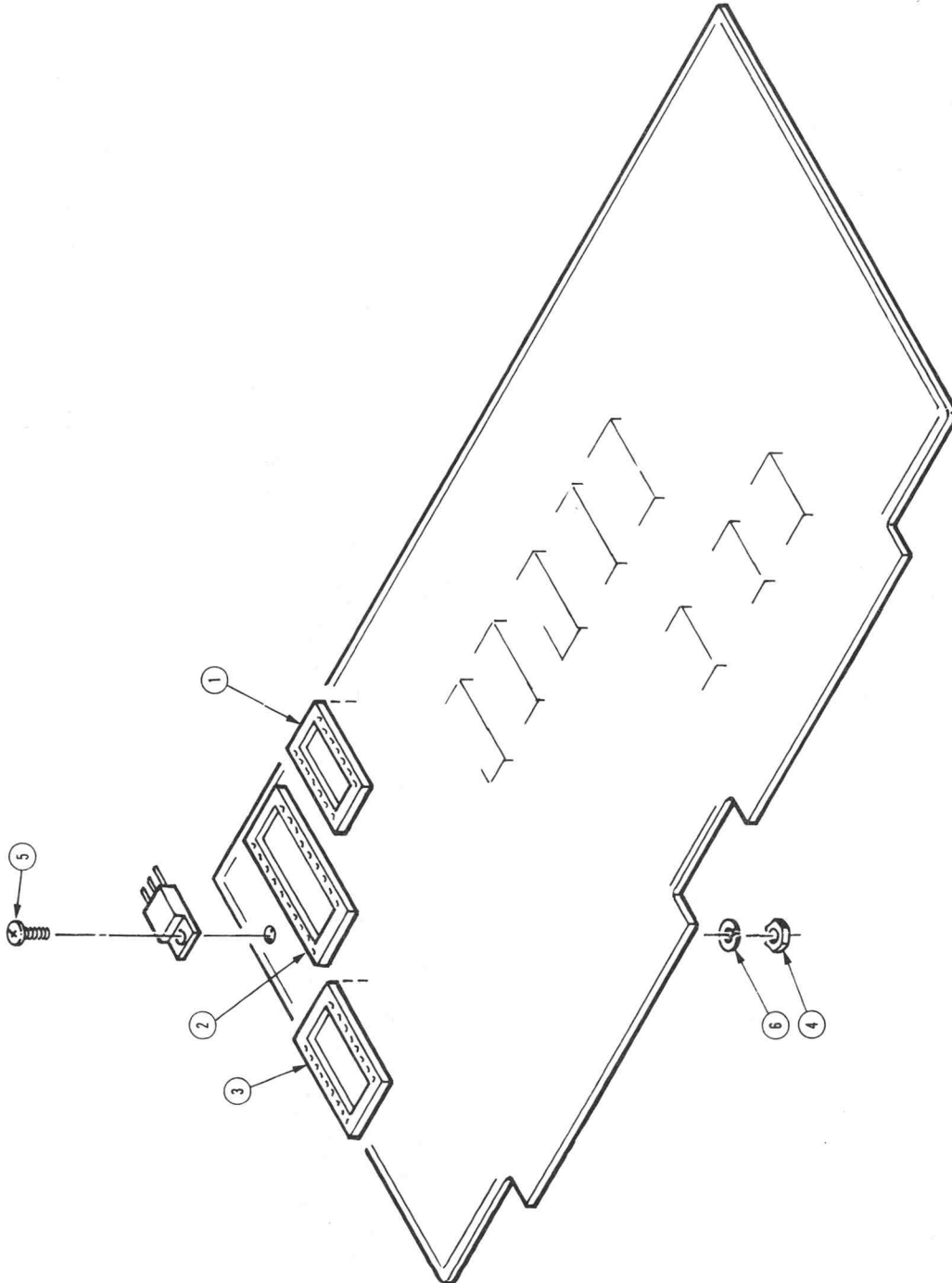


Figure 11-16. Serial Interface Circuit Card Assembly (Option)

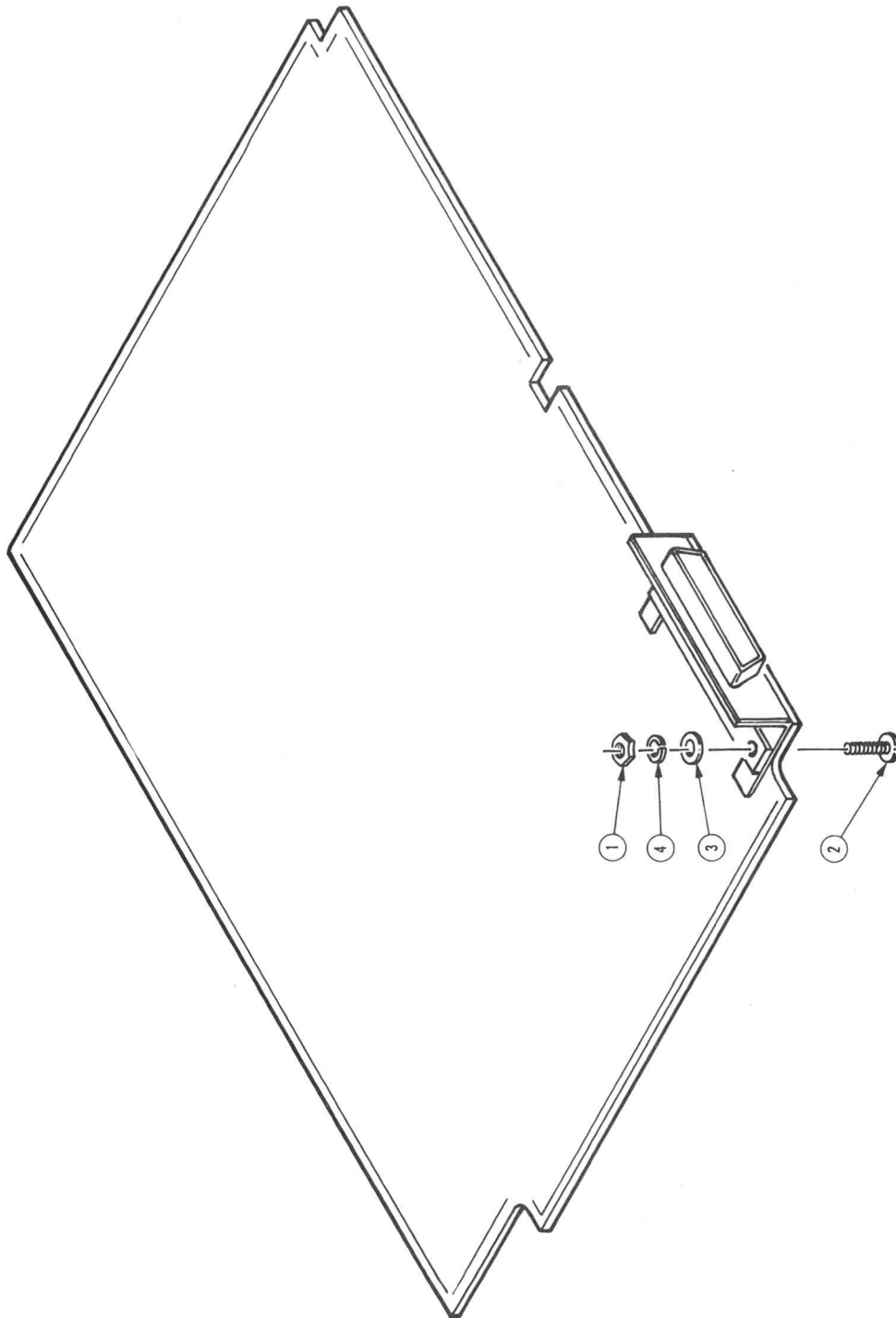
ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-16	-----	-----	1						CKT BOARD ASSY:SERIAL INTERFACE		
	-----	-----	-						(SEE A2 REPL)		
-1	136-0751-00		2						SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-2	136-0623-00		1						SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-3	136-0755-00		2						SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
	-----	-----	-						(FOR HARDWARE SEE FIG 11-37)		
-4	-----	-----	1						. NUT,HEX,M3 X 0.5		
-5	-----	-----	1						. SCREW,PNH STL M3 X 8MM		
-6	-----	-----	1						. WASHER,SPLIT LOCK,M3,5.9MM		

ILLUSTRATED PARTS LIST

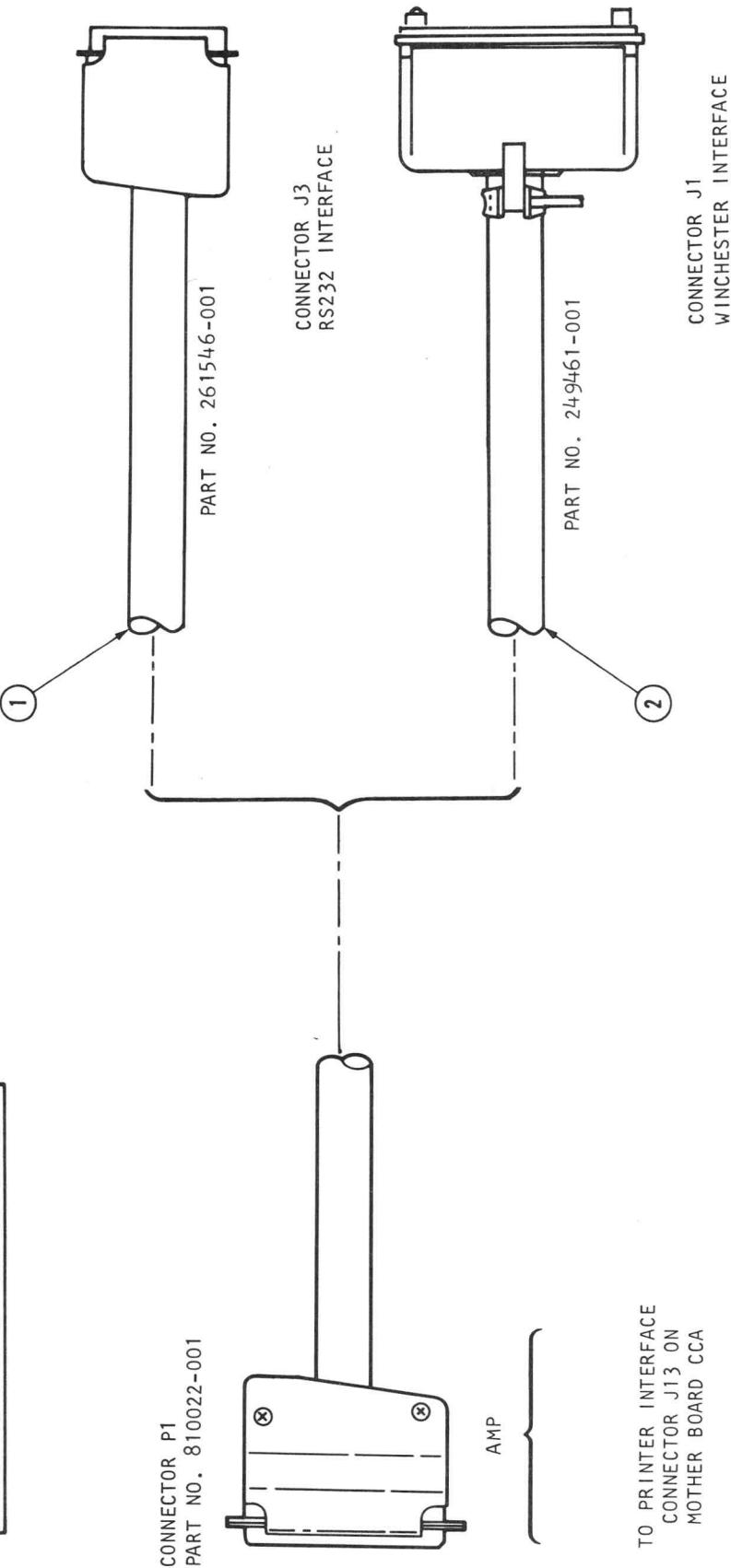
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-18	-----	-----	1						CKT BOARD ASSY:MOTHER		
	-----	-----	-						(SEE A7 REPL)		
	-----	-----	-						(FOR HARDWARE SEE FIG 11-37)		
-1	-----	-----	2						NUT,HEX M2.5		
-2	-----	-----	2						SCREW,PNH,X-RECESSED STL M2.5 X 10MM		
-3	-----	-----	2						WASHER FLAT,STL M3,7MM		
-4	-----	-----	3						WASHER,SPLIT LOCK:M3,5.9MM		

Figure 11-18. Mother Board
Circuit Card
Assembly



245123 1120

Figure 11-19. Adapter Cable Assemblies (Option)



ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-19											
-1	118-1307-00		1						CABLE:AMP TO 25 PIN RS23 ADAPTER	-----	261546-001
-2	118-1306-00		1						CABLE:AMP TO WINCHESTER ADAPTER	-----	249461-001

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-21												
-1	118-1154-00			1						WIRING HARNESS:HEAD FLEX	-----	245830-001
-2	343-0775-00			1						CLIP,SPR TNSN:	76381	3484-1000
-3	-----			1						CABLE CLAMP:	-----	810091-001

HEAD FLEX CABLE (W3)
HARNESS, PART NO. 245830-001

CONNECTOR P3 PLUGS INTO
J3, HEAD CONNECTOR

MOTHER BOARD
CCA (SEE FIGURE
11-18)

2451231129

Figure 11-21. Head Harness
Routing Diagram

①

RIBBON DRIVE
MOTOR B5

RED LEAD WIRE

②

FLAT WIRE CLIP
810049-001

③

BLUE LEAD WIRE

CABLE CLAMP
810091-001

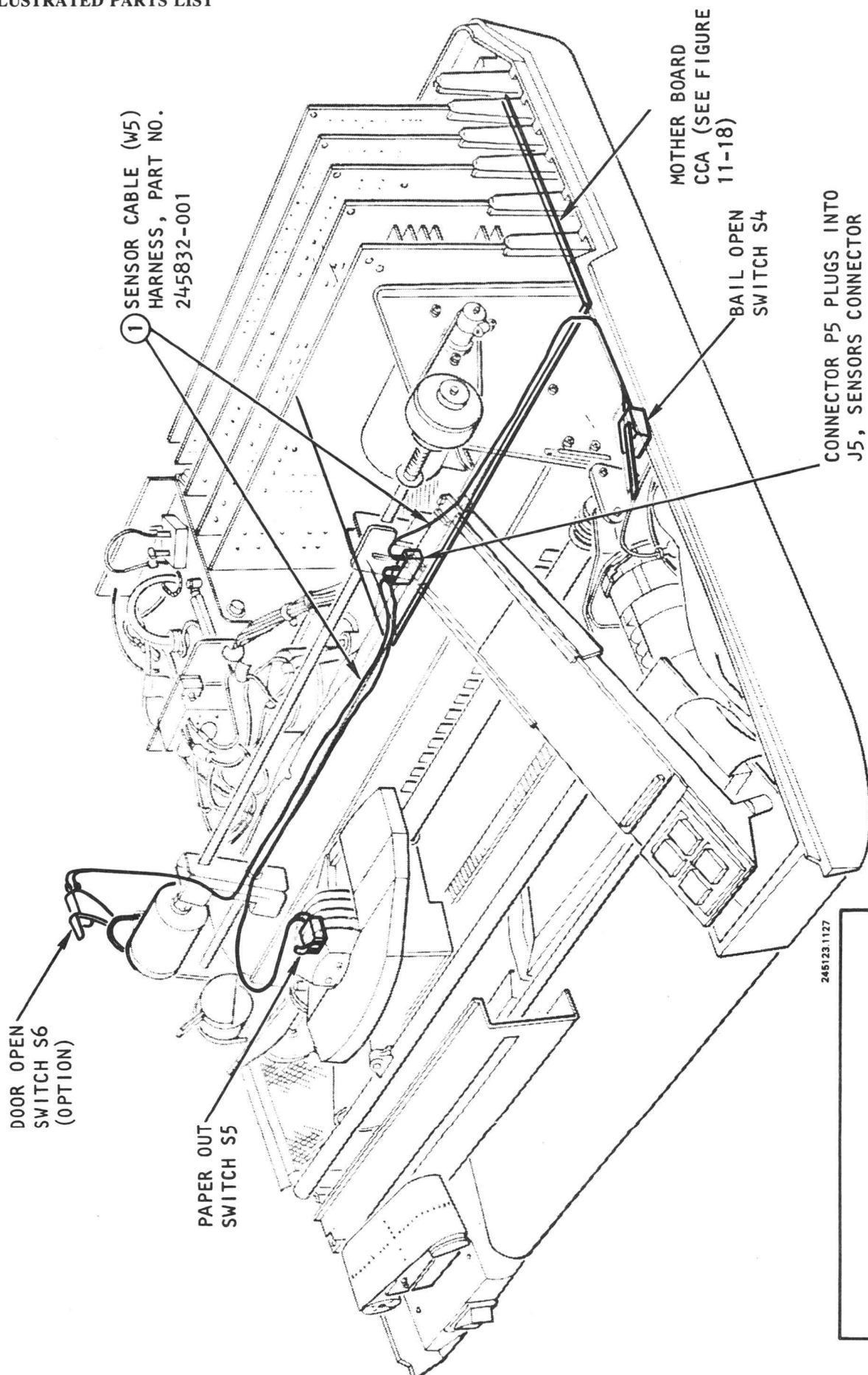


Figure 11-22. Switch Harness Routing Diagram

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-22												
-1	118-1382-00			1						CABLE HARNESS, SENSOR:	-----	245832-001

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-23 -1	118-1471-00		1						COLUMN ONE CABLE	-----	271907-001

COLUMN ONE CABLE (W4)
PART NO. 245834-001

1

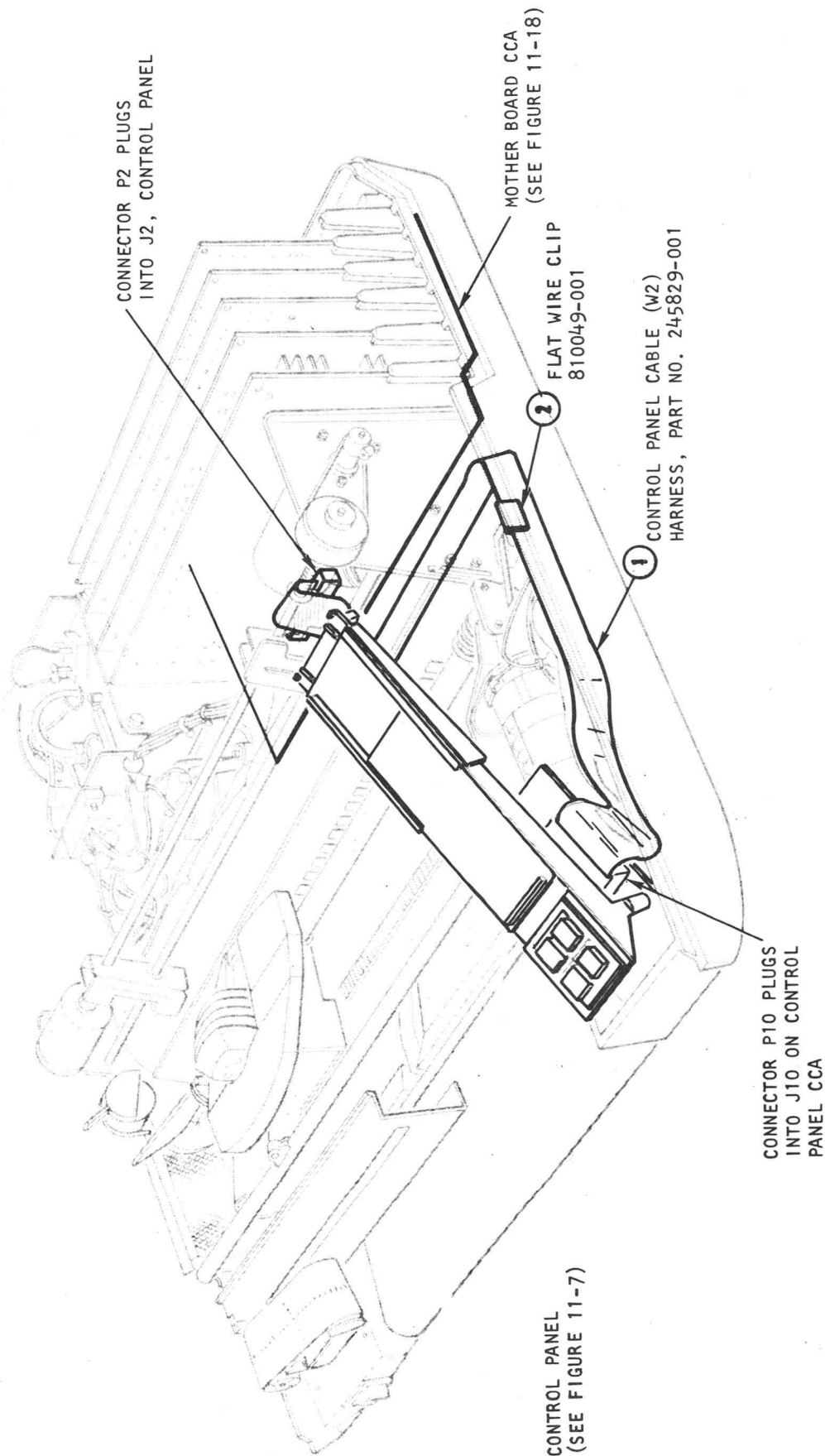
CONNECTOR P4 PLUGS INTO
J4, COLUMN ONE CONNECTOR

COLUMN ONE SENSOR

MOTHERBOARD
CCA (SEE FIGURE
11-18)

245123.1128

Figure 11-23. Column One
Harness Routing
Diagram

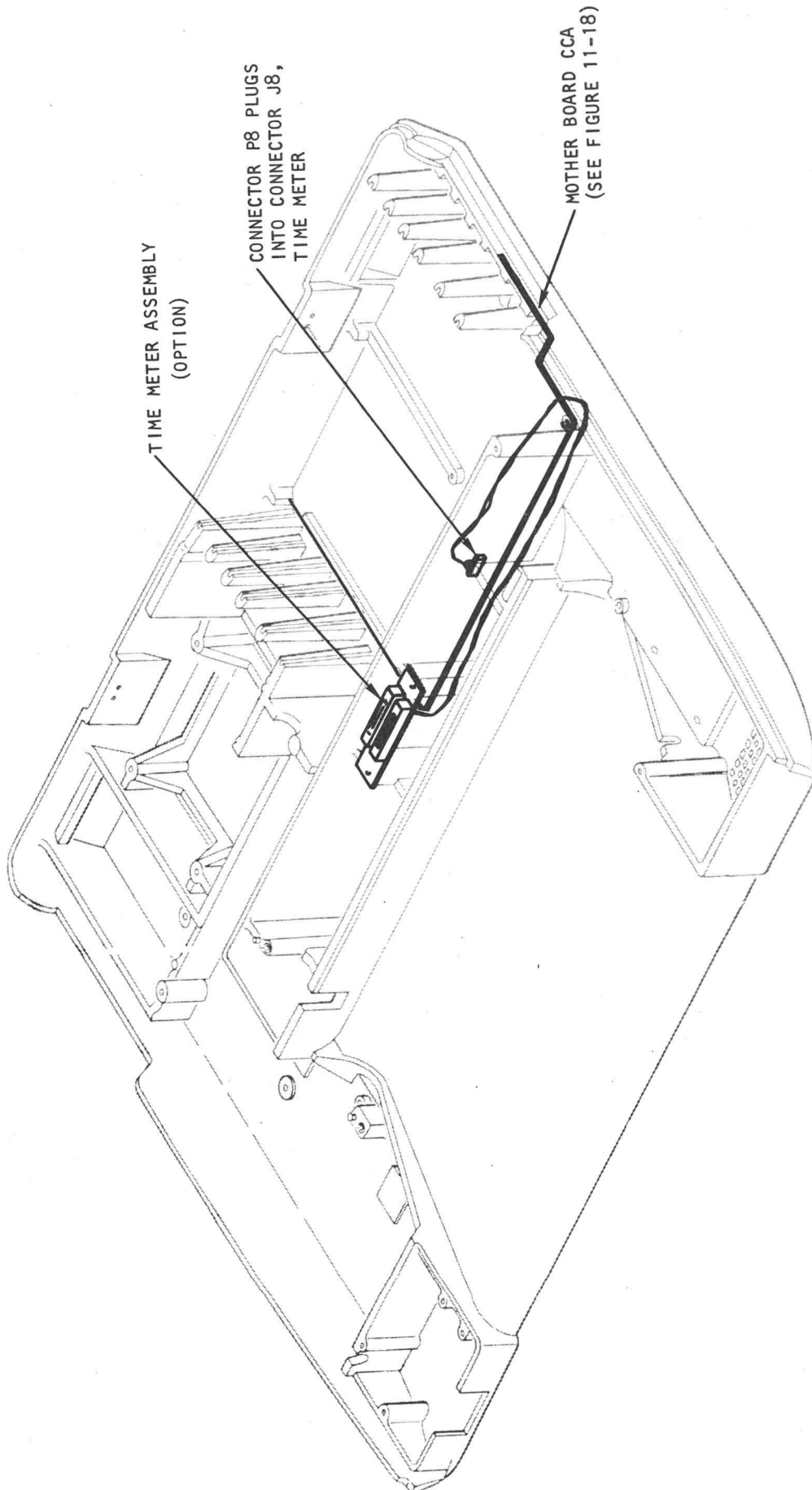


245123 1130

Figure 11-24. Control Panel
Harness Routing
Diagram

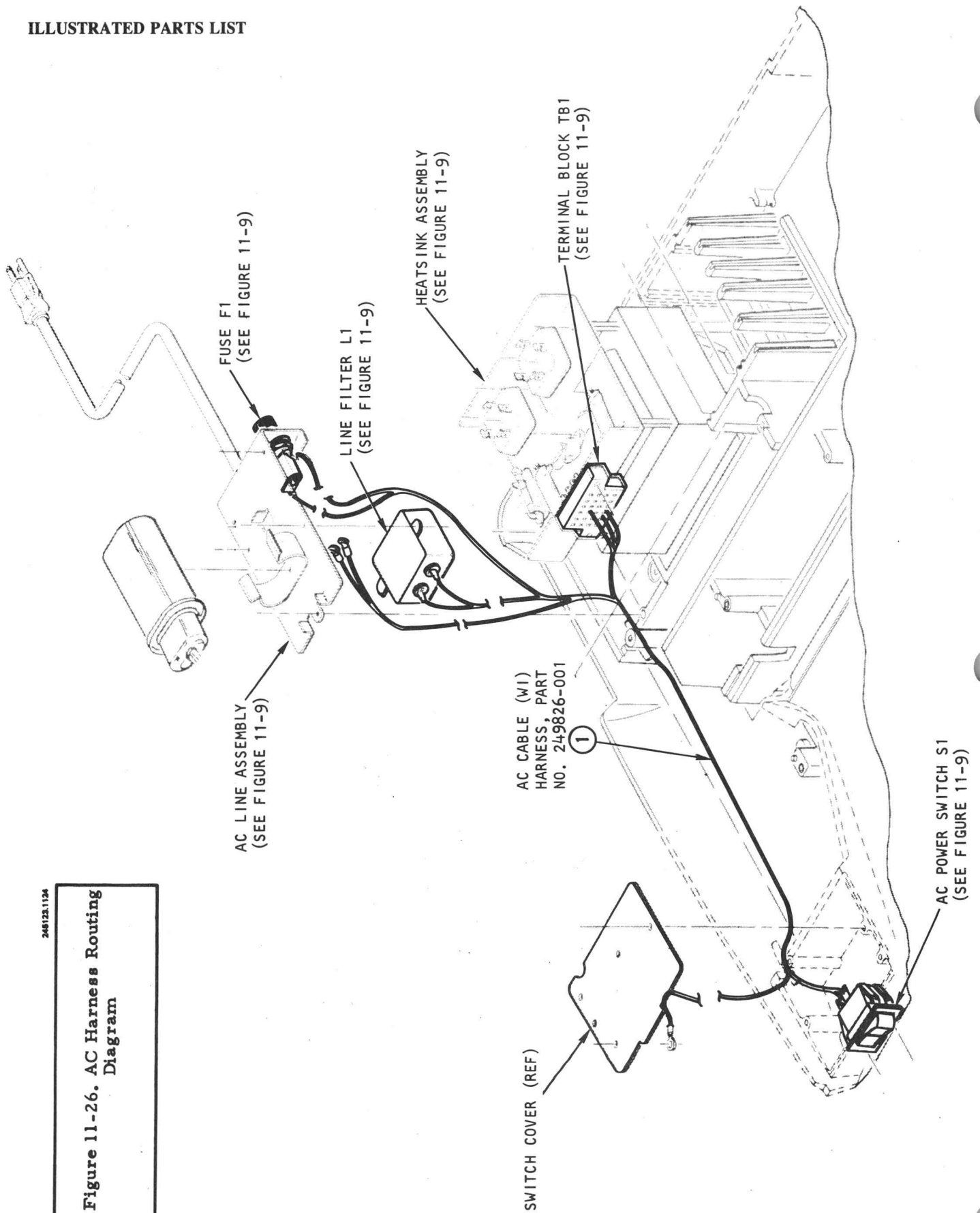
ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-24												
-1	118-1141-00			1						WIRING HARNESS:CONTROL PANEL	-----	245829-001
-2	343-0775-00			1						CLIP,SPR TNSN:	76381	3484-1000



245123 1132

Figure 11-25. Time Meter
Cabling Diagram



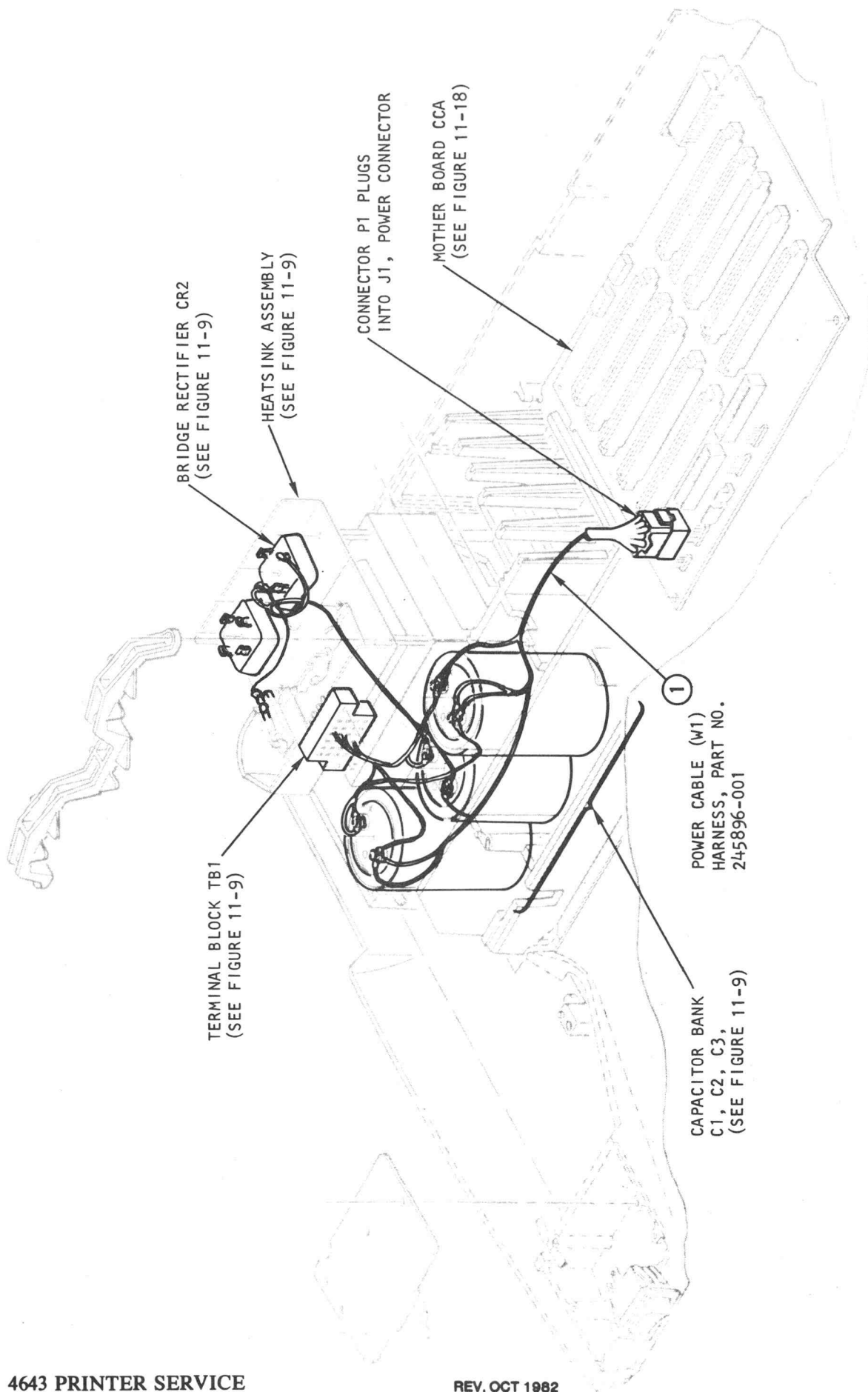
248123.1124

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-26												
-1	118-1383-00			1						CABLE HARNESS,AC:	-----	249826-001

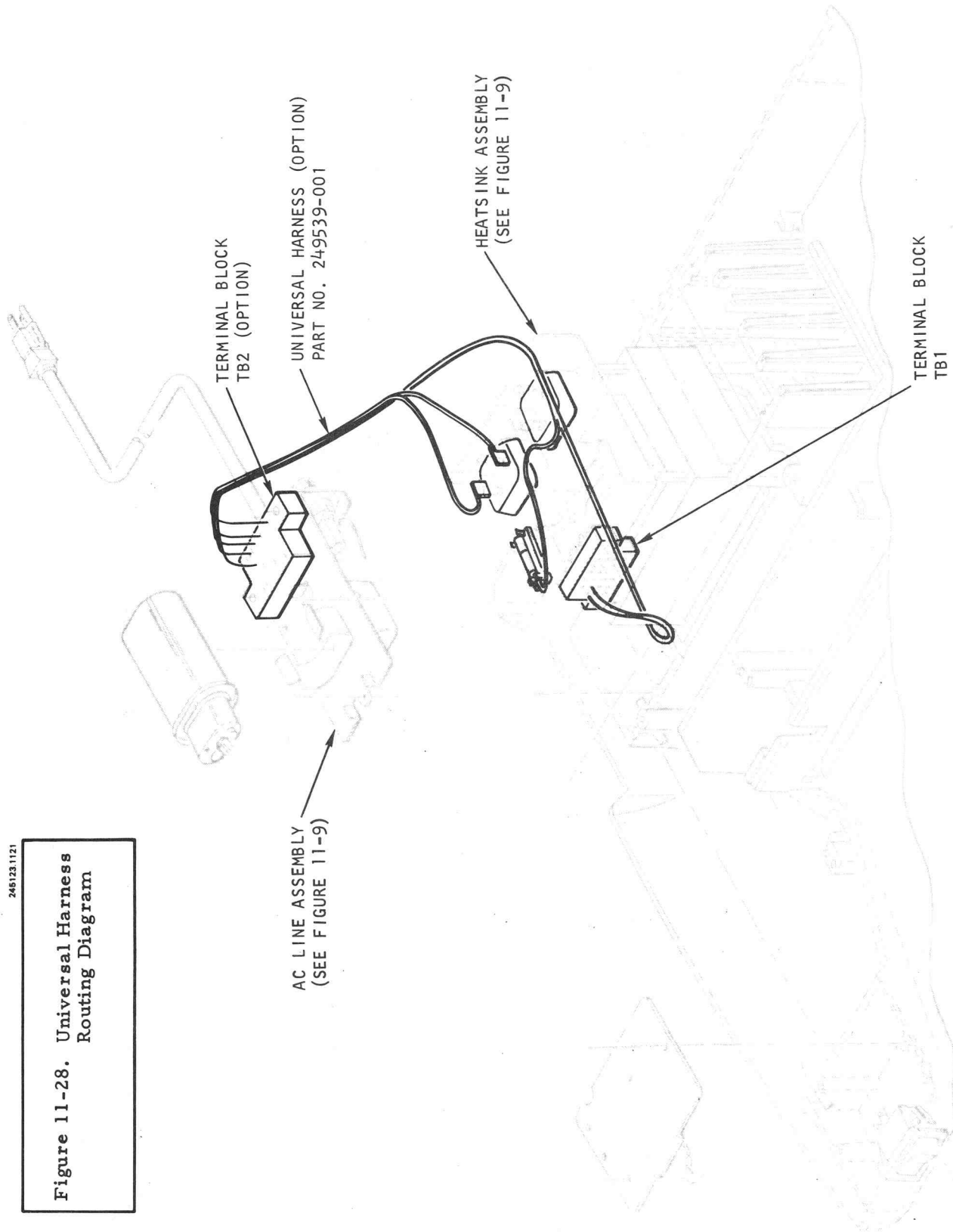
ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-27 -1	118-1527-00			1						WIRING HARNESS, POWER	-----	245896-001



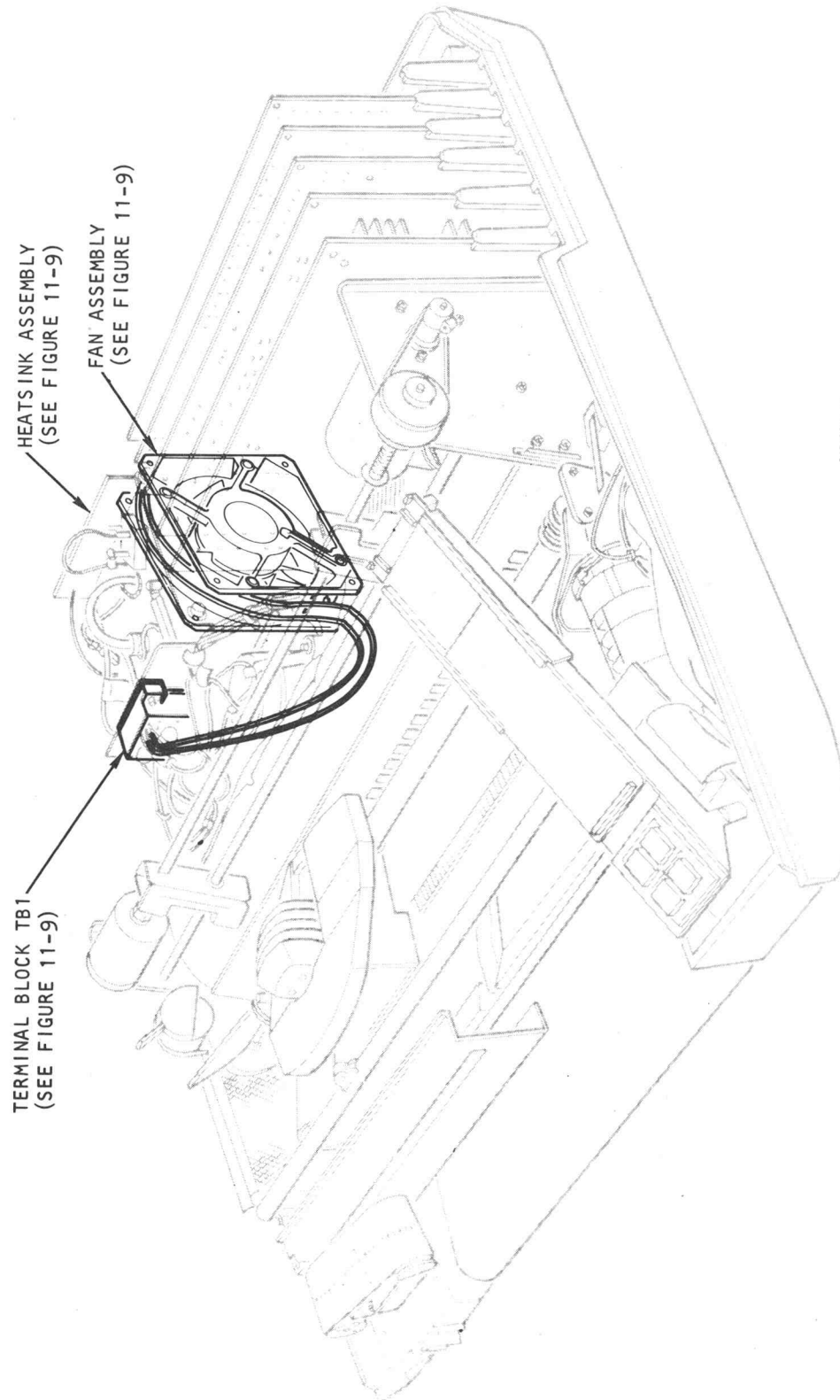
245123 1125

Figure 11-27. Power Harness
Routing Diagram



249539-001

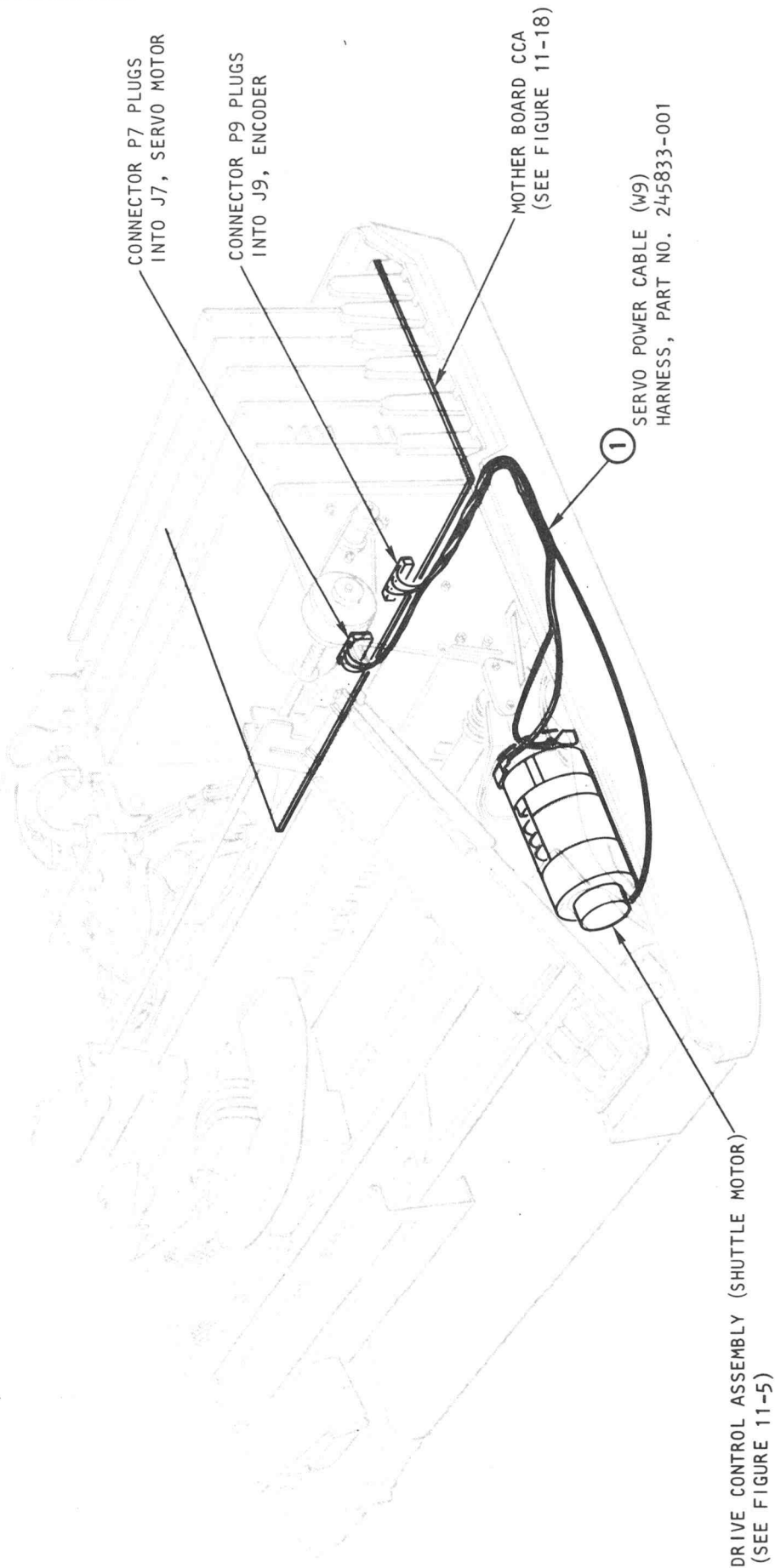
Figure 11-28. Universal Harness
Routing Diagram



245123 1123

Figure 11-29. Fan Cabling Diagram

ILLUSTRATED PARTS LIST



245123 1122

Figure 11-30. Servo Power Harness Routing Diagram

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
FIG 11-30 -1	118-1155-00			1						WIRING HARNESS,SERVO POWER	-----	245833-001

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-31	118-1558-00			1						KIT, CONTROL PANEL BUTTON:	----	249745-001
	-----			1						. KEY, ON LINE	----	249135-001
	-----			1						. KEY, ALARM/CLEAN	----	249135-002
	-----			1						. KEY, PAPER STEP	----	249135-004
	-----			1						. KEY, TOP OF FORM	----	249135-005
	118-1170-00			2						. LAMP, INCAND: #73	----	801931-001

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-32	118-1549-00		1						KNOB ASSY KIT:	-----	261288-001
	-----		1						. KNOB, FORM LENGTH	-----	245536-001
	-----		1						. LABEL, FORM LENGTH	-----	249482-001

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
11-36	118-1551-00		1						SPRING KIT:4643	-----	249748-001
-1	-----	-----	1						. SPRING,PAPER TENSION	-----	245573-001
-2	-----	-----	1						. SPRING,BELT TENSION	-----	245744-001
-3	-----	-----	1						. SPRING,PAPER CHUTE	-----	245733-001
-4	-----	-----	1						. SPRING,ASSEMBLY,DETENTED	-----	245737-001
-5	-----	-----	1						. SPRING SHOULDER	-----	245734-001
-6	-----	-----	1						. SPRING,HUB	-----	245595-001
-7	-----	-----	1						. SPRING,PAPER FEED CLUTCH	-----	254350-001
-8	118-2235-00		2						. SPRING,SHUTTLE BUMPER	-----	245741-001

ILLUSTRATED PARTS LIST

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
11-37	118-1552-00		1		HARDWARE KIT:4643	----	249747-001
-1	----	----	4		WASHER,FRONT BAR	----	245712-001
-2	----	----	4		WASHER,ADJ KNOB	----	245763-001
-3	----	----	4		SCREW,PNH RECESS,STL M2 X 10MM	----	801500-210
-4	----	----	4		SCREW,PNH RECESS,STL M3 X 4MM	----	801500-304
-5	----	----	4		SCREW,PNH RECESS,STL M3 X 6MM	----	801500-306
-6	----	----	4		SCREW,PNH RECESS,STL M3 X 8MM	----	801500-308
-7	----	----	4		SCREW,PNH RECESS,STL M3 X 10MM	----	801500-310
-8	----	----	4		SCREW,PNH RECESS,STL M3 X 16MM	----	801500-316
-9	----	----	4		SCREW,PNH RECESS,STL M3 X 22MM	----	801500-322
-10	----	----	4		SCREW,PNH RECESS,STL M3 X 22MM	----	801500-406
-11	----	----	4		SCREW,PNH RECESS,STL M4 X 8MM	----	801500-408
-12	----	----	4		SCREW,PNH RECESS,STL M4 X 10MM	----	801500-410
-13	----	----	4		SCREW,PNH RECESS,STL M4 X 12MM	----	801500-412
-14	----	----	4		SCREW,PNH RECESS,STL M4 X 16MM	----	801500-416
-15	----	----	4		SCREW,PNH RECESS,STL M4 X 20MM	----	801500-420
-16	----	----	4		SCREW,PNH RECESS,STL M2.5 X 4MM	----	801500-904
-17	----	----	4		SCREW,PNH RECESS,STL M2.5 X 6MM	----	801500-906
-18	----	----	4		SCREW,PNH RECESS,STL M2.5 X 8MM	----	801500-908
-19	----	----	4		SCREW,PNH RECESS,STL M2.5 X 10MM	----	801500-910
-20	----	----	4		SCREW,PNH RECESS,STL M2.5 X 12MM	----	801500-912
-21	----	----	4		SCREW,PNH RECESS,STL M2.5 X 14MM	----	801500-914
-22	----	----	4		SCREW,PNH RECESS,STL M2.5 X 16MM	----	801500-916
-23	----	----	4		SCREW,FLAT HD,CRST,M2 X 8MM	----	801501-208
-24	----	----	4		SCREW,FLAT HD,CRST,M3 X 16MM	----	801501-316
-25	----	----	4		SCREW,FLAT HD,CRST,M4 X 6MM	----	801501-408
-26	----	----	4		NUT,HEX,STL,M2	----	801502-002
-27	----	----	4		NUT,HEX,STL,LARGE PATTERN,M3 X 0.5	----	801502-003
-28	----	----	4		NUT,HEX,STL,LARGE PATTERN,M4 X 0.7	----	801502-004
-29	----	----	4		NUT,HEX,STL,M2.5	----	801502-025
-30	----	----	4		WASHER,FLAT,STL M3,7MM MAX OD	----	801503-003
-31	----	----	4		WASHER,FLT,STL,M4,9MM MAX OD	----	801503-004
-32	----	----	4		WASHER,FLAT,STL M6,13.0MM MAX OD	----	801503-006
-33	----	----	4		WASHER,FLAT,STL,M8	----	801503-008
-34	----	----	4		WASHER,FLAT,STL M14	----	801503-014
-35	----	----	4		WASHER,FLAT,STL M2.5	----	801503-025
-36	----	----	4		WASHER,LOCK,EXT TOOTH STL M3	----	801504-003
-37	----	----	4		WASHER,LOCK,EXT TOOTH,STL SIZE 4	----	801504-004
-38	----	----	4		WASHER,LOCK,INTERNAL TOOTH,STL M3	----	801504-103
-39	----	----	4		WASHER,LOCK,EXTERNAL TOOTH,STL SIZE 4	----	801504-104
-40	----	----	4		WASHER,LOCK,STL M2.5	----	801504-126
-41	----	----	4		WASHER,SPLIT,LK,STL 5.9MM MAX OD	----	801504-003
-42	----	----	4		WASHER,SPLIT,LOCK,STL,M4,7.3 MAX OD	----	801505-004
-43	----	----	4		SCREW,CAP,SKT HD,M3 X 12MM	----	801507-312
-44	----	----	4		SCREW,SET,STL,MAX 6	----	801509-406
-45	----	----	4		SCREW,HEX HD,CAP,STL,M3 X 6MM	----	801513-308
-46	----	----	4		SCREW,HEX HD,CAP,STL,M3 X 25MM	----	801513-325
-47	----	----	4		SCREW,BUTTON HD,STL,M6 X 16MM	----	801519-616
-48	----	----	4		SCREW,TAPTITE	----	801858-001
-49	----	----	4		E CLIP	----	801950-001
-50	----	----	4		WASHER,FLAT,M7,14MM MAX OD	----	801951-004
-51	----	----	4		SCREW,TAPPING,COUNTERSUNK,M3.5 X 8MM	----	801954-001
-52	----	----	4		SCREW,TAPPING,COUNTERSUNK,8 X 0.312 IN	----	801954-002
-53	----	----	4		SCREW,TAPPING,COUNTERSUNK,8 X 0.375 IN	----	801954-003
-54	----	----	4		WASHER,SPRING WAVY	----	810008-001

ILLUSTRATED PARTS LIST

STANDARD ACCESSORIES

070-3871-00	1	MANUAL TECH:OPERATORS	80009	070-3871-00
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OPTIONAL ACCESSORIES

118-1335-00	1	PEDESTAL ASSY:	-----	261406-019
118-2358-00	1	. CATCHER PAPER:	-----	261411-001
118-2359-00	1	. HARDWARE KIT:PEDESTAL	-----	261470-001
118-1308-00	1	BELT,TIMING:103 TEETH	-----	801862-002
-----	-	(TEST FIXTURE)		
070-3870-01	1	MANUAL TECH:SERVICE	80009	070-3870-01

OPTIONS

01	-----	-----	PARALLEL INTERFACE
02	-----	-----	SPECIFIED BAUD
49	-----	-----	RENTAL INDENT TAG
A1	-----	-----	EUROPEAN POWER OPTION
A2	-----	-----	UNITED KINGDOM POWER OPTION
A3	-----	-----	AUSTRALIAN POWER OPTION
A4	-----	-----	NORTH AMERICAN POWER OPTION



Appendix A

SWITCH SETTINGS

PROCEDURE

1. Turn the Printer power off, and unplug the line cord.
2. Open the top cover (see Section 5 of the Service manual).
3. Remove the Serial Interface circuit board. This board is one of several boards inserted vertically into dual sockets on the Mother board near the right-rear (when facing front of instrument) corner of the instrument.
4. Set the three groups of switches (shown in Figure A-1) for for your system requirements. The switch settings are explained below.

SWITCH EXPLANATION

S1-1 This switch establishes the number of stop bits. When ON, there is one stop bit. When OFF, there are two stop bits.

S1-2 Pulsed busy enable/disable is an optional feature which controls DATA TERMINAL READY(DTR), pin 20, of the RS232 connector.

When ON, DTR will be held true whenever the printer is ready to receive data, and held false whenever the printer is not ready for data.

The conditions "true" and "false" are determined as a mark or space according to the switch position of S1-3.

When OFF, DTR functions indentically to the ON position with one exception - DTR will have a brief pulse in the false direction upon receipt of each control code (L/F, C/R, etc.).

SWITCH SETTINGS

- S1-3 ON establishes the printer's DTR true to be a mark, or low voltage, and DTR false to be a space, or high voltage.
- S1-4 This switch can be ON or OFF, since it has no effect on a 4643 printer. It is used in conjunction with a current loop interface that is not available in the 4643.
- S2-1 RECEIVED LINE SIGNAL DETECTOR enable/disable is an input signal to the printer. When active, it indicates that the data communication is receiving a signal from the signal source (printer) which meets its suitability criteria. The enable/disable condition of this switch controls the printer's response to this user-generated signal. This switch should be left ON (RLSD disabled) for most applications.
- S2-2 This switch must be in the ON position for the 4643 to select RS-232 communications. When OFF, current loop communications is selected, which is not available for the 4643 printer.
- S2-3 DATA SET READY (DSR) enable/disable should be set the ON position, which disables DSR detection. This is because Tektronix terminals and computers do not usually use DSR for printer communications.
- S2-4 This switch enables or disables DC1/DC3 (XON/XOFF) flagging. ON enables DC1/DC3 flagging. OFF disables DC1/DC3 flagging.
- S3-1 Switches S3-1 through S3-4 determine the serial interface baud rate. The standard 4643 is preset to 2400 baud. A different baud rate can be specified by the user if Option 61 is present. The following chart specifies switch settings for the various baud rates.

Table A-1

BAUD RATE SWITCH SETTINGS

SWITCH	110	150	300	600	1200	2400	4800	9600
S3-1	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
S3-2	OFF	ON	OFF	OFF	ON	OFF	ON	OFF
S3-3	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
S3-4	ON	ON	ON	ON	OFF	OFF	OFF	OFF

MOTHER BOARD SWITCHES

SWITCH EXPLANATION

- S14-1 (Spare)
- S14-2 (Spare)
- S14-3 ON disables the printer's ability to print expanded print characters. OFF enables the printer's ability to print expanded print characters upon reception of the proper command character, octal code 016.
- S14-4 ON enables the printer's ability to print in condensed mode (16.7 CPI) upon reception of the octal code 022 character. OFF disables the printer's ability to print in condensed mode. The operator selection of condensed mode via the control panel overrides this switch setting.
- S14-5 ON enables the DAVFU option. OFF disables the DAVFU option. The DAVFU option is not available in Tektronix printers, so the switch should remain OFF.
- S14-6 ON allows custom prompts to be logically enabled for code conversion. OFF disables code conversion. Custom prompts for code conversion are not used in Tektronix printers, so the switch should remain OFF.
- S14-7 ON enables the TCVFU option. OFF disables the option. The TCVFU option is not available in Tektronix printers, so the switch should remain OFF.

SWITCH SETTINGS

- S14-8 (Spare)
- S15-1 The Perforation (Perf.) Skip 1 switch and the Perf. Skip 2 switch (S15-7) are interactive. See Table A-2.
- S15-2 ON selects a fixed form length of 12 inches, if no VFU is installed. OFF selects a fixed form length of 11 inches if no VFU is installed.

NOTE

Since Tektronix 4643 printers include a switch-selectable Vertical Format Unit (VFU), S15-2 has no effect on printer operation.

- S15-3 ON selects a character format of seven data bits, excluding parity, stop, and start bits. See Table A-3. OFF selects a character format of eight data bits, excluding parity, stop, and start bits. See Table A-3.
- S15-4 S15-4, in conjunction with S15-6, selects parity as odd, even, don't care, or none. S15-4 ON establishes parity enable. If S15-6 is ON, parity is ODD, and if S15-6 is OFF, parity is EVEN. Switch S15-4 OFF establishes parity disable, so if S15-6 is ON, parity is DON'T CARE, and if S15-6 is OFF, parity is NONE. See Table A-3.
- S15-5 ON activates automatic line feed. This generates an automatic line feed after a carriage return. OFF disables automatic line feed. The line feed command must be part of the user's program, or automatically generated by the host device.
- S15-6 Switch S15-6, in conjunction with S15-4, selects parity as odd, even, don't care, or none. See Table A-3. Don't care parity means that a parity bit must be provided by the host, but the logic level of the bit is of no importance to the printer.
- S15-7 Perforation Skip 2 and Perf. Skip 1 (S15-1) are interactive. See Table A-2.
- S15-8 (Spare)

Table A-2

PERFORATION SKIP SWITCHES

Perf. Skip 1 S15-1	Perf. Skip 2 S15-7	Lines Skipped
ON	ON	0
OFF	OFF	3
OFF	ON	4
ON	OFF	6

NOTE: Interface S1-1 ON for one stop bit, OFF for two stop bits.

Table A-3

4643 SELECTIONS, DATA FORMAT

S15-3	S15-4	S15-6	Start	Data	Parity	Stop
ON	ON	ON	1	7	ODD	1 or 2
ON	ON	OFF	1	7	EVEN	1 or 2
ON	OFF	ON	1	7	DON'T CARE	1 or 2
ON	OFF	OFF	1	7	NONE	1 or 2
OFF	ON	ON	1	8	ODD	1 or 2
OFF	ON	OFF	1	8	EVEN	1 or 2
OFF	OFF	ON	1	8	DON'T CARE	1 or 2
OFF	OFF	OFF	1	8	NONE	1 or 2

NOTE

The international character set prints when 8 data bits has been selected, when bit 8 is 1, and when the parity of incoming data matches the 4643 parity setting. The international character set cannot be printed when 7 data bits has been selected, because the eighth bit enables the international character set.

SWITCH SETTINGS

4643 SWITCH SETTINGS BY PRODUCT GROUP

The following tables are divided into the major Tektronix Product Groups, which are further divided into two main groups of switches, namely, RS-232 interface switches and the Mother Board switches. Each switch is described as it relates to the recommended switch position. The switch positions use the following keys:

- ON = Switch in the ON position
- OFF = Switch in the OFF position
- ... = Switch in the ON or OFF position
- (A) = Switch position may vary depending on the application requirements. Check the detailed switch descriptions for further information.

4050 SERIES

RS-232 Interface Board

Table A-4

RS-232 INTERFACE BOARD SWITCHES

Switch	Position	Description
S1-1	ON	One stop bit
S1-2	ON	Normal DTR flagging
S1-3	OFF	DTR true is a space
S1-4	...	No effect
S2-1	ON	RSLD disabled
S2-2	ON	RS-232 enabled
S2-3	ON	DSR detection disabled
S2-4	OFF (A)	DC1/DC3 flag disabled
S3-1	OFF (A)	2400 baud
S3-2	OFF (A)	2400 baud
S3-3	ON (A)	2400 baud
S3-4	OFF (A)	2400 baud

SWITCH SETTINGS

Mother Board

Table A-5

MOTHER BOARD SWITCHES

Switch	Position	Description
S14-1	...	No effect
S14-2	...	No effect
S14-3	OFF	Expanded print selectable
S14-4	ON	Condensed print selectable
S14-5	OFF	DAVFU disabled
S14-6	OFF	Code Conversion disabled
S14-7	OFF	TCVFU disabled
S14-8	...	No effect
S15-1	OFF (A)	Perf. Skip 1
S15-2	...	No effect
S15-3	ON	Seven data bits
S15-4	OFF (A)	Don't care parity (S15-6)
S15-5	ON (A)	Auto line feed enabled
S15-6	ON (A)	Don't care parity (S15-4)
S15-7	OFF (A)	Perf. Skip 2
S15-8	...	No effect

4020 SERIES TERMINALS

RS-232 Interface Board

Table A-6

RS-232 INTERFACE BOARD SWITCHES

Switch	Position	Description
S1-1	ON	One stop bit
S1-2	OFF	Pulsed DTR flagging
S1-3	OFF	DTR true is a space
S1-4	...	No effect
S2-1	ON	RLSD disabled
S2-2	ON	RS-232 enabled
S2-3	ON	DSR detection disabled
S2-4	ON (A)	DC1/DC3 flag enabled
S3-1	(A)	Baud rate
S3-2	(A)	Baud rate
S3-3	(A)	Baud rate
S3-4	(A)	Baud rate

SWITCH SETTINGS

Mother Board

Table A-7

MOTHER BOARD SWITCHES

Switch	Position	Description
S14-1	...	No effect
S14-2	...	No effect
S14-3	OFF	Expanded print selectable
S14-4	ON	Condensed print selectable
S14-5	OFF	DAVFU disabled
S14-6	OFF	Code conversion disabled
S14-7	OFF	TCVFU disabled
S14-8	...	No effect
S15-1	OFF (A)	Perf. Skip 1
S15-2	...	No effect
S15-3	ON	Seven data bits
S15-4	OFF (A)	Don't care parity (S15-6)
S15-5	OFF	Auto line feed disabled
S15-6	ON (A)	Don't care parity (S15-4)
S15-7	OFF (A)	Perf. Skip 2
S15-8	...	No effect

4110 SERIESRS-232 Interface Board

Table A-8

RS-232 INTERFACE BOARD SWITCHES

Switch	Position	Description
S1-1	ON	One stop bit
S1-2	ON	Normal DTR flagging
S1-3	OFF	DTR true is a space
S1-4	...	No effect
S2-1	ON	RLSD disabled
S2-2	ON	RS-232 enabled
S2-3	ON	DSR detection disabled
S2-4	ON (A)	DC1/DC3 flag enabled
S3-1	OFF (A)	9600 baud
S3-2	OFF (A)	9600 baud
S3-3	OFF (A)	9600 baud
S3-4	OFF (A)	9600 baud

SWITCH SETTINGS

Mother Board

Table A-9

MOTHER BOARD SWITCHES

Switch	Position	Description
S14-1	...	No effect
S14-2	...	No effect
S14-3	OFF	Expanded print selectable
S14-4	ON	Condensed print selectable
S14-5	OFF	DAVFU disabled
S14-6	OFF	Code conversion disabled
S14-7	OFF	TCVFU disabled
S14-8	...	No effect
S15-1	OFF (A)	Perf. Skip 1
S15-2	...	No effect
S15-3	OFF (A)	Eight data bits
S15-4	OFF (A)	No parity (S15-6)
S15-5	ON (A)	Auto line feed enabled
S15-6	OFF (A)	No parity (S15-4)
S15-7	OFF (A)	Perf. skip 2
S15-8	...	No effect

Parameter settings on the 4110 Series to match the above settings are:

PASSIGN PO: 4643
 PBAUD PO: 9600
 PBITS PO: 1 8
 PPARITY PO: NONE
 PFLAG PO: DTR
 PEOF PO: ' '
 PEOL PO: ' '

MDP (8500 SERIES) SYSTEM

RS-232 Interface

Table A-10

RS-232 INTERFACE

Switch	Position	Description
S1-1	ON	One stop bit
S1-2	ON	Normal DTR flagging
S1-3	OFF	DTR true is a space
S1-4	...	No effect
S2-1	ON	RLSD disabled
S2-2	ON	RS-232 enabled
S2-3	ON	DSR detection disabled
S2-4	ON	DC1/DC3 flag enabled
S3-1	OFF (A)	2400 baud
S3-2	OFF (A)	2400 baud
S3-3	ON (A)	2400 baud
S3-4	OFF (A)	2400 baud

SWITCH SETTINGS

Mother Board

Table A-11

MOTHER BOARD SWITCHES

Switch	Position	Description
S14-1	...	No effect
S14-2	...	No effect
S14-3	OFF	Expanded print selectable
S14-4	ON	Condensed print selectable
S14-5	OFF	DAVFU disabled
S14-6	OFF	Code conversion disabled
S14-7	OFF	TCVFU disabled
S14-8	...	No effect
S15-1	OFF (A)	Perf. Skip 1
S15-2	...	No effect
S15-3	OFF	Eight data bits
S15-4	OFF	No parity (S15-6)
S15-5	OFF	Auto line feed disabled
S15-6	OFF	No parity (S15-4)
S15-7	OFF (A)	Perf. Skip 2
S15-8	...	No effect

NOTE: Set switch to ON for 8560 File Paginator.